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ILI9486

a-Si TFT LCD Single Chip Driver
320RGBx480 Resolution and 262K-color

Specification
Preliminary

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1. Introduction

ILI9486 is a 262,144-color single-chip SoC driver for a-Si TFT liquid crystal display with resolution of 320RGBx480 dots, comprising a 960-channel source driver, a 480-channel gate driver, 345,600bytes GRAM for graphic data of 320RGBx480 dots, and power supply circuit.

The ILI9486 supports parallel CPU 8-/9-/16-/18-bit data bus interface and 3-/4-line serial peripheral interfaces (SPI). The ILI9486 is also compliant with RGB (16-/18-bit) data bus for video image display. For high speed serial interface, the ILI9486 also provides one data and clock lane and supports up to 500Mbps on MIPI DSI link. And also support MDDI interface.

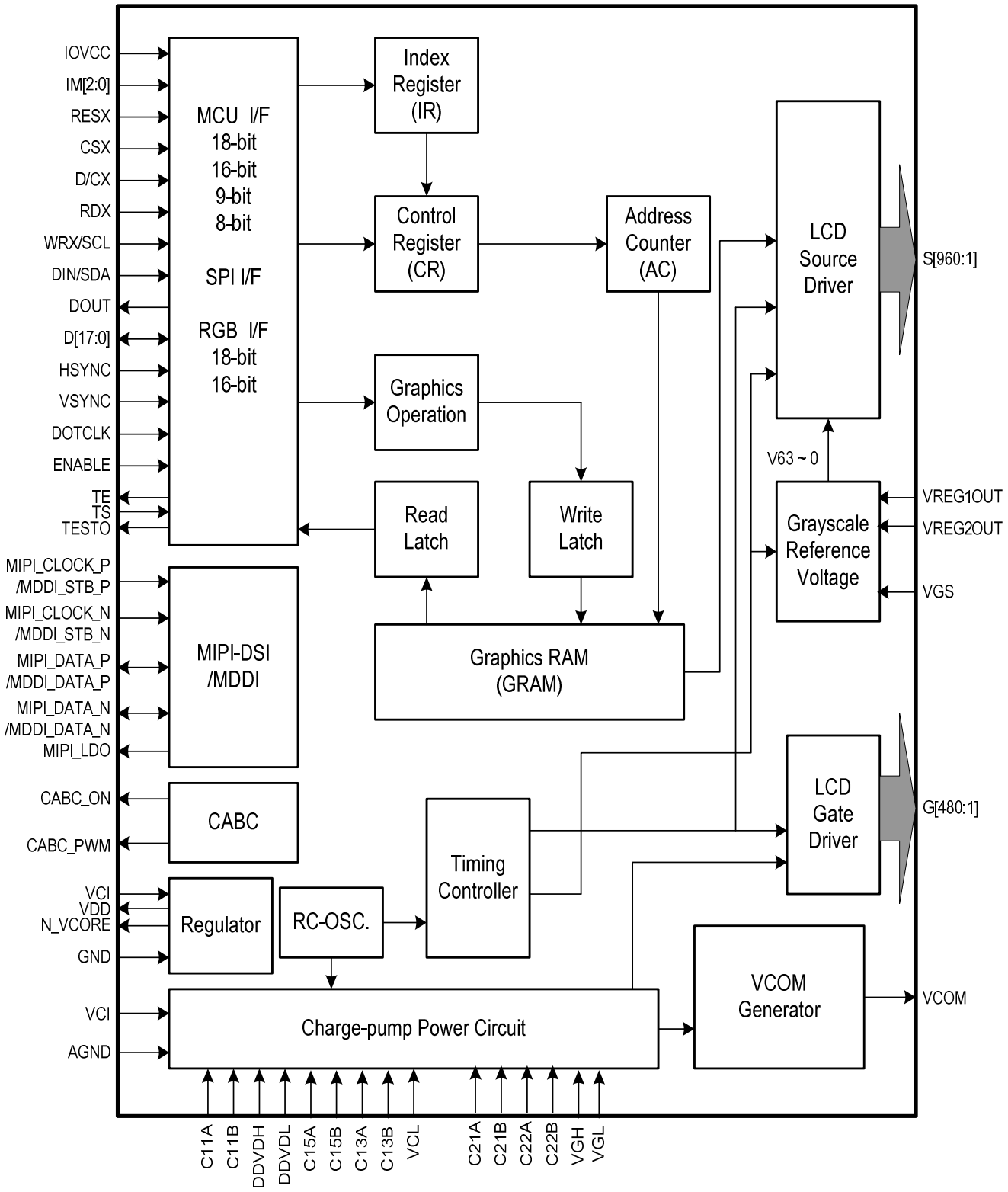
ILI9486 can operate with 1.65V I/O interface voltage and support wide analog power supply range. The ILI9486 also supports a function to display in 8 colors and a sleep mode, allowing for precise power control by software and these features make the ILI9486 as an ideal LCD driver for medium or small size portable products such as digital cellular phones, smart phone, MP3 and PMP where long battery life is a major concern.

2. Features

- Display resolution: [320xRGB](H) x 480(V)
- Output:
  - 960 source outputs
  - 480 gate outputs
  - Common electrode output
- a-TFT LCD driver with on-chip full display RAM: 345,600 bytes
- Interface
  - 8-bits, 9-bits, 16-bts, 18-bits interface with 8080-series MCU
  - 16-bits, 18-bits RGB interface with graphic controller
  - 3-line / 4-line serial interface
  - MIPI DSI (DSI v1.01r11, D-PHY v1.0), one lane 500Mbps.
  - MDDI (Mobile Display Digital Interface), one lane 400Mbps, support VESA V1.0/V1.2.
- Display mode:
  - Full color mode (Idle mode OFF) : 262K-colors, 65K-colors.
  - Reduce color mode (Idle mode ON) : 8-color.
- Power saving mode:
  - Deep-standby mode
  - Sleep mode
- On chip functions:
  - DC VCOM generator and adjustment
  - Timing generator
  - Oscillator
  - DC/DC converter
  - Dot/Column/Z inversion
  - Separate RGB Gamma correction
  - CABC(Content adaptive brightness control)
- MTP (4 times):
  - 8-bits for ID1
  - 8-bits for ID2
  - 8-bits for ID3
  - 7-bits for VCOM adjustment

- Low -power consumption architecture
  - Low operating power supplies:
    - IOVCC = 1.65V ~ 3.6V (Digital)
    - VCI = 2.5V ~ 3.6V (Analog)
- LCD Voltage drive:
  - Source/VCOM power supply voltage
    - DDVDH - GND = 4.5V ~ 6.0V
    - VCL - GND = -2.0~-3.0V
    - VCI1 - VCL 6.0V
  - Gate driver output voltage
    - VGH - GND = 10.0V ~ 20.0V
    - VGL - GND = -5.0V ~ -15.0V
    - VGH - VGL 32.0V
  - VCOM driver output voltage
    - VCOM = 0~2.0V
- Operate temperature range: -40℃ to 85℃
- a-Si TFT LCD storage capacitor : Cst on Common structure only

3. Block Diagram



4. Pin Descriptions

<table>
<tr><th colspan="4">Bus Interface Pins</th></tr>
<tr><th>Pin Name</th><th>I/O</th><th>Type</th><th>Descriptions</th></tr>
<tr><td>IM2,IM1,IM0</td><td>I</td><td>MPU
IOVCC/DGND</td><td>- Select the interface mode
<table>
<tr><th>IM2</th><th>IM1</th><th>IM0</th><th>Interface</th><th>Data Pin in Use</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>8080 18-bit bus interface</td><td>DB[17:0]</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>8080 9-bit bus interface</td><td>DB[8:0]</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>8080 16-bit bus interface</td><td>DB[15:0]</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>8080 8-bit bus interface</td><td>DB[7:0]</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>MDDI</td><td>MDDI_DATA_P
MDDI_DATA_N
MDDI_STB_P
MDDI_STB_N</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>3-line SPI</td><td>SDA</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>MIPI DSI</td><td>MIPI_DATA_P,
MIPI_DATA_N
MIPI_CLOCK_P
MIPI_CLOCK_N</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>4-line SPI</td><td>SDA</td></tr>
</table></td></tr>
<tr><td>RESX</td><td>I</td><td>MPU/
Reset circuit</td><td>- The external reset input.
- Initializes the chip with a low input. Be sure to execute a power-on reset after supplying power.</td></tr>
<tr><td>CSX</td><td>I</td><td>MPU</td><td>- A chip select signal.
Low: the chip is selected and accessible
High: the chip is not selected and not accessible
Fix to IOVCC or DGND level when not in use.</td></tr>
<tr><td>D/CX</td><td>I</td><td>MPU</td><td>- Parallel interface (D/CX): The signal for command or parameter select.
Low: Command.
High: Parameter.
Fix to IOVCC or DGND level when not in use.</td></tr>
<tr><td>WRX/SCL</td><td>I</td><td>MPU
IOVCC</td><td>- 8080 system (WRX): Serves as a write signal and writes data at the rising edge.
- 3/4-line serial interface (SCL): The pin used as serial clock pin.
Fix to IOVCC or DGND level when not in use.</td></tr>
<tr><td>RDX</td><td>I</td><td>MPU</td><td>- 8080 system (RDX): Serves as a read signal and read data at the rising edge.
Fix to IOVCC or DGND level when not in use.</td></tr>
<tr><td>DIN/SDA</td><td>I/O</td><td>MPU</td><td>- Serial data input / output.
Fix to IOVCC or DGND level when not in use.</td></tr>
<tr><td>DOUT</td><td>O</td><td>MCU</td><td>- Serial data output
Leave the pin to open when not in use.</td></tr>
<tr><td>TE</td><td>O</td><td>MPU</td><td>- Tearing effect output.
Leave the pin to open when not in use.</td></tr>
<tr><td>CABC_PWM</td><td>O</td><td>VCI</td><td>- Back light control pin.
Leave the pin to open when not in use.</td></tr>
<tr><td>CABC_ON</td><td>O</td><td>VCI</td><td>- Back light control pin.
Leave the pin to open when not in use.</td></tr>
<tr><td>MIPI_CLOCK_P
/MDDI_STB_P</td><td>I</td><td>MIPI</td><td>- Positive polarity of low voltage differential clock signal</td></tr>
<tr><td>MIPI_CLOCK_N
/MDDI_STB_N</td><td>I</td><td>MIPI</td><td>- Negative polarity of low voltage differential clock signal</td></tr>
</table>

<table>
<tr><td>MIPI_DATA_P
/MDDI_DATA_P</td><td>I/O</td><td>MIPI</td><td>- Positive polarity of low voltage differential data signal</td></tr>
<tr><td>MIPI_DATA_N
MDDI_DATA_N</td><td>I/O</td><td>MIPI</td><td>- Negative polarity of low voltage differential data signal</td></tr>
<tr><td>DB[17:0]</td><td>I/O</td><td>MPU</td><td>- A 18-bit parallel bi-directional data bus for MCU system
<table>
<tr><th>Interface Mode</th><th>Data Pin in Use</th></tr>
<tr><td>8-bit MCU System Interface Mode</td><td>DB[7:0]</td></tr>
<tr><td>9-bit MCU System Interface Mode</td><td>DB[8:0]</td></tr>
<tr><td>16-bit MCU System Interface Mode</td><td>DB[15:0]</td></tr>
<tr><td>18-bit MCU System Interface Mode</td><td>DB[17:0]</td></tr>
<tr><td>16-bit RGB Interface Mode</td><td>DB[15:0]</td></tr>
<tr><td>18-bit RGB Interface Mode</td><td>DB[17:0]</td></tr>
</table>
Fix to DGND level when not in use.</td></tr>
<tr><td>VSYNC</td><td>I</td><td>MPU</td><td>- Frame synchronizing signal for RGB interface operation.
Fix to DGND level when not in use.</td></tr>
<tr><td>HSYNC</td><td>I</td><td>MPU</td><td>- Line synchronizing signal for RGB interface operation.
Fix to DGND level when not in use.</td></tr>
<tr><td>ENABLE</td><td>I</td><td>MPU</td><td>- Data enable signal for RGB interface operation.
Low : access enabled.
High : access inhibited.
Fix to DGND level when not in use.</td></tr>
<tr><td>DOTCLK</td><td>I</td><td>MPU</td><td>- Dot clock signal for RGB interface operation.
Fix to IOVCC level when not in use.</td></tr>
</table>

LCD Driving Signals			
Pin Name	I/O	Type	Descriptions
S961~S1	O	LCD	- Source output voltage signals applied to liquid crystal. ***Leave the pin to open when not in use.***
G480~G1	O	LCD	- Gate line output signals. VGH: the level selecting gate lines VGL: the level not selecting gate lines ***Leave the pin to open when not in use.***
VCOM	O	-	- The power supply of common voltage in DC VCOM driving. - The voltage range is set between -2V to 0V.
VREG1OUT	O	-	- Internal generated stable power for source driver unit. - The voltage level can be set by VRH1[4:0]. - VREG1OUT is a positive grayscale reference voltage of source driver. - VREG1OUT =3.6~5.5V
VREG2OUT	O	-	- Internal generated stable power for source driver unit. - The voltage level can be set by VRH2[4:0]. - VREG2OUT is a negative grayscale reference voltage of source driver. - VREG2OUT =-3.6~-5.5V
VGS	I	-	Reference level for grayscale generating circuit.

Charge-pump and Regulator Circuit			
Pin Name	I/O	Type	Descriptions
VCI	P	Power supply	- A supply voltage to the analog circuit. Connect to an external power supply of 2.5 ~ 3.6V.
DDVDH	O	Stabilizing capacitor	- Power supply for the source driver and VCOM driver. - Connect to a stabilizing capacitor between DDVDH and GND.
DDVDL	O	Stabilizing capacitor	- Power supply for the source driver and VCOM driver. - Connect to a stabilizing capacitor between DDVDL and

			GND.
VGH	O	Stabilizing capacitor	- Power supply for the gate driver. - Connect to a stabilizing capacitor between VGH and GND.
VGL	O	Stabilizing capacitor	- Power supply for the gate driver. . - Connect to a stabilizing capacitor between VGL and GND.
VCL	O	Stabilizing capacitor	- VCOML driver power supply. - VCL = 0.5 ~ -VCI, place a stabilizing capacitor between VCL and GND.
C11A, C11B C15A, C15B	O	Step-up capacitor	- Capacitor connection pins for the step-up circuit 1
C13A, C13B C21A, C21B C22A, C22B	O	Step-up capacitor	- Capacitor connection pins for the step-up circuit 2.

Power Pads			
Pin Name	I/O	Type	Descriptions
IOVCC	P	Power supply	- A supply voltage to the digital circuit. Connect to an external power supply of 1.65 ~ 3.6V.
VDD	O	Power	- Digital circuit power pad. Connect these pins with the 1uF capacitor.
N_VCORE	O	Power	- Digital circuit negative power pad. Connect these pins with the 1uF capacitor.
DGND	P	Power supply	- DGND for the digital side: DGND = 0V. In case of COG, connect to GND on the FPC to prevent noise.
AGND	P	Power supply	- AGND for the analog side: AGND = 0V. In case of COG, connect to GND on the FPC to prevent noise.
VPG	P	Power supply	- Power supply pin for the NV memory programming. Please provide 7 volt to this pin for NV memory programming.
MIPI_LDO	P	Stabilizing capacitor	- MIPI core power pad. - Connect to a stabilizing capacitor between MIPI_LDO and GND.

Test Pads			
Pin Name	I/O	Type	Descriptions
DUMMY	-	-	-- Dummy pad. ***Leave the pin to be open when not in use.***
TS[2:0]	I	IOGND	- Test pins These pins are internal pulled low. Please leave these pins as open.
TEST[5:0] CABC_ON/TEST6 CABC_PWM/TEST7	O	-	-TEST[7:0]: When set in test mode, the pin are test pins. -CABC_ON: In normal mode, it's a LED driver control pin which Used for turning ON/OFF LED backlight. -CABC_PWM: In normal mode the PWM frequency output for LED driver control. ***Leave these pins to be open when not in use.***
V1T V62T VWT	I	-	- Test pins. ***Leave these pins to be open when not in use.***

Liquid crystal power supply specifications Table

No.	Item		Description
1	TFT Source Driver		960 pins (320 x RGB)
2	TFT Gate Driver		480 pins
3	TFT Display's Capacitor Structure		Cst structure only (Cs on Common)
4	Liquid Crystal Drive Output	S1 ~ S960	V0 ~ V63 grayscales
		G1 ~ G480	VGH – VGL
		VCOM	0~-2.0V
5	Input Voltage	IOVCC	1.65 ~ 3.60V
		VCI	2.50 ~ 3.60V
6	Liquid Crystal Drive Voltages	DDVDH	4.5V ~ 6.5V
		DDVDL	-6.5V ~ -4.5V
		VGH	10.0V ~ 20.0V
		VGL	-5.0V ~ -15.0V
		VCL	-1.9 ~ -3.0V
		VGH – VGL	Max. 32.0V
7	Internal Step-up Circuits	DDVDH	VCI1 X2
		DDVDL	-(VCI1-VCL)
		VGH	VCI1 x4, x5, x6
		VGL	VCI1 x-3, x-4, x-5
		VCL	VCI1 x-1

5. Pad Arrangement and Coordination

Chip Size: 22850um x 850um

Chip thickness : 280um (typ.)

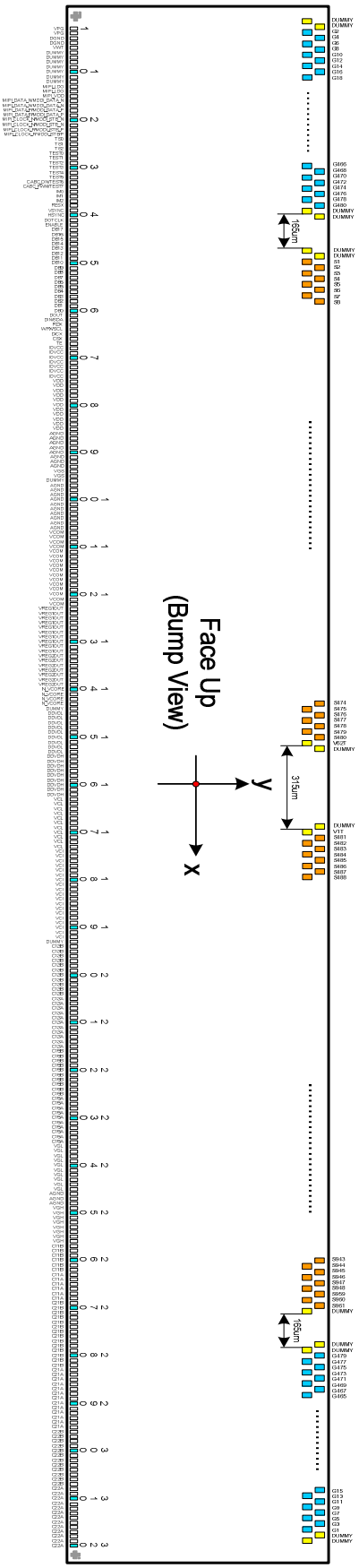
Pad Location: Pad Center.

Coordinate Origin: Chip center

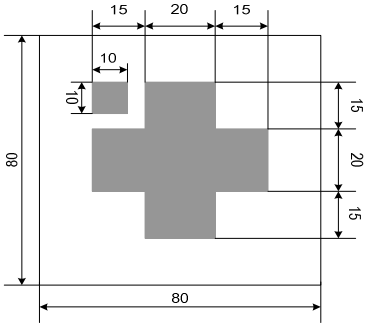
Au bump height: 15um (typ.)

Au Bump Size:

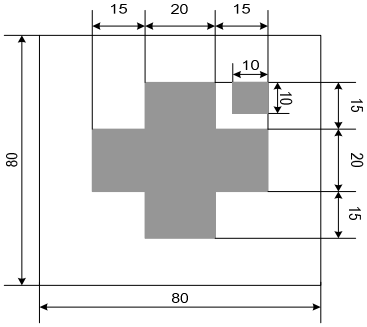
1. 15um x 110um
   Gate: G1 ~ G480
   Source: S1 ~ S961
2. 50um x 70um
   Input Pads
   Pad 1 to 320.



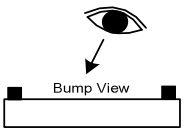
Alignment Marks



Alignment Mark: Left



Alignment Mark: Right



No.	Name	X	Y	No.	Name	X	Y	No.	Name	X	Y	No.	Name	X	Y	No.	Name	X	Y
1	VPG	-11165	-279	51	DB9	-7665	-279	101	AGND	-4165	-279	151	DDVDL	-665	-279	201	C13B	2835	-279
2	VPG	-11095	-279	52	DB8	-7595	-279	102	AGND	-4095	-279	152	DDVDL	-595	-279	202	C13B	2905	-279
3	DGND	-11025	-279	53	DB7	-7525	-279	103	AGND	-4025	-279	153	DDVDL	-525	-279	203	C13B	2975	-279
4	DGND	-10955	-279	54	DB6	-7455	-279	104	AGND	-3955	-279	154	DDVDH	-455	-279	204	C13B	3045	-279
5	VWT	-10885	-279	55	DB5	-7385	-279	105	AGND	-3885	-279	155	DDVDH	-385	-279	205	C13A	3115	-279
6	DUMMY	-10815	-279	56	DB4	-7315	-279	106	AGND	-3815	-279	156	DDVDH	-315	-279	206	C13A	3185	-279
7	DUMMY	-10745	-279	57	DB3	-7245	-279	107	VCOM	-3745	-279	157	DDVDH	-245	-279	207	C13A	3255	-279
8	DUMMY	-10675	-279	58	DB2	-7175	-279	108	VCOM	-3675	-279	158	DDVDH	-175	-279	208	C13A	3325	-279
9	DUMMY	-10605	-279	59	DB1	-7105	-279	109	VCOM	-3605	-279	159	DDVDH	-105	-279	209	C13A	3395	-279
10	DUMMY	-10535	-279	60	DB0	-7035	-279	110	VCOM	-3535	-279	160	DDVDH	-35	-279	210	C13A	3465	-279
11	DUMMY	-10465	-279	61	DOUT	-6965	-279	111	VCOM	-3465	-279	161	DDVDH	35	-279	211	C13A	3535	-279
12	DUMMY	-10395	-279	62	DIN/SDA	-6895	-279	112	VCOM	-3395	-279	162	DDVDH	105	-279	212	C13A	3605	-279
13	MIPI_LDO	-10325	-279	63	RDX	-6825	-279	113	VCOM	-3325	-279	163	VCL	175	-279	213	C13A	3675	-279
14	MIPI_LDO	-10255	-279	64	WRX/SCL	-6755	-279	114	VCOM	-3255	-279	164	VCL	245	-279	214	C13A	3745	-279
15	MIPI_VDD	-10185	-279	65	D/CX	-6685	-279	115	VCOM	-3185	-279	165	VCL	315	-279	215	C13A	3815	-279
16	MIPI_DATA_N/MDDI_DATA_N	-10115	-279	66	CSX	-6615	-279	116	VCOM	-3115	-279	166	VCL	385	-279	216	C15B	3885	-279
17	MIPI_DATA_N/MDDI_DATA_N	-10045	-279	67	TE	-6545	-279	117	VCOM	-3045	-279	167	VCL	455	-279	217	C15B	3955	-279
18	MIPI_DATA_P/MDDI_DATA_P	-9975	-279	68	IOVCC	-6475	-279	118	VCOM	-2975	-279	168	VCL	525	-279	218	C15B	4025	-279
19	MIPI_DATA_P/MDDI_DATA_P	-9905	-279	69	IOVCC	-6405	-279	119	VCOM	-2905	-279	169	VCL	595	-279	219	C15B	4095	-279
20	MIPI_CLOCK_N/MDDI_STB_N	-9835	-279	70	IOVCC	-6335	-279	120	VCOM	-2835	-279	170	VCL	665	-279	220	C15B	4165	-279
21	MIPI_CLOCK_N/MDDI_STB_N	-9765	-279	71	IOVCC	-6265	-279	121	VCOM	-2765	-279	171	VCL	735	-279	221	C15B	4235	-279
22	MIPI_CLOCK_P/MDDI_STB_P	-9695	-279	72	IOVCC	-6195	-279	122	VCOM	-2695	-279	172	VCL	805	-279	222	C15B	4305	-279
23	MIPI_CLOCK_P/MDDI_STB_P	-9625	-279	73	IOVCC	-6125	-279	123	VREG1OUT	-2625	-279	173	VCL	875	-279	223	C15B	4375	-279
24	TS0	-9555	-279	74	IOVCC	-6055	-279	124	VREG1OUT	-2555	-279	174	VCI	945	-279	224	C15B	4445	-279
25	TS1	-9485	-279	75	VDD	-5985	-279	125	VREG1OUT	-2485	-279	175	VCI	1015	-279	225	C15B	4515	-279
26	TS2	-9415	-279	76	VDD	-5915	-279	126	VREG1OUT	-2415	-279	176	VCI	1085	-279	226	C15A	4585	-279
27	TEST0	-9345	-279	77	VDD	-5845	-279	127	VREG1OUT	-2345	-279	177	VCI	1155	-279	227	C15A	4655	-279
28	TEST1	-9275	-279	78	VDD	-5775	-279	128	VREG1OUT	-2275	-279	178	VCI	1225	-279	228	C15A	4725	-279
29	TEST2	-9205	-279	79	VDD	-5705	-279	129	VREG1OUT	-2205	-279	179	VCI	1295	-279	229	C15A	4795	-279
30	TEST3	-9135	-279	80	VDD	-5635	-279	130	VREG1OUT	-2135	-279	180	VCI	1365	-279	230	C15A	4865	-279
31	TEST4	-9065	-279	81	VDD	-5565	-279	131	VREG1OUT	-2065	-279	181	VCI	1435	-279	231	C15A	4935	-279
32	TEST5	-8995	-279	82	VDD	-5495	-279	132	VREG1OUT	-1995	-279	182	VCI	1505	-279	232	C15A	5005	-279
33	CABC_ON/TEST6	-8925	-279	83	VDD	-5425	-279	133	VREG2OUT	-1925	-279	183	VCI	1575	-279	233	C15A	5075	-279
34	CABC_PWM/TEST7	-8855	-279	84	VDD	-5355	-279	134	VREG2OUT	-1855	-279	184	VCI	1645	-279	234	C15A	5145	-279
35	IM0/ID	-8785	-279	85	VDD	-5285	-279	135	VREG2OUT	-1785	-279	185	VCI	1715	-279	235	C15A	5215	-279
36	IM1	-8715	-279	86	AGND	-5215	-279	136	VREG2OUT	-1715	-279	186	VCI	1785	-279	236	VGL	5285	-279
37	IM2	-8645	-279	87	AGND	-5145	-279	137	VREG2OUT	-1645	-279	187	VCI	1855	-279	237	VGL	5355	-279
38	RESX	-8575	-279	88	AGND	-5075	-279	138	VREG2OUT	-1575	-279	188	VCI	1925	-279	238	VGL	5425	-279
39	VSYNC	-8505	-279	89	AGND	-5005	-279	139	VREG2OUT	-1505	-279	189	VCI	1995	-279	239	VGL	5495	-279
40	HSYNC	-8435	-279	90	AGND	-4935	-279	140	N_VCORE	-1435	-279	190	VCI	2065	-279	240	VGL	5565	-279
41	DOTCLK	-8365	-279	91	AGND	-4865	-279	141	N_VCORE	-1365	-279	191	VCI	2135	-279	241	VGL	5635	-279
42	ENABLE	-8295	-279	92	AGND	-4795	-279	142	N_VCORE	-1295	-279	192	VCI	2205	-279	242	VGL	5705	-279
43	DB17	-8225	-279	93	AGND	-4725	-279	143	N_VCORE	-1225	-279	193	DUMMY	2275	-279	243	VGL	5775	-279
44	DB16	-8155	-279	94	VGS	-4655	-279	144	DUMMY	-1155	-279	194	C13B	2345	-279	244	VGL	5845	-279
45	DB15	-8085	-279	95	VGS	-4585	-279	145	DDVDL	-1085	-279	195	C13B	2415	-279	245	VGL	5915	-279
46	DB14	-8015	-279	96	DUMMY	-4515	-279	146	DDVDL	-1015	-279	196	C13B	2485	-279	246	AGND	5985	-279
47	DB13	-7945	-279	97	AGND	-4445	-279	147	DDVDL	-945	-279	197	C13B	2555	-279	247	AGND	6055	-279
48	DB12	-7875	-279	98	AGND	-4375	-279	148	DDVDL	-875	-279	198	C13B	2625	-279	248	AGND	6125	-279
49	DB11	-7805	-279	99	AGND	-4305	-279	149	DDVDL	-805	-279	199	C13B	2695	-279	249	VGH	6195	-279
50	DB10	-7735	-279	100	AGND	-4235	-279	150	DDVDL	-735	-279	200	C13B	2765	-279	250	VGH	6265	-279

No.	Name	X	Y
251	VGH	6335	-279
252	VGH	6405	-279
253	VGH	6475	-279
254	VGH	6545	-279
255	VGH	6615	-279
256	VGH	6685	-279
257	C11B	6755	-279
258	C11B	6825	-279
259	C11B	6895	-279
260	C11B	6965	-279
261	C11B	7035	-279
262	C11B	7105	-279
263	C11A	7175	-279
264	C11A	7245	-279
265	C11A	7315	-279
266	C11A	7385	-279
267	C11A	7455	-279
268	C11A	7525	-279
269	C21B	7595	-279
270	C21B	7665	-279
271	C21B	7735	-279
272	C21B	7805	-279
273	C21B	7875	-279
274	C21B	7945	-279
275	C21B	8015	-279
276	C21B	8085	-279
277	C21B	8155	-279
278	C21B	8225	-279
279	C21B	8295	-279
280	C21B	8365	-279
281	C21B	8435	-279
282	C21B	8505	-279
283	C21A	8575	-279
284	C21A	8645	-279
285	C21A	8715	-279
286	C21A	8785	-279
287	C21A	8855	-279
288	C21A	8925	-279
289	C21A	8995	-279
290	C21A	9065	-279
291	C21A	9135	-279
292	C21A	9205	-279
293	C21A	9275	-279
294	C21A	9345	-279
295	C21A	9415	-279
296	C22B	9486	-279
297	C22B	9555	-279
298	C22B	9625	-279
299	C22B	9695	-279
300	C22B	9765	-279

No.	Name	X	Y
301	C22B	9835	-279
302	C22B	9905	-279
303	C22B	9975	-279
304	C22B	10045	-279
305	C22B	10115	-279
306	C22B	10185	-279
307	C22B	10255	-279
308	C22A	10325	-279
309	C22A	10395	-279
310	C22A	10465	-279
311	C22A	10535	-279
312	C22A	10605	-279
313	C22A	10675	-279
314	C22A	10745	-279
315	C22A	10815	-279
316	C22A	10885	-279
317	C22A	10955	-279
318	C22A	11025	-279
319	C22A	11095	-279
320	C22A	11165	-279
321	DUMMY	11205	154
322	DUMMY	11190	299
323	G1	11175	154
324	G3	11160	299
325	G5	11145	154
326	G7	11130	299
327	G9	11115	154
328	G11	11100	299
329	G13	11085	154
330	G15	11070	299
331	G17	11055	154
332	G19	11040	299
333	G21	11025	154
334	G23	11010	299
335	G25	10995	154
336	G27	10980	299
337	G29	10965	154
338	G31	10950	299
339	G33	10935	154
340	G35	10920	299
341	G37	10905	154
342	G39	10890	299
343	G41	10875	154
344	G43	10860	299
345	G45	10845	154
346	G47	10830	299
347	G49	10815	154
348	G51	10800	299
349	G53	10785	154
350	G55	10770	299

No.	Name	X	Y
351	G57	10755	154
352	G59	10740	299
353	G61	10725	154
354	G63	10710	299
355	G65	10695	154
356	G67	10680	299
357	G69	10665	154
358	G71	10650	299
359	G73	10635	154
360	G75	10620	299
361	G77	10605	154
362	G79	10590	299
363	G81	10575	154
364	G83	10560	299
365	G85	10545	154
366	G87	10530	299
367	G89	10515	154
368	G91	10500	299
369	G93	10485	154
370	G95	10470	299
371	G97	10455	154
372	G99	10440	299
373	G101	10425	154
374	G103	10410	299
375	G105	10395	154
376	G107	10380	299
377	G109	10365	154
378	G111	10350	299
379	G113	10335	154
380	G115	10320	299
381	G117	10305	154
382	G119	10290	299
383	G121	10275	154
384	G123	10260	299
385	G125	10245	154
386	G127	10230	299
387	G129	10215	154
388	G131	10200	299
389	G133	10185	154
390	G135	10170	299
391	G137	10155	154
392	G139	10140	299
393	G141	10125	154
394	G143	10110	299
395	G145	10095	154
396	G147	10080	299
397	G149	10065	154
398	G151	10050	299
399	G153	10035	154
400	G155	10020	299

No.	Name	X	Y
401	G157	10005	154
402	G159	9990	299
403	G161	9975	154
404	G163	9960	299
405	G165	9945	154
406	G167	9930	299
407	G169	9915	154
408	G171	9900	299
409	G173	9885	154
410	G175	9870	299
411	G177	9855	154
412	G179	9840	299
413	G181	9825	154
414	G183	9810	299
415	G185	9795	154
416	G187	9780	299
417	G189	9765	154
418	G191	9750	299
419	G193	9735	154
420	G195	9720	299
421	G197	9705	154
422	G199	9690	299
423	G201	9675	154
424	G203	9660	299
425	G205	9645	154
426	G207	9630	299
427	G209	9615	154
428	G211	9600	299
429	G213	9585	154
430	G215	9570	299
431	G217	9555	154
432	G219	9540	299
433	G221	9525	154
434	G223	9510	299
435	G225	9495	154
436	G227	9480	299
437	G229	9465	154
438	G231	9450	299
439	G233	9435	154
440	G235	9420	299
441	G237	9405	154
442	G239	9390	299
443	G241	9375	154
444	G243	9360	299
445	G245	9345	154
446	G247	9330	299
447	G249	9315	154
448	G251	9300	299
449	G253	9285	154
450	G255	9270	299

No.	Name	X	Y
451	G257	9255	154
452	G259	9240	299
453	G261	9225	154
454	G263	9210	299
455	G265	9195	154
456	G267	9180	299
457	G269	9165	154
458	G271	9150	299
459	G273	9135	154
460	G275	9120	299
461	G277	9105	154
462	G279	9090	299
463	G281	9075	154
464	G283	9060	299
465	G285	9045	154
466	G287	9030	299
467	G289	9015	154
468	G291	9000	299
469	G293	8985	154
470	G295	8970	299
471	G297	8955	154
472	G299	8940	299
473	G301	8925	154
474	G303	8910	299
475	G305	8895	154
476	G307	8880	299
477	G309	8865	154
478	G311	8850	299
479	G313	8835	154
480	G315	8820	299
481	G317	8805	154
482	G319	8790	299
483	G321	8775	154
484	G323	8760	299
485	G325	8745	154
486	G327	8730	299
487	G329	8715	154
488	G331	8700	299
489	G333	8685	154
490	G335	8670	299
491	G337	8655	154
492	G339	8640	299
493	G341	8625	154
494	G343	8610	299
495	G345	8595	154
496	G347	8580	299
497	G349	8565	154
498	G351	8550	299
499	G353	8535	154
500	G355	8520	299

No.	Name	X	Y
501	G357	8505	154
502	G359	8490	299
503	G361	8475	154
504	G363	8460	299
505	G365	8445	154
506	G367	8430	299
507	G369	8415	154
508	G371	8400	299
509	G373	8385	154
510	G375	8370	299
511	G377	8355	154
512	G379	8340	299
513	G381	8325	154
514	G383	8310	299
515	G385	8295	154
516	G387	8280	299
517	G389	8265	154
518	G391	8250	299
519	G393	8235	154
520	G395	8220	299
521	G397	8205	154
522	G399	8190	299
523	G401	8175	154
524	G403	8160	299
525	G405	8145	154
526	G407	8130	299
527	G409	8115	154
528	G411	8100	299
529	G413	8085	154
530	G415	8070	299
531	G417	8055	154
532	G419	8040	299
533	G421	8025	154
534	G423	8010	299
535	G425	7995	154
536	G427	7980	299
537	G429	7965	154
538	G431	7950	299
539	G433	7935	154
540	G435	7920	299
541	G437	7905	154
542	G439	7890	299
543	G441	7875	154
544	G443	7860	299
545	G445	7845	154
546	G447	7830	299
547	G449	7815	154
548	G451	7800	299
549	G453	7785	154
550	G455	7770	299

No.	Name	X	Y
551	G457	7755	154
552	G459	7740	299
553	G461	7725	154
554	G463	7710	299
555	G465	7695	154
556	G467	7680	299
557	G469	7665	154
558	G471	7650	299
559	G473	7635	154
560	G475	7620	299
561	G477	7605	154
562	G479	7590	299
563	DUMMY	7575	154
564	DUMMY	7560	299
565	DUMMY	7395	154
566	S961	7380	299
567	S960	7365	154
568	S959	7350	299
569	S958	7335	154
570	S957	7320	299
571	S956	7305	154
572	S955	7290	299
573	S954	7275	154
574	S953	7260	299
575	S952	7245	154
576	S951	7230	299
577	S950	7215	154
578	S949	7200	299
579	S948	7185	154
580	S947	7170	299
581	S946	7155	154
582	S945	7140	299
583	S944	7125	154
584	S943	7110	299
585	S942	7095	154
586	S941	7080	299
587	S940	7065	154
588	S939	7050	299
589	S938	7035	154
590	S937	7020	299
591	S936	7005	154
592	S935	6990	299
593	S934	6975	154
594	S933	6960	299
595	S932	6945	154
596	S931	6930	299
597	S930	6915	154
598	S929	6900	299
599	S928	6885	154
600	S927	6870	299

No.	Name	X	Y
601	S926	6855	154
602	S925	6840	299
603	S924	6825	154
604	S923	6810	299
605	S922	6795	154
606	S921	6780	299
607	S920	6765	154
608	S919	6750	299
609	S918	6735	154
610	S917	6720	299
611	S916	6705	154
612	S915	6690	299
613	S914	6675	154
614	S913	6660	299
615	S912	6645	154
616	S911	6630	299
617	S910	6615	154
618	S909	6600	299
619	S908	6585	154
620	S907	6570	299
621	S906	6555	154
622	S905	6540	299
623	S904	6525	154
624	S903	6510	299
625	S902	6495	154
626	S901	6480	299
627	S900	6465	154
628	S899	6450	299
629	S898	6435	154
630	S897	6420	299
631	S896	6405	154
632	S895	6390	299
633	S894	6375	154
634	S893	6360	299
635	S892	6345	154
636	S891	6330	299
637	S890	6315	154
638	S889	6300	299
639	S888	6285	154
640	S887	6270	299
641	S886	6255	154
642	S885	6240	299
643	S884	6225	154
644	S883	6210	299
645	S882	6195	154
646	S881	6180	299
647	S880	6165	154
648	S879	6150	299
649	S878	6135	154
650	S877	6120	299

No.	Name	X	Y
651	S876	6105	154
652	S875	6090	299
653	S874	6075	154
654	S873	6060	299
655	S872	6045	154
656	S871	6030	299
657	S870	6015	154
658	S869	6000	299
659	S868	5985	154
660	S867	5970	299
661	S866	5955	154
662	S865	5940	299
663	S864	5925	154
664	S863	5910	299
665	S862	5895	154
666	S861	5880	299
667	S860	5865	154
668	S859	5850	299
669	S858	5835	154
670	S857	5820	299
671	S856	5805	154
672	S855	5790	299
673	S854	5775	154
674	S853	5760	299
675	S852	5745	154
676	S851	5730	299
677	S850	5715	154
678	S849	5700	299
679	S848	5685	154
680	S847	5670	299
681	S846	5655	154
682	S845	5640	299
683	S844	5625	154
684	S843	5610	299
685	S842	5595	154
686	S841	5580	299
687	S840	5565	154
688	S839	5550	299
689	S838	5535	154
690	S837	5520	299
691	S836	5505	154
692	S835	5490	299
693	S834	5475	154
694	S833	5460	299
695	S832	5445	154
696	S831	5430	299
697	S830	5415	154
698	S829	5400	299
699	S828	5385	154
700	S827	5370	299

No.	Name	X	Y
701	S826	5355	154
702	S825	5340	299
703	S824	5325	154
704	S823	5310	299
705	S822	5295	154
706	S821	5280	299
707	S820	5265	154
708	S819	5250	299
709	S818	5235	154
710	S817	5220	299
711	S816	5205	154
712	S815	5190	299
713	S814	5175	154
714	S813	5160	299
715	S812	5145	154
716	S811	5130	299
717	S810	5115	154
718	S809	5100	299
719	S808	5085	154
720	S807	5070	299
721	S806	5055	154
722	S805	5040	299
723	S804	5025	154
724	S803	5010	299
725	S802	4995	154
726	S801	4980	299
727	S800	4965	154
728	S799	4950	299
729	S798	4935	154
730	S797	4920	299
731	S796	4905	154
732	S795	4890	299
733	S794	4875	154
734	S793	4860	299
735	S792	4845	154
736	S791	4830	299
737	S790	4815	154
738	S789	4800	299
739	S788	4785	154
740	S787	4770	299
741	S786	4755	154
742	S785	4740	299
743	S784	4725	154
744	S783	4710	299
745	S782	4695	154
746	S781	4680	299
747	S780	4665	154
748	S779	4650	299
749	S778	4635	154
750	S777	4620	299

No.	Name	X	Y
751	S776	4605	154
752	S775	4590	299
753	S774	4575	154
754	S773	4560	299
755	S772	4545	154
756	S771	4530	299
757	S770	4515	154
758	S769	4500	299
759	S768	4485	154
760	S767	4470	299
761	S766	4455	154
762	S765	4440	299
763	S764	4425	154
764	S763	4410	299
765	S762	4395	154
766	S761	4380	299
767	S760	4365	154
768	S759	4350	299
769	S758	4335	154
770	S757	4320	299
771	S756	4305	154
772	S755	4290	299
773	S754	4275	154
774	S753	4260	299
775	S752	4245	154
776	S751	4230	299
777	S750	4215	154
778	S749	4200	299
779	S748	4185	154
780	S747	4170	299
781	S746	4155	154
782	S745	4140	299
783	S744	4125	154
784	S743	4110	299
785	S742	4095	154
786	S741	4080	299
787	S740	4065	154
788	S739	4050	299
789	S738	4035	154
790	S737	4020	299
791	S736	4005	154
792	S735	3990	299
793	S734	3975	154
794	S733	3960	299
795	S732	3945	154
796	S731	3930	299
797	S730	3915	154
798	S729	3900	299
799	S728	3885	154
800	S727	3870	299

No.	Name	X	Y
801	S726	3855	154
802	S725	3840	299
803	S724	3825	154
804	S723	3810	299
805	S722	3795	154
806	S721	3780	299
807	S720	3765	154
808	S719	3750	299
809	S718	3735	154
810	S717	3720	299
811	S716	3705	154
812	S715	3690	299
813	S714	3675	154
814	S713	3660	299
815	S712	3645	154
816	S711	3630	299
817	S710	3615	154
818	S709	3600	299
819	S708	3585	154
820	S707	3570	299
821	S706	3555	154
822	S705	3540	299
823	S704	3525	154
824	S703	3510	299
825	S702	3495	154
826	S701	3480	299
827	S700	3465	154
828	S699	3450	299
829	S698	3435	154
830	S697	3420	299
831	S696	3405	154
832	S695	3390	299
833	S694	3375	154
834	S693	3360	299
835	S692	3345	154
836	S691	3330	299
837	S690	3315	154
838	S689	3300	299
839	S688	3285	154
840	S687	3270	299
841	S686	3255	154
842	S685	3240	299
843	S684	3225	154
844	S683	3210	299
845	S682	3195	154
846	S681	3180	299
847	S680	3165	154
848	S679	3150	299
849	S678	3135	154
850	S677	3120	299

No.	Name	X	Y
851	S676	3105	154
852	S675	3090	299
853	S674	3075	154
854	S673	3060	299
855	S672	3045	154
856	S671	3030	299
857	S670	3015	154
858	S669	3000	299
859	S668	2985	154
860	S667	2970	299
861	S666	2955	154
862	S665	2940	299
863	S664	2925	154
864	S663	2910	299
865	S662	2895	154
866	S661	2880	299
867	S660	2865	154
868	S659	2850	299
869	S658	2835	154
870	S657	2820	299
871	S656	2805	154
872	S655	2790	299
873	S654	2775	154
874	S653	2760	299
875	S652	2745	154
876	S651	2730	299
877	S650	2715	154
878	S649	2700	299
879	S648	2685	154
880	S647	2670	299
881	S646	2655	154
882	S645	2640	299
883	S644	2625	154
884	S643	2610	299
885	S642	2595	154
886	S641	2580	299
887	S640	2565	154
888	S639	2550	299
889	S638	2535	154
890	S637	2520	299
891	S636	2505	154
892	S635	2490	299
893	S634	2475	154
894	S633	2460	299
895	S632	2445	154
896	S631	2430	299
897	S630	2415	154
898	S629	2400	299
899	S628	2385	154
900	S627	2370	299

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904	S623	2310	299
905	S622	2295	154
906	S621	2280	299
907	S620	2265	154
908	S619	2250	299
909	S618	2235	154
910	S617	2220	299
911	S616	2205	154
912	S615	2190	299
913	S614	2175	154
914	S613	2160	299
915	S612	2145	154
916	S611	2130	299
917	S610	2115	154
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920	S607	2070	299
921	S606	2055	154
922	S605	2040	299
923	S604	2025	154
924	S603	2010	299
925	S602	1995	154
926	S601	1980	299
927	S600	1965	154
928	S599	1950	299
929	S598	1935	154
930	S597	1920	299
931	S596	1905	154
932	S595	1890	299
933	S594	1875	154
934	S593	1860	299
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936	S591	1830	299
937	S590	1815	154
938	S589	1800	299
939	S588	1785	154
940	S587	1770	299
941	S586	1755	154
942	S585	1740	299
943	S584	1725	154
944	S583	1710	299
945	S582	1695	154
946	S581	1680	299
947	S580	1665	154
948	S579	1650	299
949	S578	1635	154
950	S577	1620	299

No.	Name	X	Y
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956	S571	1530	299
957	S570	1515	154
958	S569	1500	299
959	S568	1485	154
960	S567	1470	299
961	S566	1455	154
962	S565	1440	299
963	S564	1425	154
964	S563	1410	299
965	S562	1395	154
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971	S556	1305	154
972	S555	1290	299
973	S554	1275	154
974	S553	1260	299
975	S552	1245	154
976	S551	1230	299
977	S550	1215	154
978	S549	1200	299
979	S548	1185	154
980	S547	1170	299
981	S546	1155	154
982	S545	1140	299
983	S544	1125	154
984	S543	1110	299
985	S542	1095	154
986	S541	1080	299
987	S540	1065	154
988	S539	1050	299
989	S538	1035	154
990	S537	1020	299
991	S536	1005	154
992	S535	990	299
993	S534	975	154
994	S533	960	299
995	S532	945	154
996	S531	930	299
997	S530	915	154
998	S529	900	299
999	S528	885	154
1000	S527	870	299

No.	Name	X	Y	No.	Name	X	Y	No.	Name	X	Y	No.	Name	X	Y	No.	Name	X	Y
1001	S526	855	154	1051	S480	-180	299	1101	S430	-930	299	1151	S380	-1680	299	1201	S330	-2430	299
1002	S525	840	299	1052	S479	-195	154	1102	S429	-945	154	1152	S379	-1695	154	1202	S329	-2445	154
1003	S524	825	154	1053	S478	-210	299	1103	S428	-960	299	1153	S378	-1710	299	1203	S328	-2460	299
1004	S523	810	299	1054	S477	-225	154	1104	S427	-975	154	1154	S377	-1725	154	1204	S327	-2475	154
1005	S522	795	154	1055	S476	-240	299	1105	S426	-990	299	1155	S376	-1740	299	1205	S326	-2490	299
1006	S521	780	299	1056	S475	-255	154	1106	S425	-1005	154	1156	S375	-1755	154	1206	S325	-2505	154
1007	S520	765	154	1057	S474	-270	299	1107	S424	-1020	299	1157	S374	-1770	299	1207	S324	-2520	299
1008	S519	750	299	1058	S473	-285	154	1108	S423	-1035	154	1158	S373	-1785	154	1208	S323	-2535	154
1009	S518	735	154	1059	S472	-300	299	1109	S422	-1050	299	1159	S372	-1800	299	1209	S322	-2550	299
1010	S517	720	299	1060	S471	-315	154	1110	S421	-1065	154	1160	S371	-1815	154	1210	S321	-2565	154
1011	S516	705	154	1061	S470	-330	299	1111	S420	-1080	299	1161	S370	-1830	299	1211	S320	-2580	299
1012	S515	690	299	1062	S469	-345	154	1112	S419	-1095	154	1162	S369	-1845	154	1212	S319	-2595	154
1013	S514	675	154	1063	S468	-360	299	1113	S418	-1110	299	1163	S368	-1860	299	1213	S318	-2610	299
1014	S513	660	299	1064	S467	-375	154	1114	S417	-1125	154	1164	S367	-1875	154	1214	S317	-2625	154
1015	S512	645	154	1065	S466	-390	299	1115	S416	-1140	299	1165	S366	-1890	299	1215	S316	-2640	299
1016	S511	630	299	1066	S465	-405	154	1116	S415	-1155	154	1166	S365	-1905	154	1216	S315	-2655	154
1017	S510	615	154	1067	S464	-420	299	1117	S414	-1170	299	1167	S364	-1920	299	1217	S314	-2670	299
1018	S509	600	299	1068	S463	-435	154	1118	S413	-1185	154	1168	S363	-1935	154	1218	S313	-2685	154
1019	S508	585	154	1069	S462	-450	299	1119	S412	-1200	299	1169	S362	-1950	299	1219	S312	-2700	299
1020	S507	570	299	1070	S461	-465	154	1120	S411	-1215	154	1170	S361	-1965	154	1220	S311	-2715	154
1021	S506	555	154	1071	S460	-480	299	1121	S410	-1230	299	1171	S360	-1980	299	1221	S310	-2730	299
1022	S505	540	299	1072	S459	-495	154	1122	S409	-1245	154	1172	S359	-1995	154	1222	S309	-2745	154
1023	S504	525	154	1073	S458	-510	299	1123	S408	-1260	299	1173	S358	-2010	299	1223	S308	-2760	299
1024	S503	510	299	1074	S457	-525	154	1124	S407	-1275	154	1174	S357	-2025	154	1224	S307	-2775	154
1025	S502	495	154	1075	S456	-540	299	1125	S406	-1290	299	1175	S356	-2040	299	1225	S306	-2790	299
1026	S501	480	299	1076	S455	-555	154	1126	S405	-1305	154	1176	S355	-2055	154	1226	S305	-2805	154
1027	S500	465	154	1077	S454	-570	299	1127	S404	-1320	299	1177	S354	-2070	299	1227	S304	-2820	299
1028	S499	450	299	1078	S453	-585	154	1128	S403	-1335	154	1178	S353	-2085	154	1228	S303	-2835	154
1029	S498	435	154	1079	S452	-600	299	1129	S402	-1350	299	1179	S352	-2100	299	1229	S302	-2850	299
1030	S497	420	299	1080	S451	-615	154	1130	S401	-1365	154	1180	S351	-2115	154	1230	S301	-2865	154
1031	S496	405	154	1081	S450	-630	299	1131	S400	-1380	299	1181	S350	-2130	299	1231	S300	-2880	299
1032	S495	390	299	1082	S449	-645	154	1132	S399	-1395	154	1182	S349	-2145	154	1232	S299	-2895	154
1033	S494	375	154	1083	S448	-660	299	1133	S398	-1410	299	1183	S348	-2160	299	1233	S298	-2910	299
1034	S493	360	299	1084	S447	-675	154	1134	S397	-1425	154	1184	S347	-2175	154	1234	S297	-2925	154
1035	S492	345	154	1085	S446	-690	299	1135	S396	-1440	299	1185	S346	-2190	299	1235	S296	-2940	299
1036	S491	330	299	1086	S445	-705	154	1136	S395	-1455	154	1186	S345	-2205	154	1236	S295	-2955	154
1037	S490	315	154	1087	S444	-720	299	1137	S394	-1470	299	1187	S344	-2220	299	1237	S294	-2970	299
1038	S489	300	299	1088	S443	-735	154	1138	S393	-1485	154	1188	S343	-2235	154	1238	S293	-2985	154
1039	S488	285	154	1089	S442	-750	299	1139	S392	-1500	299	1189	S342	-2250	299	1239	S292	-3000	299
1040	S487	270	299	1090	S441	-765	154	1140	S391	-1515	154	1190	S341	-2265	154	1240	S291	-3015	154
1041	S486	255	154	1091	S440	-780	299	1141	S390	-1530	299	1191	S340	-2280	299	1241	S290	-3030	299
1042	S485	240	299	1092	S439	-795	154	1142	S389	-1545	154	1192	S339	-2295	154	1242	S289	-3045	154
1043	S484	225	154	1093	S438	-810	299	1143	S388	-1560	299	1193	S338	-2310	299	1243	S288	-3060	299
1044	S483	210	299	1094	S437	-825	154	1144	S387	-1575	154	1194	S337	-2325	154	1244	S287	-3075	154
1045	S482	195	154	1095	S436	-840	299	1145	S386	-1590	299	1195	S336	-2340	299	1245	S286	-3090	299
1046	S481	180	299	1096	S435	-855	154	1146	S385	-1605	154	1196	S335	-2355	154	1246	S285	-3105	154
1047	V1T	165	154	1097	S434	-870	299	1147	S384	-1620	299	1197	S334	-2370	299	1247	S284	-3120	299
1048	DUMMY	150	299	1098	S433	-885	154	1148	S383	-1635	154	1198	S333	-2385	154	1248	S283	-3135	154
1049	DUMMY	-150	299	1099	S432	-900	299	1149	S382	-1650	299	1199	S332	-2400	299	1249	S282	-3150	299
1050	V62T	-165	154	1100	S431	-915	154	1150	S381	-1665	154	1200	S331	-2415	154	1250	S281	-3165	154

No.	Name	X	Y	No.	Name	X	Y	No.	Name	X	Y	No.	Name	X	Y	No.	Name	X	Y
1251	S280	-3180	299	1301	S230	-3930	299	1351	S180	-4680	299	1401	S130	-5430	299	1451	S80	-6180	299
1252	S279	-3195	154	1302	S229	-3945	154	1352	S179	-4695	154	1402	S129	-5445	154	1452	S79	-6195	154
1253	S278	-3210	299	1303	S228	-3960	299	1353	S178	-4710	299	1403	S128	-5460	299	1453	S78	-6210	299
1254	S277	-3225	154	1304	S227	-3975	154	1354	S177	-4725	154	1404	S127	-5475	154	1454	S77	-6225	154
1255	S276	-3240	299	1305	S226	-3990	299	1355	S176	-4740	299	1405	S126	-5490	299	1455	S76	-6240	299
1256	S275	-3255	154	1306	S225	-4005	154	1356	S175	-4755	154	1406	S125	-5505	154	1456	S75	-6255	154
1257	S274	-3270	299	1307	S224	-4020	299	1357	S174	-4770	299	1407	S124	-5520	299	1457	S74	-6270	299
1258	S273	-3285	154	1308	S223	-4035	154	1358	S173	-4785	154	1408	S123	-5535	154	1458	S73	-6285	154
1259	S272	-3300	299	1309	S222	-4050	299	1359	S172	-4800	299	1409	S122	-5550	299	1459	S72	-6300	299
1260	S271	-3315	154	1310	S221	-4065	154	1360	S171	-4815	154	1410	S121	-5565	154	1460	S71	-6315	154
1261	S270	-3330	299	1311	S220	-4080	299	1361	S170	-4830	299	1411	S120	-5580	299	1461	S70	-6330	299
1262	S269	-3345	154	1312	S219	-4095	154	1362	S169	-4845	154	1412	S119	-5595	154	1462	S69	-6345	154
1263	S268	-3360	299	1313	S218	-4110	299	1363	S168	-4860	299	1413	S118	-5610	299	1463	S68	-6360	299
1264	S267	-3375	154	1314	S217	-4125	154	1364	S167	-4875	154	1414	S117	-5625	154	1464	S67	-6375	154
1265	S266	-3390	299	1315	S216	-4140	299	1365	S166	-4890	299	1415	S116	-5640	299	1465	S66	-6390	299
1266	S265	-3405	154	1316	S215	-4155	154	1366	S165	-4905	154	1416	S115	-5655	154	1466	S65	-6405	154
1267	S264	-3420	299	1317	S214	-4170	299	1367	S164	-4920	299	1417	S114	-5670	299	1467	S64	-6420	299
1268	S263	-3435	154	1318	S213	-4185	154	1368	S163	-4935	154	1418	S113	-5685	154	1468	S63	-6435	154
1269	S262	-3450	299	1319	S212	-4200	299	1369	S162	-4950	299	1419	S112	-5700	299	1469	S62	-6450	299
1270	S261	-3465	154	1320	S211	-4215	154	1370	S161	-4965	154	1420	S111	-5715	154	1470	S61	-6465	154
1271	S260	-3480	299	1321	S210	-4230	299	1371	S160	-4980	299	1421	S110	-5730	299	1471	S60	-6480	299
1272	S259	-3495	154	1322	S209	-4245	154	1372	S159	-4995	154	1422	S109	-5745	154	1472	S59	-6495	154
1273	S258	-3510	299	1323	S208	-4260	299	1373	S158	-5010	299	1423	S108	-5760	299	1473	S58	-6510	299
1274	S257	-3525	154	1324	S207	-4275	154	1374	S157	-5025	154	1424	S107	-5775	154	1474	S57	-6525	154
1275	S256	-3540	299	1325	S206	-4290	299	1375	S156	-5040	299	1425	S106	-5790	299	1475	S56	-6540	299
1276	S255	-3555	154	1326	S205	-4305	154	1376	S155	-5055	154	1426	S105	-5805	154	1476	S55	-6555	154
1277	S254	-3570	299	1327	S204	-4320	299	1377	S154	-5070	299	1427	S104	-5820	299	1477	S54	-6570	299
1278	S253	-3585	154	1328	S203	-4335	154	1378	S153	-5085	154	1428	S103	-5835	154	1478	S53	-6585	154
1279	S252	-3600	299	1329	S202	-4350	299	1379	S152	-5100	299	1429	S102	-5850	299	1479	S52	-6600	299
1280	S251	-3615	154	1330	S201	-4365	154	1380	S151	-5115	154	1430	S101	-5865	154	1480	S51	-6615	154
1281	S250	-3630	299	1331	S200	-4380	299	1381	S150	-5130	299	1431	S100	-5880	299	1481	S50	-6630	299
1282	S249	-3645	154	1332	S199	-4395	154	1382	S149	-5145	154	1432	S99	-5895	154	1482	S49	-6645	154
1283	S248	-3660	299	1333	S198	-4410	299	1383	S148	-5160	299	1433	S98	-5910	299	1483	S48	-6660	299
1284	S247	-3675	154	1334	S197	-4425	154	1384	S147	-5175	154	1434	S97	-5925	154	1484	S47	-6675	154
1285	S246	-3690	299	1335	S196	-4440	299	1385	S146	-5190	299	1435	S96	-5940	299	1485	S46	-6690	299
1286	S245	-3705	154	1336	S195	-4455	154	1386	S145	-5205	154	1436	S95	-5955	154	1486	S45	-6705	154
1287	S244	-3720	299	1337	S194	-4470	299	1387	S144	-5220	299	1437	S94	-5970	299	1487	S44	-6720	299
1288	S243	-3735	154	1338	S193	-4485	154	1388	S143	-5235	154	1438	S93	-5985	154	1488	S43	-6735	154
1289	S242	-3750	299	1339	S192	-4500	299	1389	S142	-5250	299	1439	S92	-6000	299	1489	S42	-6750	299
1290	S241	-3765	154	1340	S191	-4515	154	1390	S141	-5265	154	1440	S91	-6015	154	1490	S41	-6765	154
1291	S240	-3780	299	1341	S190	-4530	299	1391	S140	-5280	299	1441	S90	-6030	299	1491	S40	-6780	299
1292	S239	-3795	154	1342	S189	-4545	154	1392	S139	-5295	154	1442	S89	-6045	154	1492	S39	-6795	154
1293	S238	-3810	299	1343	S188	-4560	299	1393	S138	-5310	299	1443	S88	-6060	299	1493	S38	-6810	299
1294	S237	-3825	154	1344	S187	-4575	154	1394	S137	-5325	154	1444	S87	-6075	154	1494	S37	-6825	154
1295	S236	-3840	299	1345	S186	-4590	299	1395	S136	-5340	299	1445	S86	-6090	299	1495	S36	-6840	299
1296	S235	-3855	154	1346	S185	-4605	154	1396	S135	-5355	154	1446	S85	-6105	154	1496	S35	-6855	154
1297	S234	-3870	299	1347	S184	-4620	299	1397	S134	-5370	299	1447	S84	-6120	299	1497	S34	-6870	299
1298	S233	-3885	154	1348	S183	-4635	154	1398	S133	-5385	154	1448	S83	-6135	154	1498	S33	-6885	154
1299	S232	-3900	299	1349	S182	-4650	299	1399	S132	-5400	299	1449	S82	-6150	299	1499	S32	-6900	299
1300	S231	-3915	154	1350	S181	-4665	154	1400	S131	-5415	154	1450	S81	-6165	154	1500	S31	-6915	154

No.	Name	X	Y
1501	S30	-6930	299
1502	S29	-6945	154
1503	S28	-6960	299
1504	S27	-6975	154
1505	S26	-6990	299
1506	S25	-7005	154
1507	S24	-7020	299
1508	S23	-7035	154
1509	S22	-7050	299
1510	S21	-7065	154
1511	S20	-7080	299
1512	S19	-7095	154
1513	S18	-7110	299
1514	S17	-7125	154
1515	S16	-7140	299
1516	S15	-7155	154
1517	S14	-7170	299
1518	S13	-7185	154
1519	S12	-7200	299
1520	S11	-7215	154
1521	S10	-7230	299
1522	S9	-7245	154
1523	S8	-7260	299
1524	S7	-7275	154
1525	S6	-7290	299
1526	S5	-7305	154
1527	S4	-7320	299
1528	S3	-7335	154
1529	S2	-7350	299
1530	S1	-7365	154
1531	DUMMY	-7380	299
1532	DUMMY	-7395	154
1533	DUMMY	-7560	299
1534	DUMMY	-7575	154
1535	G480	-7590	299
1536	G478	-7605	154
1537	G476	-7620	299
1538	G474	-7635	154
1539	G472	-7650	299
1540	G470	-7665	154
1541	G468	-7680	299
1542	G466	-7695	154
1543	G464	-7710	299
1544	G462	-7725	154
1545	G460	-7740	299
1546	G458	-7755	154
1547	G456	-7770	299
1548	G454	-7785	154
1549	G452	-7800	299
1550	G450	-7815	154

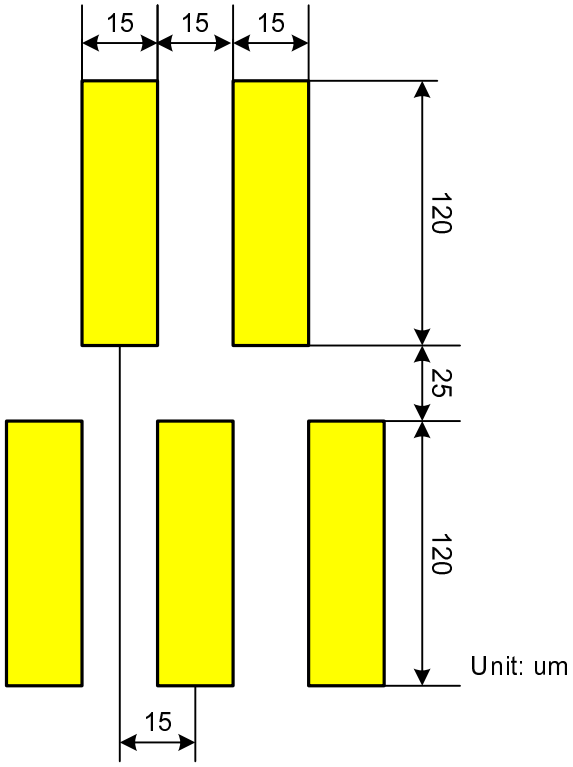
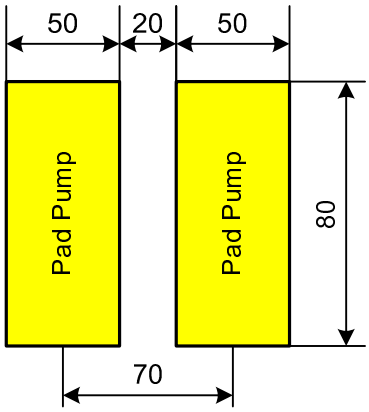
No.	Name	X	Y
1551	G448	-7830	299
1552	G446	-7845	154
1553	G444	-7860	299
1554	G442	-7875	154
1555	G440	-7890	299
1556	G438	-7905	154
1557	G436	-7920	299
1558	G434	-7935	154
1559	G432	-7950	299
1560	G430	-7965	154
1561	G428	-7980	299
1562	G426	-7995	154
1563	G424	-8010	299
1564	G422	-8025	154
1565	G420	-8040	299
1566	G418	-8055	154
1567	G416	-8070	299
1568	G414	-8085	154
1569	G412	-8100	299
1570	G410	-8115	154
1571	G408	-8130	299
1572	G406	-8145	154
1573	G404	-8160	299
1574	G402	-8175	154
1575	G400	-8190	299
1576	G398	-8205	154
1577	G396	-8220	299
1578	G394	-8235	154
1579	G392	-8250	299
1580	G390	-8265	154
1581	G388	-8280	299
1582	G386	-8295	154
1583	G384	-8310	299
1584	G382	-8325	154
1585	G380	-8340	299
1586	G378	-8355	154
1587	G376	-8370	299
1588	G374	-8385	154
1589	G372	-8400	299
1590	G370	-8415	154
1591	G368	-8430	299
1592	G366	-8445	154
1593	G364	-8460	299
1594	G362	-8475	154
1595	G360	-8490	299
1596	G358	-8505	154
1597	G356	-8520	299
1598	G354	-8535	154
1599	G352	-8550	299
1600	G350	-8565	154

No.	Name	X	Y
1601	G348	-8580	299
1602	G346	-8595	154
1603	G344	-8610	299
1604	G342	-8625	154
1605	G340	-8640	299
1606	G338	-8655	154
1607	G336	-8670	299
1608	G334	-8685	154
1609	G332	-8700	299
1610	G330	-8715	154
1611	G328	-8730	299
1612	G326	-8745	154
1613	G324	-8760	299
1614	G322	-8775	154
1615	G320	-8790	299
1616	G318	-8805	154
1617	G316	-8820	299
1618	G314	-8835	154
1619	G312	-8850	299
1620	G310	-8865	154
1621	G308	-8880	299
1622	G306	-8895	154
1623	G304	-8910	299
1624	G302	-8925	154
1625	G300	-8940	299
1626	G298	-8955	154
1627	G296	-8970	299
1628	G294	-8985	154
1629	G292	-9000	299
1630	G290	-9015	154
1631	G288	-9030	299
1632	G286	-9045	154
1633	G284	-9060	299
1634	G282	-9075	154
1635	G280	-9090	299
1636	G278	-9105	154
1637	G276	-9120	299
1638	G274	-9135	154
1639	G272	-9150	299
1640	G270	-9165	154
1641	G268	-9180	299
1642	G266	-9195	154
1643	G264	-9210	299
1644	G262	-9225	154
1645	G260	-9240	299
1646	G258	-9255	154
1647	G256	-9270	299
1648	G254	-9285	154
1649	G252	-9300	299
1650	G250	-9315	154

No.	Name	X	Y
1651	G248	-9330	299
1652	G246	-9345	154
1653	G244	-9360	299
1654	G242	-9375	154
1655	G240	-9390	299
1656	G238	-9405	154
1657	G236	-9420	299
1658	G234	-9435	154
1659	G232	-9450	299
1660	G230	-9465	154
1661	G228	-9480	299
1662	G226	-9495	154
1663	G224	-9510	299
1664	G222	-9525	154
1665	G220	-9540	299
1666	G218	-9555	154
1667	G216	-9570	299
1668	G214	-9585	154
1669	G212	-9600	299
1670	G210	-9615	154
1671	G208	-9630	299
1672	G206	-9645	154
1673	G204	-9660	299
1674	G202	-9675	154
1675	G200	-9690	299
1676	G198	-9705	154
1677	G196	-9720	299
1678	G194	-9735	154
1679	G192	-9750	299
1680	G190	-9765	154
1681	G188	-9780	299
1682	G186	-9795	154
1683	G184	-9810	299
1684	G182	-9825	154
1685	G180	-9840	299
1686	G178	-9855	154
1687	G176	-9870	299
1688	G174	-9885	154
1689	G172	-9900	299
1690	G170	-9915	154
1691	G168	-9930	299
1692	G166	-9945	154
1693	G164	-9960	299
1694	G162	-9975	154
1695	G160	-9990	299
1696	G158	-10005	154
1697	G156	-10020	299
1698	G154	-10035	154
1699	G152	-10050	299
1700	G150	-10065	154

No.	Name	X	Y
1701	G148	-10080	299
1702	G146	-10095	154
1703	G144	-10110	299
1704	G142	-10125	154
1705	G140	-10140	299
1706	G138	-10155	154
1707	G136	-10170	299
1708	G134	-10185	154
1709	G132	-10200	299
1710	G130	-10215	154
1711	G128	-10230	299
1712	G126	-10245	154
1713	G124	-10260	299
1714	G122	-10275	154
1715	G120	-10290	299
1716	G118	-10305	154
1717	G116	-10320	299
1718	G114	-10335	154
1719	G112	-10350	299
1720	G110	-10365	154
1721	G108	-10380	299
1722	G106	-10395	154
1723	G104	-10410	299
1724	G102	-10425	154
1725	G100	-10440	299
1726	G98	-10455	154
1727	G96	-10470	299
1728	G94	-10485	154
1729	G92	-10500	299
1730	G90	-10515	154
1731	G88	-10530	299
1732	G86	-10545	154
1733	G84	-10560	299
1734	G82	-10575	154
1735	G80	-10590	299
1736	G78	-10605	154
1737	G76	-10620	299
1738	G74	-10635	154
1739	G72	-10650	299
1740	G70	-10665	154
1741	G68	-10680	299
1742	G66	-10695	154
1743	G64	-10710	299
1744	G62	-10725	154
1745	G60	-10740	299
1746	G58	-10755	154
1747	G56	-10770	299
1748	G54	-10785	154
1749	G52	-10800	299
1750	G50	-10815	154

No.	Name	X	Y
1751	G48	-10830	299
1752	G46	-10845	154
1753	G44	-10860	299
1754	G42	-10875	154
1755	G40	-10890	299
1756	G38	-10905	154
1757	G36	-10920	299
1758	G34	-10935	154
1759	G32	-10950	299
1760	G30	-10965	154
1761	G28	-10980	299
1762	G26	-10995	154
1763	G24	-11010	299
1764	G22	-11025	154
1765	G20	-11040	299
1766	G18	-11055	154
1767	G16	-11070	299
1768	G14	-11085	154
1769	G12	-11100	299
1770	G10	-11115	154
1771	G8	-11130	299
1772	G6	-11145	154
1773	G4	-11160	299
1774	G2	-11175	154
1775	DUMMY	-11190	299
1776	DUMMY	-11205	154
Alignment mark -Left		-11300	-270
Alignment mark -Right		11300	-270

S1 ~ S960 G1 ~ G480 (No. 321 ~ 1766)	
I/O pads (No.1 ~ 320)	

6. Block Function Description

MCU System Interface

The ILI9486 supplies four kinds of MCU system interface with 8080-series parallel interface, 3-/4-line serial interface, MIPI DSI interface and MDDI interface. The selection of the given interfaces are done by external IM [2:0] pins and shown as below:

IM2	IM1	IM0	Interface	Data Pin in Use
0	0	0	8080 18-bit bus interface	DB[17:0]
0	0	1	8080 9-bit bus interface	DB[8:0]
0	1	0	8080 16-bit bus interface	DB[15:0]
0	1	1	8080 8-bit bus interface	DB[7:0]
1	0	0	MDDI	MDDI_DATA_P MDDI_DATA_N MDDI_STB_P MDDI_STB_N
1	0	1	3-line SPI	SDA
1	1	0	MIPI DSI	MIPI_DATA_P, MIPI_DATA_N MIPI_CLOCK_P MIPI_CLOCK_N
1	1	1	4-line SPI	SDA

ILI9486 has a 16-bit index register (IR), a 18-bit write-data register (WDR), and an 18-bit read-data register (RDR). The IR is the register to store index information from control registers and the internal GRAM. The WDR is the register to temporarily store data to be written to control registers and the internal GRAM. The RDR is the register to temporarily store data read from the GRAM. Data from the MPU to be written to the internal GRAM are first written to the WDR and then automatically written to the internal GRAM in internal operation. Data are read via the RDR from the internal GRAM. Therefore, invalid data are read out to the data bus when the ILI9486 read the first data from the internal GRAM. Valid data are read out after the ILI9486 performs the second read operation.

Register are written consecutively as the register execution time except starting oscillator takes 0 clock cycle.

8080-Series			Operation
D/CX	RDX	WRX	
"L"	"H"	↑	Write command
"H"	↑	"H"	Read parameter
"H"	"H"	↑	Write parameter

Address Counter (AC)

The address counter (AC) gives an address to the internal GRAM. When the index of the register for setting a RAM address in the AC is written to the IR, the address information is sent from the IR to the AC. As writing data to the internal GRAM, the address in the AC is automatically updated plus or minus 1. The window address function enables writing data only in the rectangular area arbitrarily set by users on the GRAM.

Graphic RAM (GRAM)

The GRAM is graphics RAM storing bit-pattern data of 345,600 bytes with 18 bits per pixel, enabling a maximum 320(RGB) x480 dot graphic display.

Grayscale Voltage Generating Circuit

Grayscale voltage generating circuit generates a liquid crystal drive voltage, which corresponds to grayscale level set in the Gamma correction register. The ILI9486 can display 262k colors at the maximum.

Power Supply Circuit

The LCD drive power supply circuit generates the voltage levels as VREG1OUT, VGH, VGL and VCOM for driving TFT LCD panel.

Timing Generating

The timing generator generates timing signals for internal circuits such as the internal GRAM. The timing for display operation such as RAM read operation and the timing for internal operation such as RAM access by MPU is outputted separately so that they do not interfere with each other.

Oscillator

The ILI9486 incorporates RC oscillator circuit. The frame frequency is changeable by command settings.

Panel Driver Circuit

The liquid crystal display driver circuit consists of a 960-output source drivers (S1~S960) and a 480-output gate driver (G1~G480).

MIPI Controller Circuit

The MIPI controller circuit consists of D-PHY controller, protocol control unit (PCU), packet processing unit (PPU), ECC generating circuit, Internal data / command buffer and analog transceiver. The D-PHY controller is in charge of the communication with the analog block and ECC generating circuit will generate the ECC for outgoing data stream to accuracy of receiving data packet. The PCU is used to handle of outgoing and incoming data stream and PPU is charge of the transmitting packet distribution and merging. The internal data and command buffer is used as temporary storage for incoming command and display data.

7. Function Description

7.1. MCU interfaces

ILI9486 provides the 18-/16-/9-/8-bit parallel system interface for 8080 series, and 3-/4-line serial system interface for serial data input. The input system interface is selected by external pins as IM [2:0] and the bit formal per pixel color order is selected by DBI [2:0] bits.

7.1.1. MCU interface selection

The selection of a given interfaces are done by setting external pins IM [2:0] as show in the following table.

IM2	IM1	IM0	Interface	Data Pin in Use
0	0	0	8080 18-bit bus interface	DB[17:0]
0	0	1	8080 9-bit bus interface	DB[8:0]
0	1	0	8080 16-bit bus interface	DB[15:0]
0	1	1	8080 8-bit bus interface	DB[7:0]
1	0	0	MDDI	MDDI_DATA_P MDDI_DATA_N MDDI_STB_P MDDI_STB_N
1	0	1	3-line SPI	SDA
1	1	0	MIPI DSI	MIPI_DATA_P, MIPI_DATA_N MIPI_CLOCK_P MIPI_CLOCK_N
1	1	1	4-line SPI	SDA

7.1.2. 8080-Series Parallel Interface

ILI9486 can be accessed via 8-/9-/16-/18-bit MCU 8080-series parallel interface. The chip-select CSX (active low) is used to enable or disable ILI9486 chip. The RESX (active low) is an external reset signal. WRX is the parallel data write strobe, RDX is the parallel data read strobe and DB[17:0] is parallel data bus.

The MCU latches the input data at the rising edge of WRX signal. The D/CX is the signal of data/command selection. When D/CX='1', DB[17:0] bits are display RAM data or command parameters. When D/CX='0', D B[17:0] bits are commands.

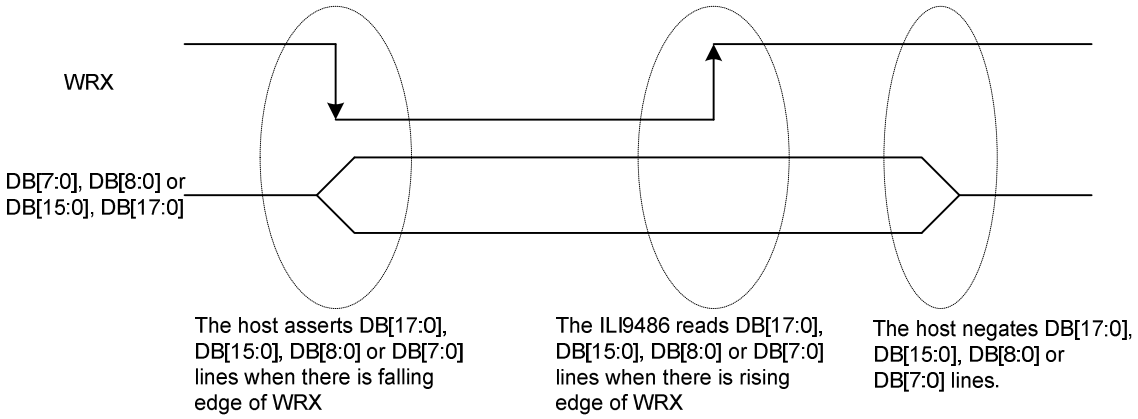
The 8080-series bi-directional interface can be used for communication between the MCU controller and LCD driver chip. The selection of 8080-series parallel interface is shown as the table in the following.

IM2	IM1	IM0	MPU-Interface Mode	WRX	RDX	D/CX	Function
0	0	0	8080 MCU 18-bit bus interface	↑	"H"	"L"	Write command code.
				"H"	↑	"H"	Read internal status.
				↑	"H"	"H"	Write parameter or display data.
				"H"	↑	"H"	Reads parameter or display data.
0	0	1	8080 MCU 9-bit bus interface	↑	"H"	"L"	Write command code.
				"H"	↑	"H"	Read internal status.
				↑	"H"	"H"	Write parameter or display data.
				"H"	↑	"H"	Reads parameter or display data.
0	1	0	8080 MCU 16-bit bus interface	↑	"H"	"L"	Write command code.
				"H"	↑	"H"	Read internal status.
				↑	"H"	"H"	Write parameter or display data.
				"H"	↑	"H"	Reads parameter or display data.
0	1	1	8080 MCU 8-bit bus interface	↑	"H"	"L"	Write command code.
				"H"	↑	"H"	Read internal status.
				↑	"H"	"H"	Write parameter or display data.
				"H"	↑	"H"	Reads parameter or display data.

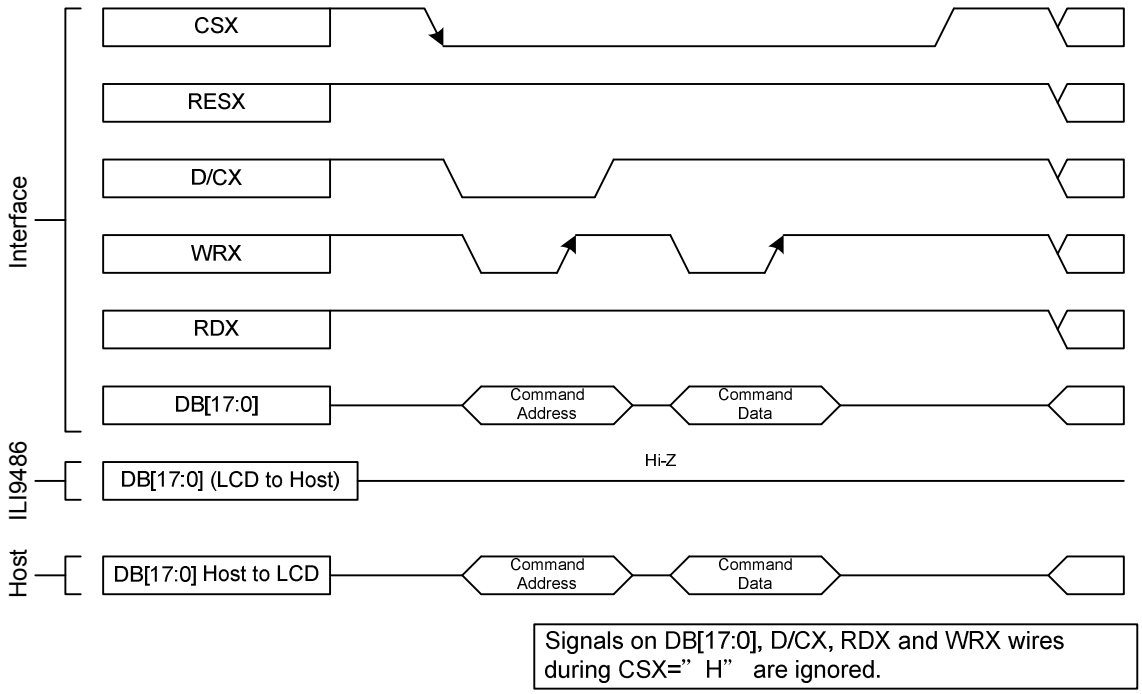
7.1.2.1. Write Cycle Sequence

The WRX signal is driven from high to low then pulled back to high during the write cycle. The host processor provides information during the write cycle when the display module captures the information from host processor on the rising edge of WRX. When the D/CX signal is driven to low level, then input data on the interface is interpreted as command information. The D/CX signal also can be pulled high level when the data on the interface is RAM data or command parameter.

The following figure shows a write cycle for the 8080 MCU interface.



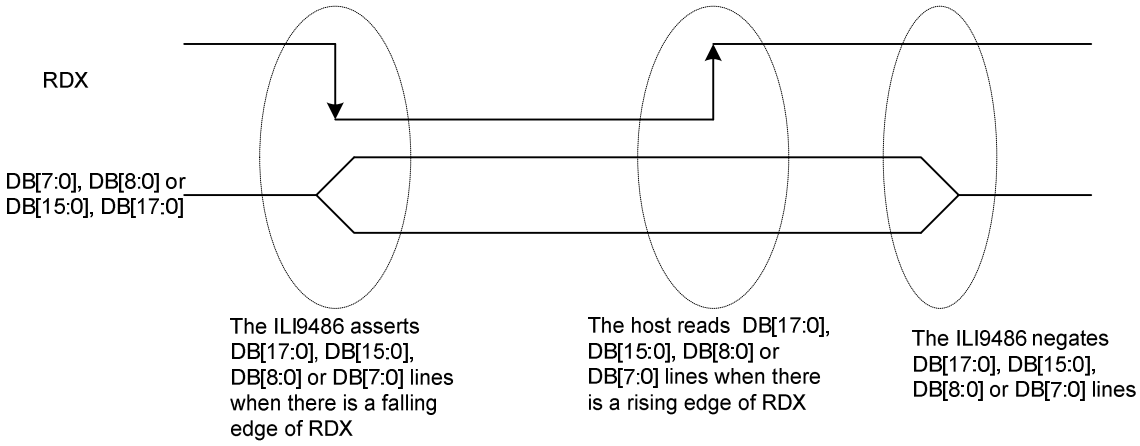
Note: WRX is an unsynchronized signal (It can be stopped)



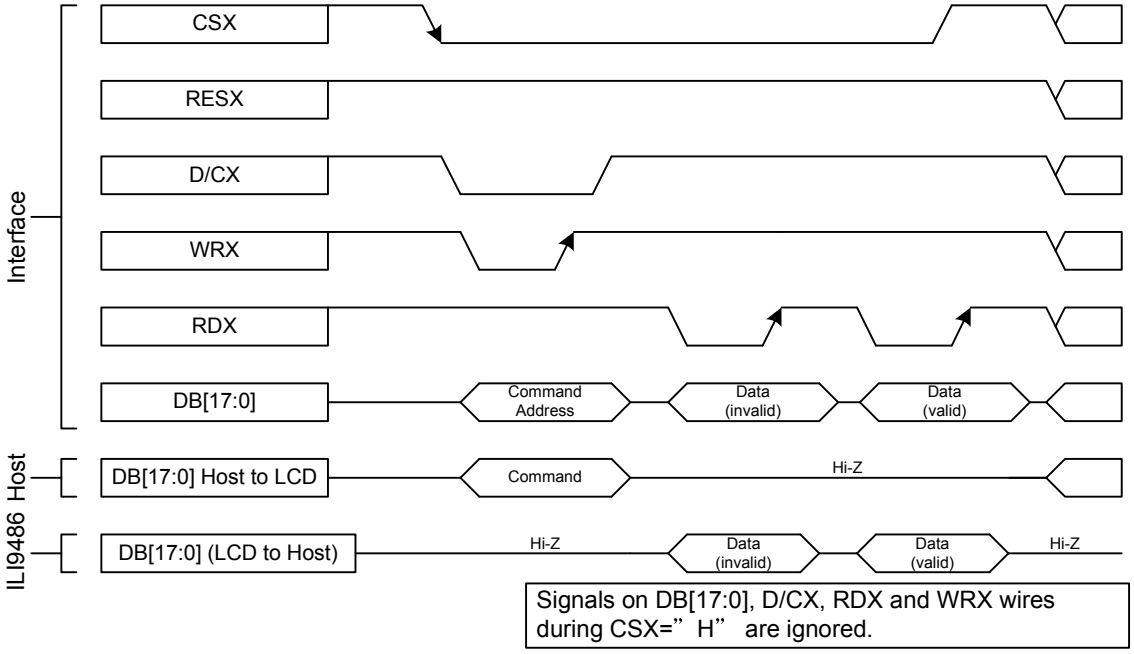
7.1.2.2. Read Cycle Sequence

The RDX signal is driven from high to low then allowed to be pulled back to high during the read cycle. The display module provides information to the host processor during the read cycle while the host processor reads the display module information on the rising edge of RDX signal. When the D/CX signal is driven to low level, then input data on the interface is interpreted as internal status or parameter. The D/CX signal also can be pulled high level when the data on the interface is RAM data or command parameter.

The following figure shows the read cycle for the 8080 MCU interface.



Note: RDX is an unsynchronized signal (It can be stopped).



Note: Read Data is only valid when the D/CX input is pulled high. If D/CX is driven low during read then the display information outputs will be High-Z.

7.1.3. Serial Interface

The selection of this interface is done by IM [2:0] bits. Please refer to the Table in the following.

IM2	IM1	IM0	MPU-Interface Mode	CSX	D/CX	SCL	Function
1	0	1	3-line serial interface	"L"	-	⎍	Read/Write command, parameter or display data.
1	1	1	4-line serial interface	"L"	"L"/"H"	⎍	Read/Write command, parameter or display data.

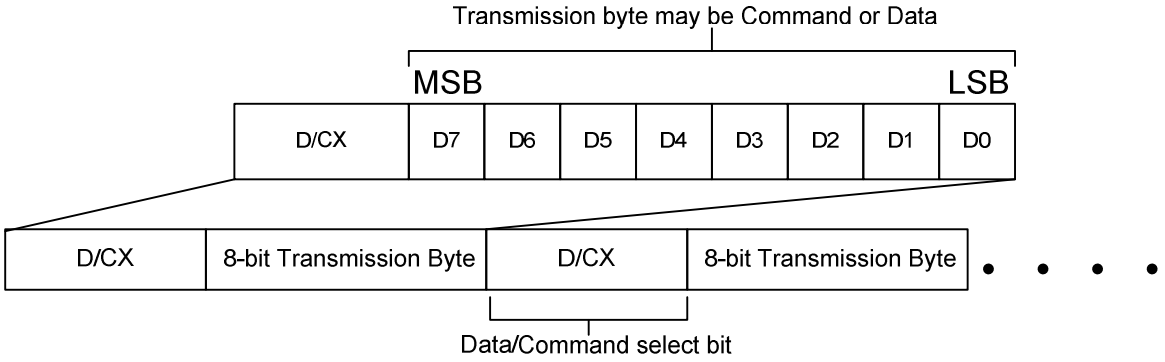
The ILI9486 supplies 3-lines/ 9-bit and 4-line/8-bit bi-directional serial interfaces for communication between the host and ILI9486. The 3-line serial mode consists of the chip enable input (CSX), the serial clock input (SCL) and serial data Input/Output (SDA). The 4-line serial mode consists of the Data/Command selection input (D/CX), chip enable input (CSX), the serial clock input (SCL) and serial data Input/Output (SDA) for data transmission. The data bus (D [17:0]) which are not used, must be leave these unused pins to open. Serial clock (SCL) is used for interface with MCU only, so it can be stopped when no communication is necessary.

7.1.3.1. Write Cycle Sequence

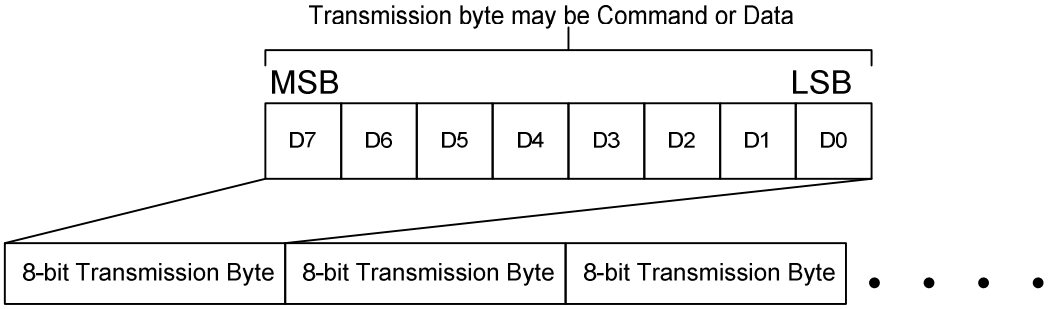
The write mode of the interface means the host writes commands and data to ILI9486. The 3-lines serial data packet contains a data/command select bit (D/CX) and a transmission byte. If D/CX is "low", the transmission byte is interpreted as a command byte. If D/CX is "high", the transmission byte is stored in the display data RAM (Memory write command), or command register as parameter.

Any instruction can be sent in any order to the ILI9486 and the MSB is transmitted first. The serial interface is initialized when CSX is high status. In this state, SCL clock pulse and SDA data are no effect. A falling edge on CSX enables the serial interface and indicates the start of data transmission. See the detail of data format for 3-/4-line serial interface.

Data Format for 3-line Serial Interface

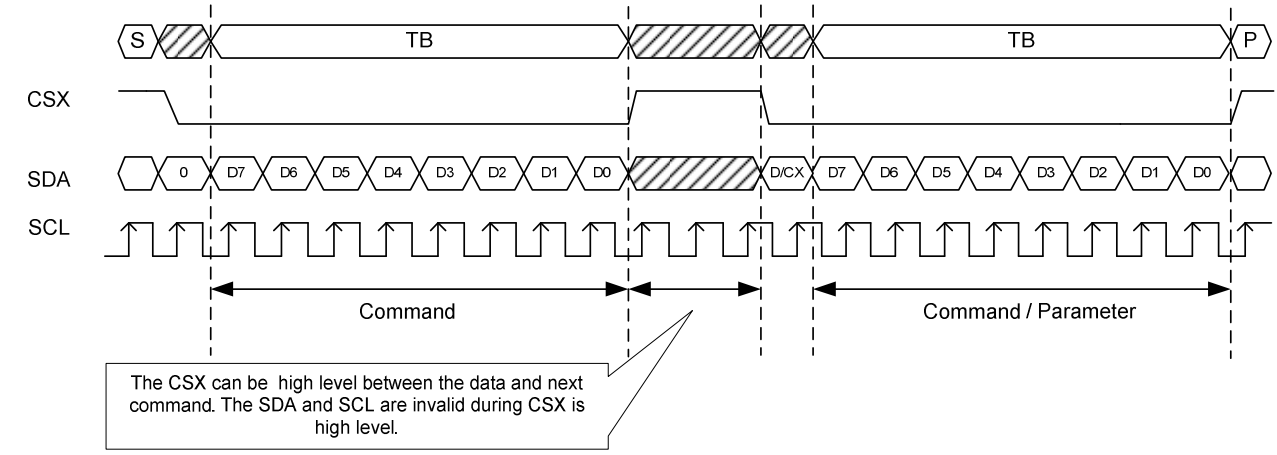


Data Format for 4-line Serial Interface

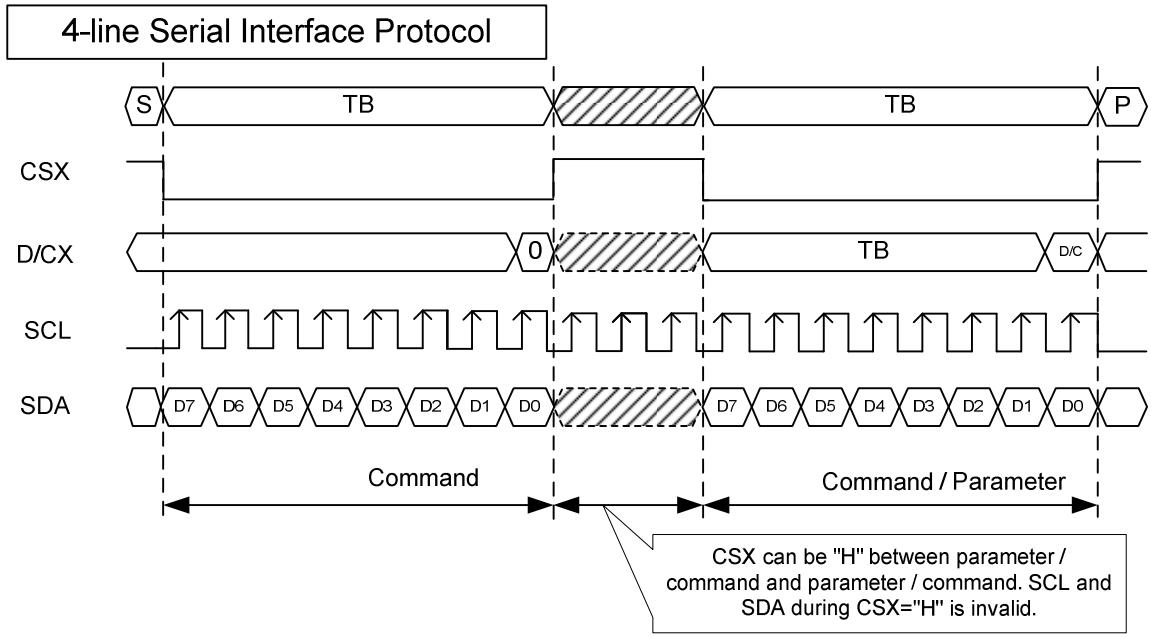


The host drives the CSX pin to low and starts by setting the D/CX bit on SDA. The bit is read by ILI9486 on the first rising edge of SCL signal. On the next falling edge of SCL, the MSB data bit (D7) is set on SDA by the host. On the next falling edge of SCL the next bit (D6) is set on SDA. If the optional D/CX signal is used, a byte is eight read cycle long. The 3/4-line serial interface writes sequence described in the Figure as below.

3-line Serial Interface Protocol



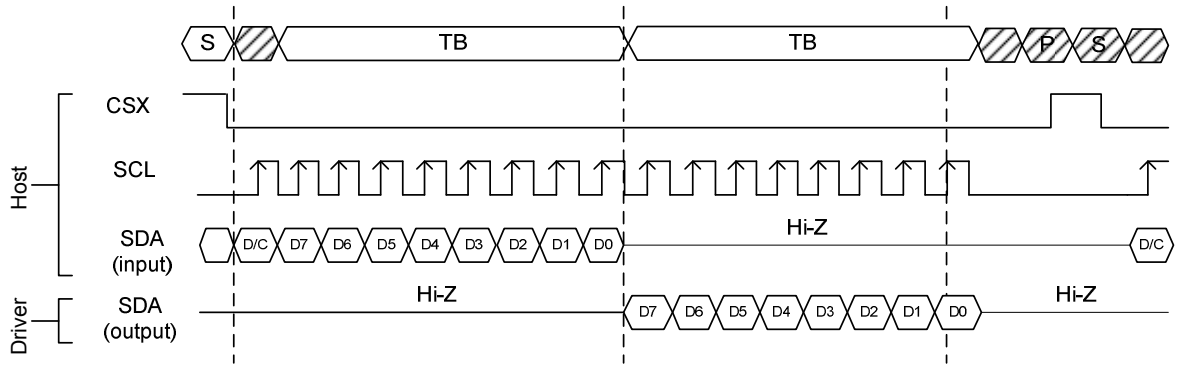
4-line Serial Interface Protocol



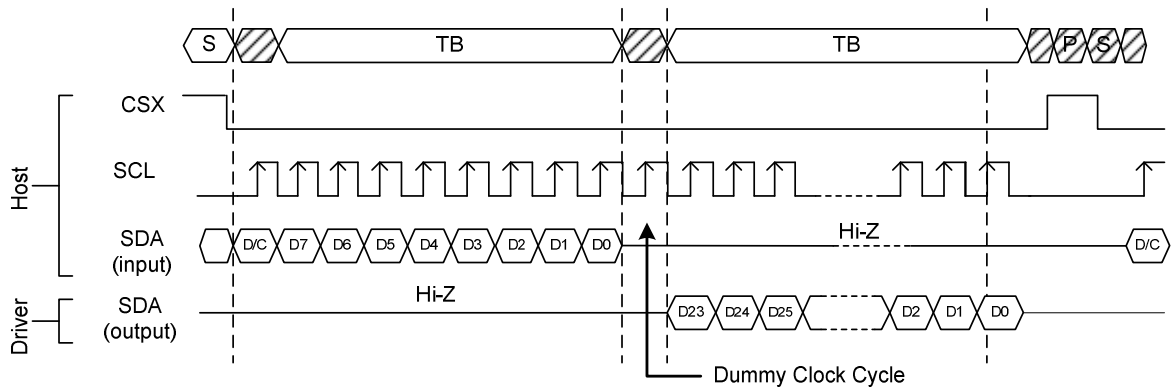
7.1.3.2. Read Cycle Sequence

The read mode of the interface means that the host reads register value from ILI9486. The host has to send a command (Read ID or register command) and then the following byte is transmitted in the opposite direction. The ILI9486 samples the SDA (input data) at the rising edges of SCL (serial clock), but shifts SDA (output data) at falling edges of SCL (serial clock). After the read status command has been sent, the SDA line must be set to tri-state no later than at the falling edge of SCL of the last bit. The read mode has three types of transmitted command data (8-/24-/32-bit) according command code.

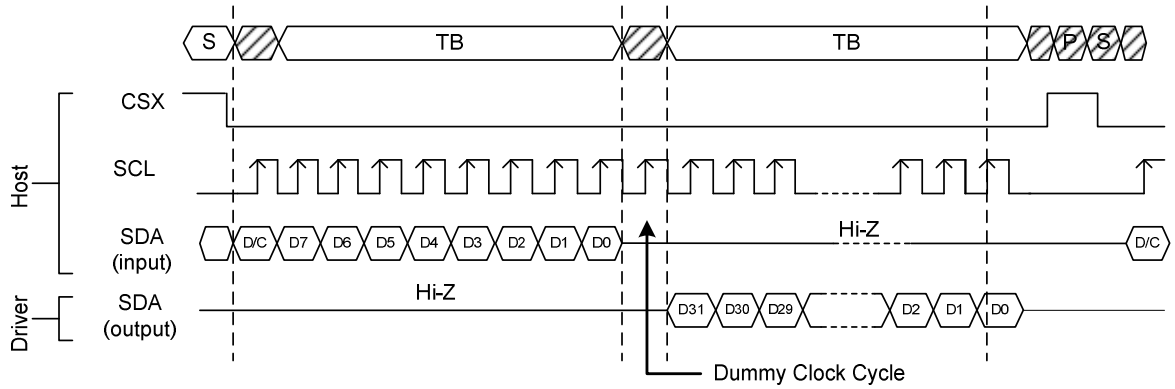
3-line Serial Protocol (for RDID1/RDID2/RDID3/0Ah/0Bh/0Ch/0Dh/0Eh/0Fh command: 8-bit read)



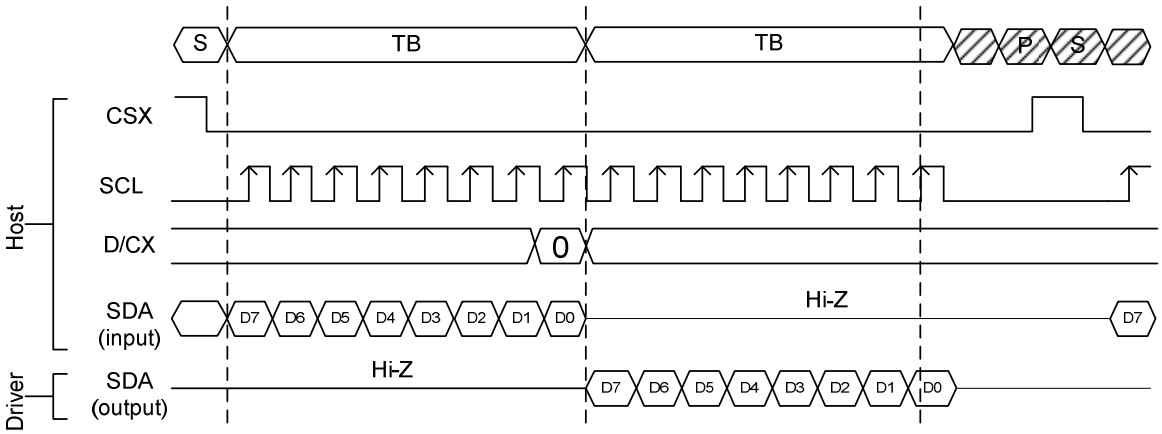
3-line Serial Protocol (for RDDID command: 24-bit read)



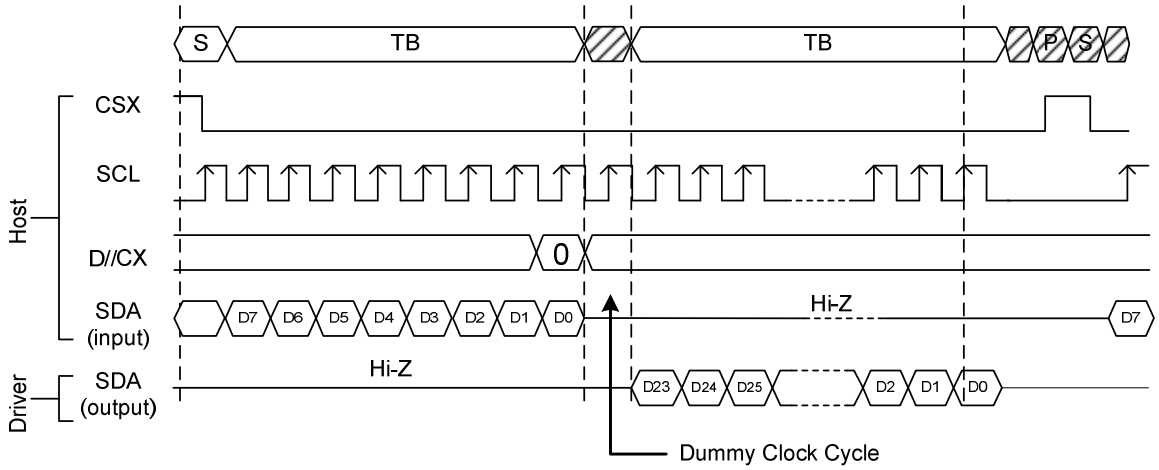
3-line Serial Protocol (for RDDST command: 32-bit read)



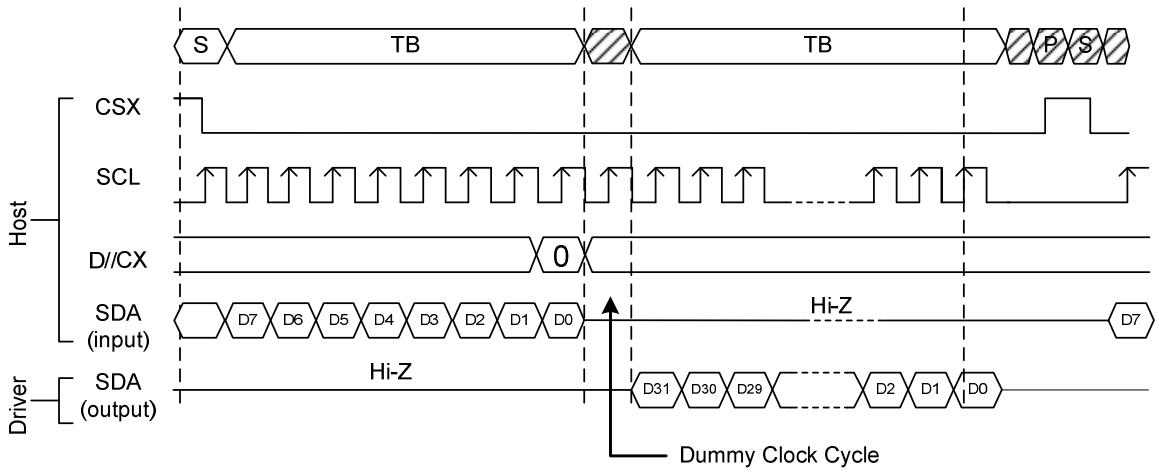
4-line Serial Protocol (for RDID1/RDID2/RDID3/0Ah/0Bh/0Ch/0Dh/0Eh/0Fh command: 8-bit read)



4-line Serial Protocol (for RDDID command: 24-bit read)

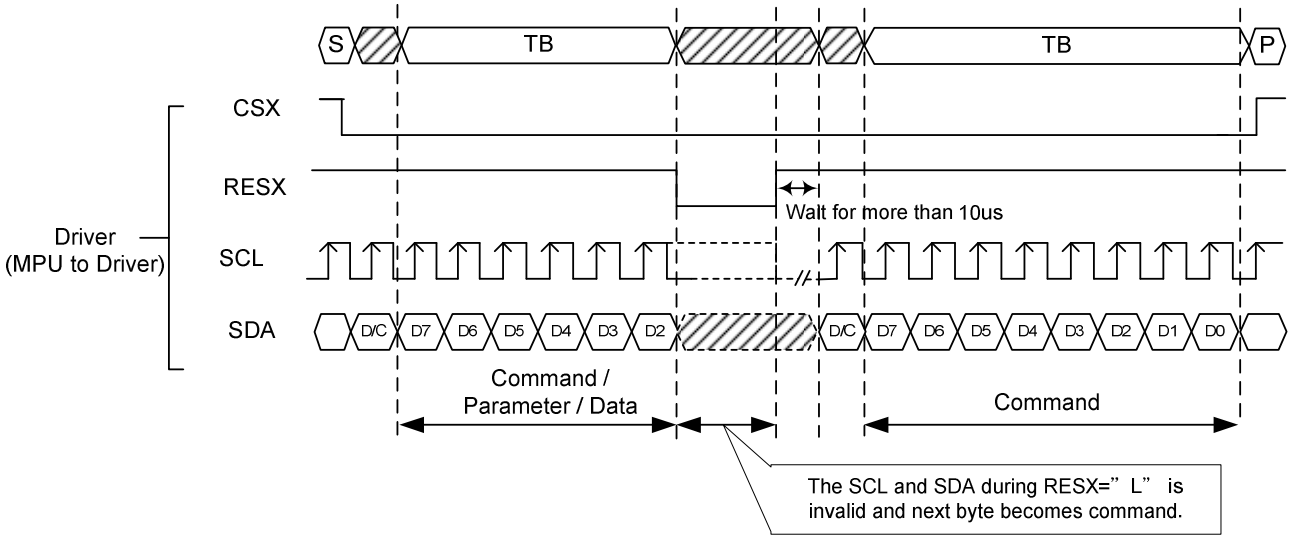


4-line Serial Protocol (for RDDST command: 32-bit read)

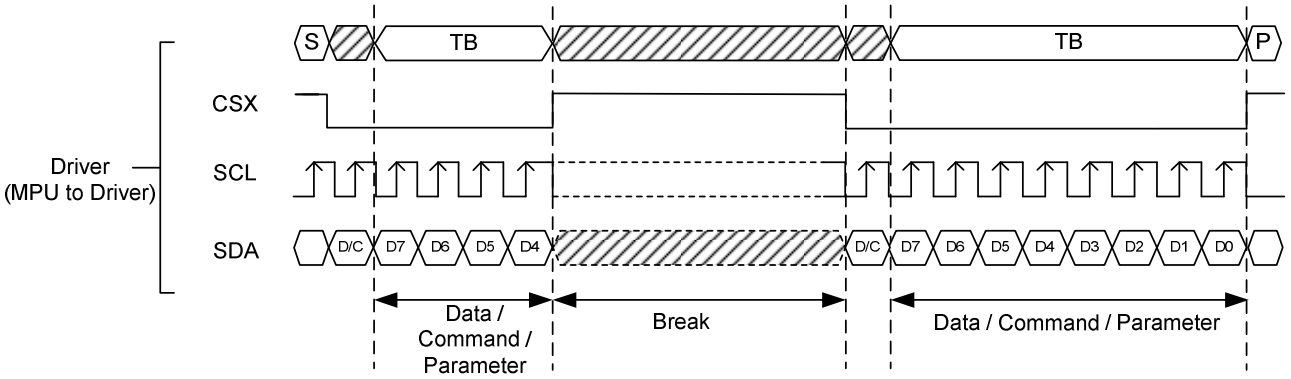


7.1.4. Data Transfer Break and Recovery

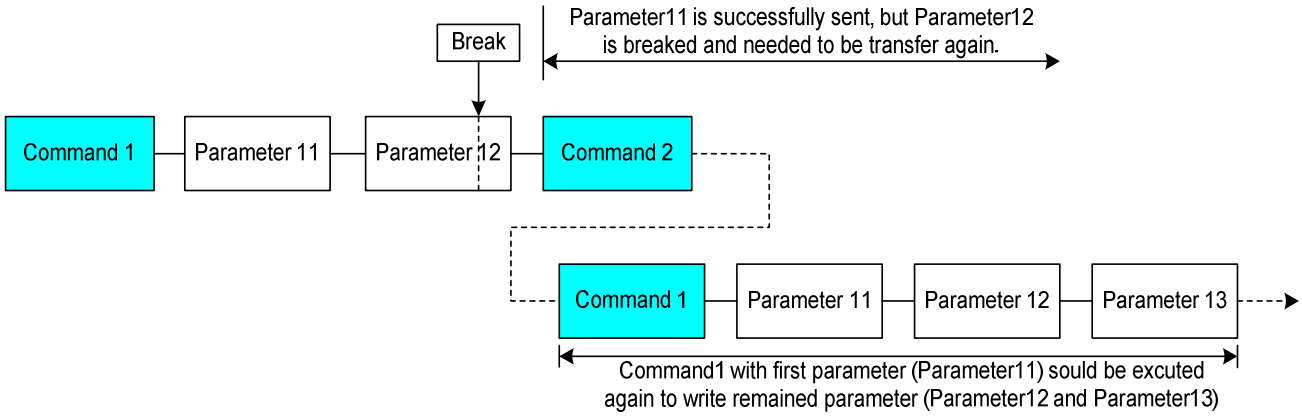
If there is a break in data transmission by RESX pulse, while transferring a Command or Frame Memory Data or Multiple Parameter command Data, before Bit D0 of the byte has been completed, then the driver will reject the previous bits and have reset the interface such that it will be ready to receive command data again when the chip select pin (CSX) is next activated after RESX have been High state.



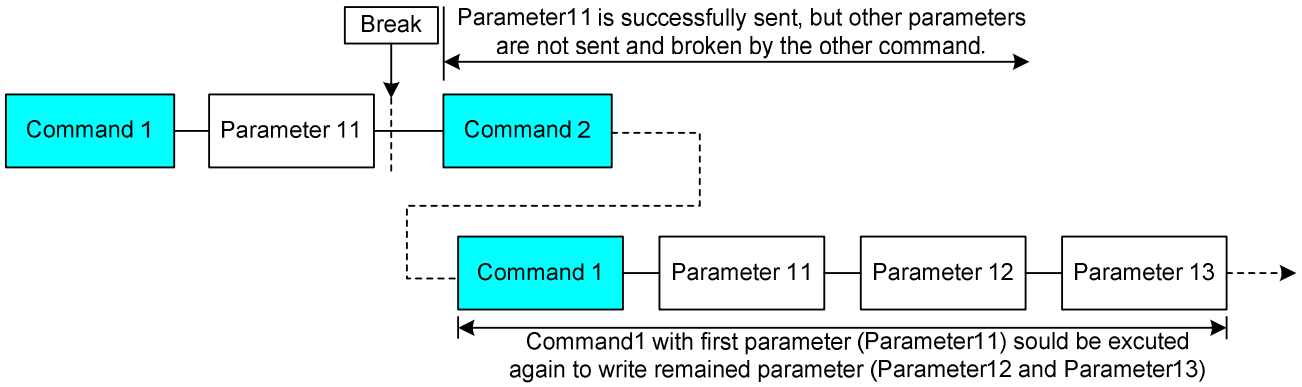
If there is a break in data transmission by CSX pulse, while transferring a Command or Frame Memory Data or Multiple Parameter command Data, before Bit D0 of the byte has been completed, then the driver will reject the previous bits and have reset the interface such that it will be ready to receive the same byte re-transmitted when the chip select pin (CSX) is next activated.



If a two or more parameter command is being sent and a break occurs while sending any parameter before the last one and if the host then sends a new command rather than continue to send the remained parameters that was interrupted, then the parameters that were successfully sent are stored and the parameter where the break occurred is rejected. The interface is ready to receive next byte as shown below.



If a two or more parameter command is being sent and a break occurs by the other command before the last one is sent, then the parameters that were successfully sent are stored and the other parameter of that command remains previous value.



7.1.5. Data Transfer Pause

It will be possible when transferring a Command, Frame Memory Data or Multiple Parameter Data to invoke a pause in the data transmission. If the Chip Select pin (CSX) is released after a whole byte of a Frame Memory Data or Multiple Parameter Data has been completed, then ILI9486 will wait and continue the Frame Memory Data or Parameter Data Transmission from the point where it was paused. If the Chip Select pin is released after a whole byte of a command has been completed, then the display module will receive either the command's parameters (if appropriate) or a new command when the Chip Select Line is next enabled as shown below.

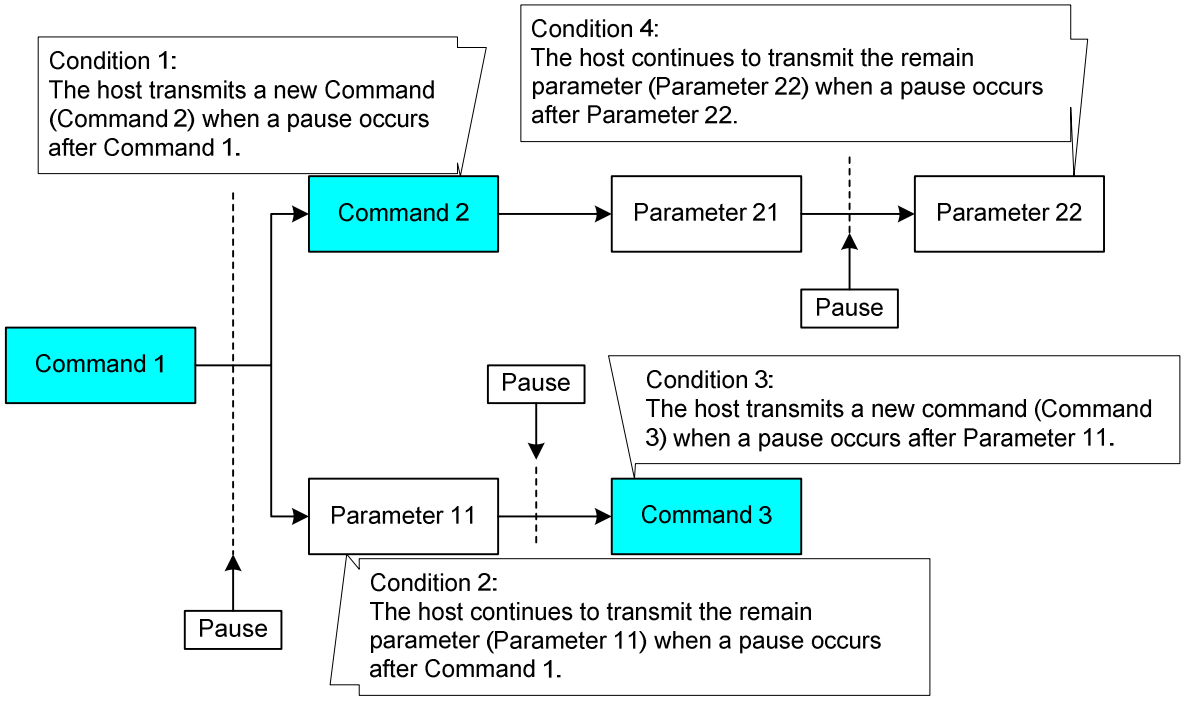
This applies to the following 4 conditions:

1) Command-Pause-Command

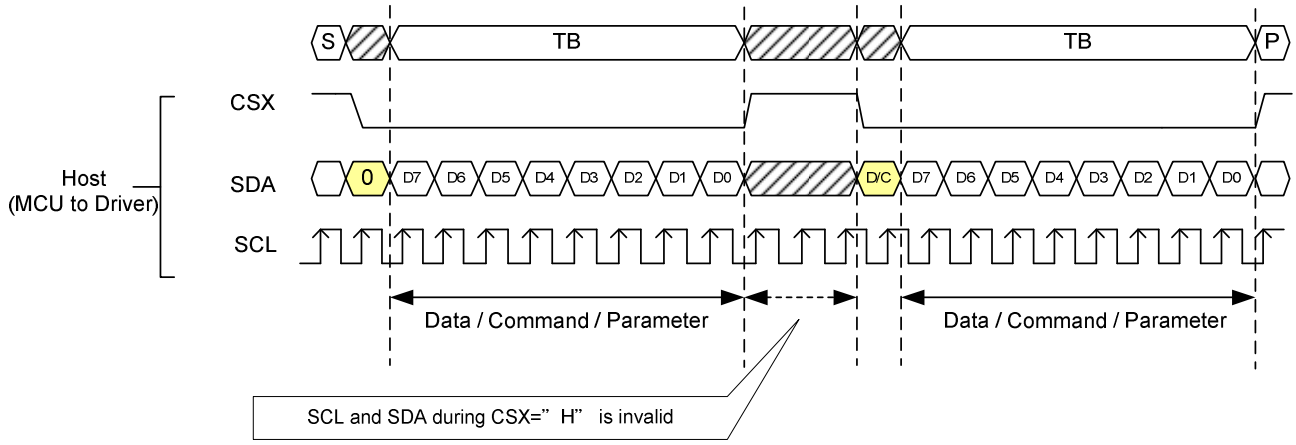
2) Command-Pause-Parameter

3) Parameter-Pause-Command

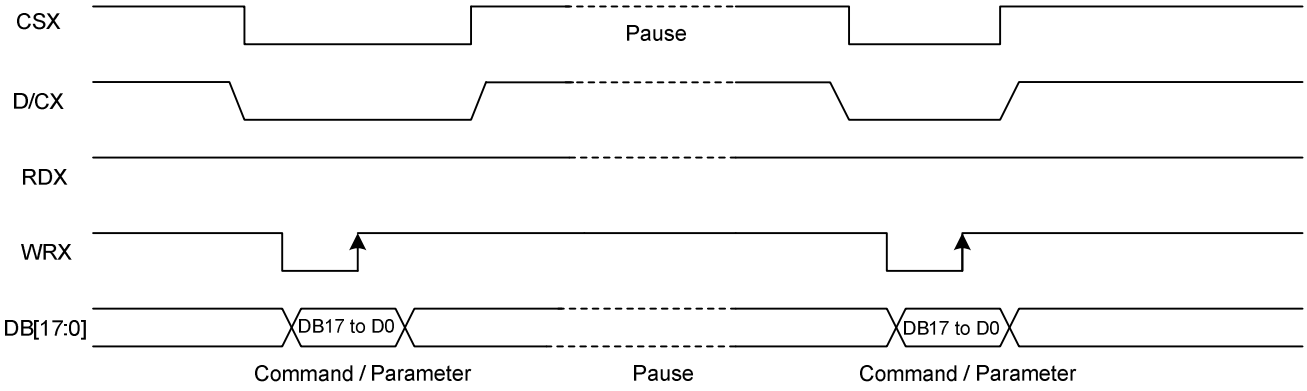
4) Parameter-Pause-Parameter



7.1.5.1. Serial Interface Pause



7.1.5.2. Parallel Interface Pause

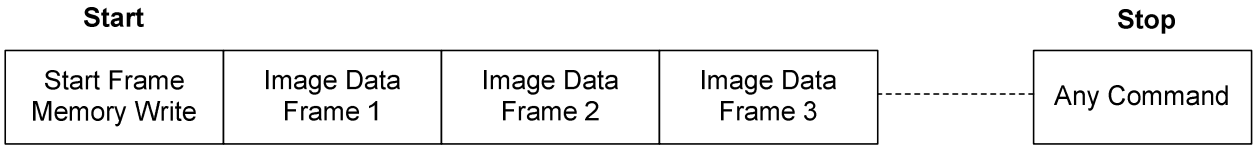


7.1.6. Data Transfer Mode

ILI9486 can provide four different kinds of color depth (8-bit/pixel, 9-bit/pixel, 16-bit/pixel and 18-bit/pixel) display data to the graphic RAM. The data format is described for each interface. Data can be downloaded to the Frame Memory by 2 methods.

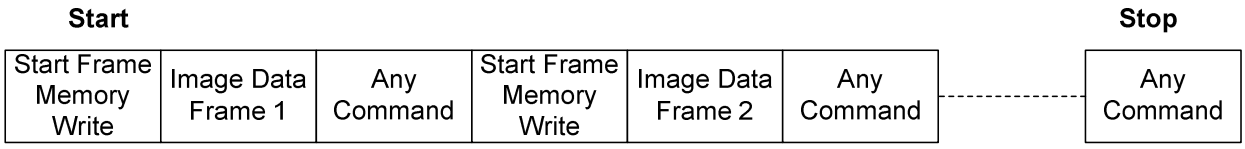
7.1.6.1. Method 1

The Image data is sent to the Frame Memory in the successive Frame writing, each time the Frame Memory is filled by image data, the Frame Memory pointer is reset to the start point and the next Frame is written.



7.1.6.2. Method 2

Image Data is sent and at the end of each Frame Memory download, a command is sent to stop Frame Memory Writing. Then Start Memory Write command is sent, and a new Frame is downloaded.



Note 1: These apply to all data transfer Color modes on both serial and parallel interfaces.

Note 2: The frame memory can contain both odd and even number of pixels for both methods. Only complete pixel data will be stored in the frame memory.

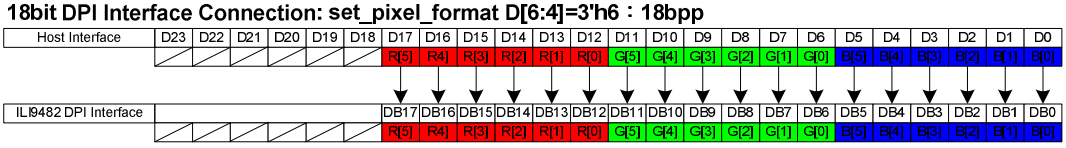
7.2. RGB Interface

7.2.1. RGB Interface Selection

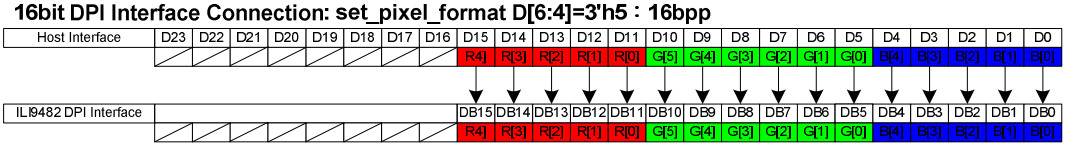
The ILI9486 has the RGB interface and these interfaces can be selected by RCM bit. When RCM is set to “0”, the DE mode is selected which utilizes VSYNC, HSYNC, DOTCLK, DE, D [17:0] pins; when RCM is set to “1”, the SYNC mode is selected which utilizes which utilizes VSYNC, HSYNC, DOTCLK, D [17:0] pins. The ILI9486 supports several pixel format that can be selected by DPI[3:0] bits in “Pixel Format Set (3Ah)” command. The selection of a given interfaces are done by DPI[3:0] as show in the following table.

RCM	DPI[2:0]				RGB Interface Mode	RGB Mode	Used Pins
0	0	1	1	0	18-bit RGB interface (262K colors)	**DE Mode** Valid data is determined by the DE signal	VSYNC, HSYNC, DE, DOTCLK,D[17:0]
0	0	1	0	1	16-bit RGB interface (65K colors)		VSYNC, HSYNC, DE, DOTCLK,D[15:0]
1	0	1	1	0	18-bit RGB interface (262K colors)	**SYNC Mode** In SYNC mode, DE signal is ignored; blanking porch is determined by B5h command.	VSYNC, HSYNC, DOTCLK, D[17:0]
1	0	1	0	1	16-bit RGB interface (65K colors)		VSYNC, HSYNC, DOTCLK, D[15:0]

18bit DPI Interface Connection: set_pixel_format D[6:4]=3'h6：18bpp



16bit DPI Interface Connection: set_pixel_format D[6:4]=3'h5：16bpp



Pixel clock (DOTCLK) is running all the time without stopping and it is used to entering VSYNC, HSYNC, ENABLE and DB[17:0] states when there is a rising edge of the DOTCLK. The DOTCLK can not be used as continues internal clock for other functions of the display module.

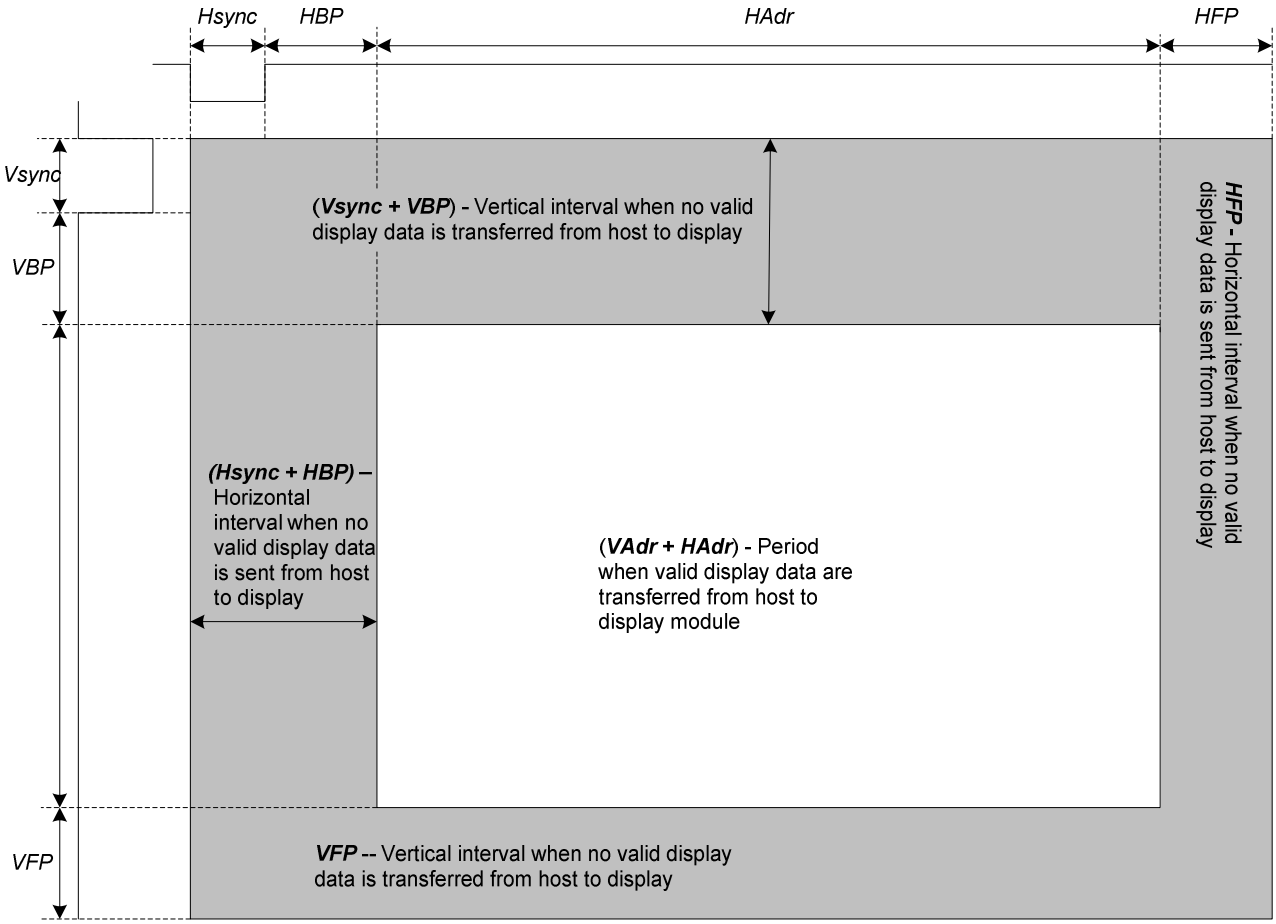
Vertical synchronization (VSYNC) is used to tell when there is received a new frame of the display. This is low enable and its state is read to the display module by a rising edge of the DOTCLK signal.

Horizontal synchronization (HSYNC) is used to tell when there is received a new line of the frame. This is low enable and its state is read to the display module by a rising edge of the DOTCLK signal.

Data Enable (ENABLE) is used to tell when there is received RGB information that should be transferred on the display. This is a high enable and its state is read to the display module by a rising edge of the DOTCLK signal.

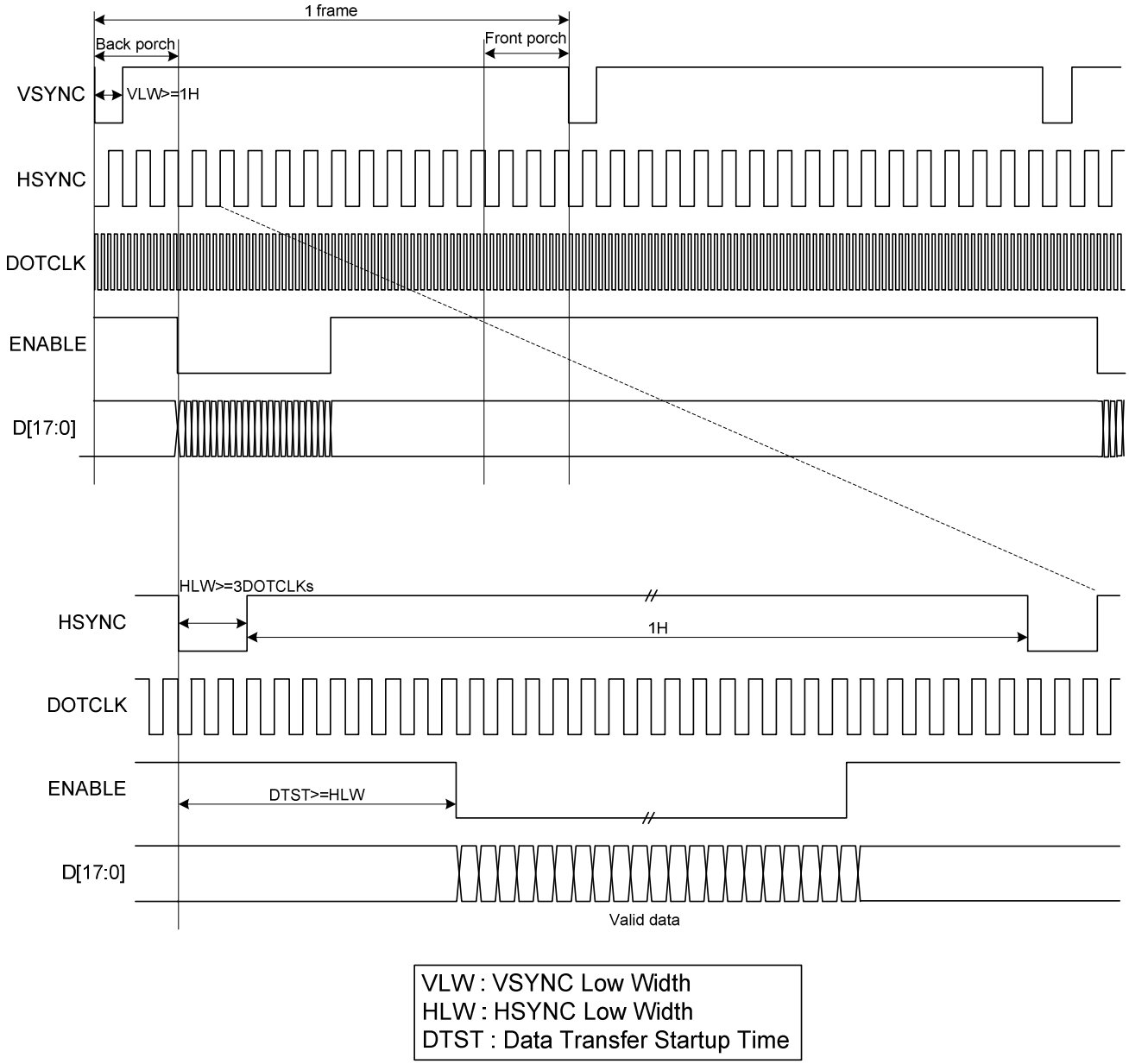
DB[17:0] are used to tell what is the information of the image that is transferred on the display (When

ENABLE= ’0’ (low) and there is a rising edge of DOTCLK). DB[17:0] can be ‘0’ (low) or ‘1’ (high). These lines are read by a rising edge of the DOTCLK signal. In RGB interface modes, the input display data is written to GRAM first then outputs corresponding source voltage according the gray data from GRAM.



7.2.2. RGB Interface Timing

The timing chart of 18-/16-bit RGB interface mode is shown as below.



VLW : VSYNC Low Width
HLW : HSYNC Low Width
DTST : Data Transfer Startup Time

Note 1: The DE signal is not needed when RGB interface SYNC mode is selected.

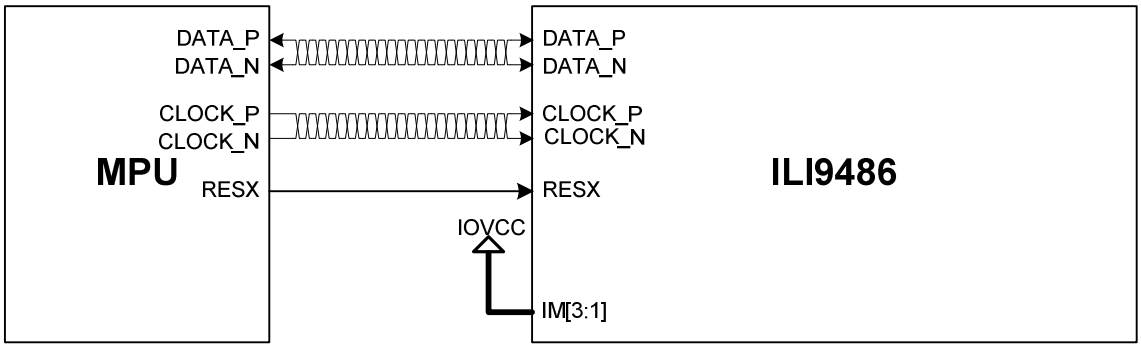
Note 2: VSPL='0', HSPL='0', DPL='0' and EPL='0' of "Interface Mode Control (B0h)" command.

7.3. MIPI – DSI (Mobile Industry Processor Interface – Display Serial Interface)

ILI9486 supports MIPI DSI which can be enabled or disabled by external IM [4] pin. ILI9486 can be accessed through one PHY lane module which communicates via two lines to a complementary part at the other side of the lane interconnects. The communication can be separated two different levels between the MCU and ILI9486:

- Low level communication what is done on the interface level.
- High level communication what is done on the packet level.

ILI9486 uses data and clock lane differential pairs for DSI, The data lane (DATAP and DATAN) is used for data communication and clock lane (CLKP and CLKN) is used to transmit the clock signal. The Mobile Industry Processor Interface (MIPI) can be used for communication between the processor and DSI-compliant LCD driver chip. The selection of this interface is done when IM [3:1] pins are high state (IOVCC level).



Low Power mode means that each line of the differential pair is used in single end mode and a differential receiver is disable (A termination resistor of the receiver is disable) and it can be driven into a low power mode. High Speed mode means that differential pairs (The termination resistor of the receiver is enable) are not used in the single end mode.

There are used different modes and protocols in each mode when there are wanted to transfer information from the MCU to ILI9486 and vice versa.

The State Codes of the High Speed (HS) and Low Power (LP) lane pair are defined below.

Lane Pair State Code	Line DC Voltage Levels		High Speed (HS)	Low Power	
	DATA_P	DATA_N	Burst Mode	CLOCK_P	CLOCK_N
HS-0	Low (HS)	High (HS)	Differential – 0	Note 1	Note1
HS-1	High (HS)	Low (HS)	Differential – 1	Note 1	Note 1
LP-00	Low (LP)	Low (LP)	Not Defined	Bridge	Space
LP-01	Low (LP)	High (LP)	Not Defined	HS – Request	Mark - 0
LP-10	High (LP)	Low (LP)	Not Defined	LP - Request	Mark - 1
LP-11	High (LP)	High (LP)	Not Defined	Stop	Note 2

Notes: (1) Low-Power Receivers (LP-Rx) of the lane pair are checking the LP-00 state code, when the Lane Pair is in the High Speed (HS) mode.

(2). If Low-Power Receivers (LP-Rx) of the lane pair recognizes LP-11 state code, the lane pair returns to LP-11 of the Control Mode.

7.3.1. Interface Level Communication – Clock Lanes

DSI-CLOCK_P/N lanes can be driven into three different power modes:

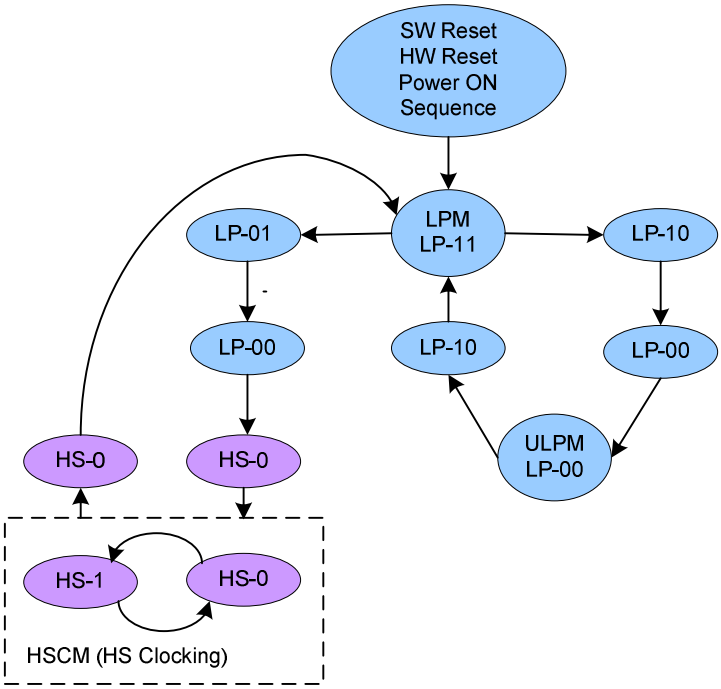
- Low Power Mode (LPM)
- Ultra Low Power Mode (ULPM)
- High Speed Clock Mode (HSCM)

Clock lanes are in a single end mode (LP = Low Power) when there is entering or leaving Low Power Mode (LPM) or Ultra Low Power Mode (ULPM).

Clock lanes are in the single end mode (LP = Low Power) when there is entering in or leaving out High Speed Clock Mode (HSCM).

These entering and leaving protocols are using clock lanes in the single end mode to generate an entering or leaving sequences.

The principal flow chart of the different clock lanes power modes is illustrated below.

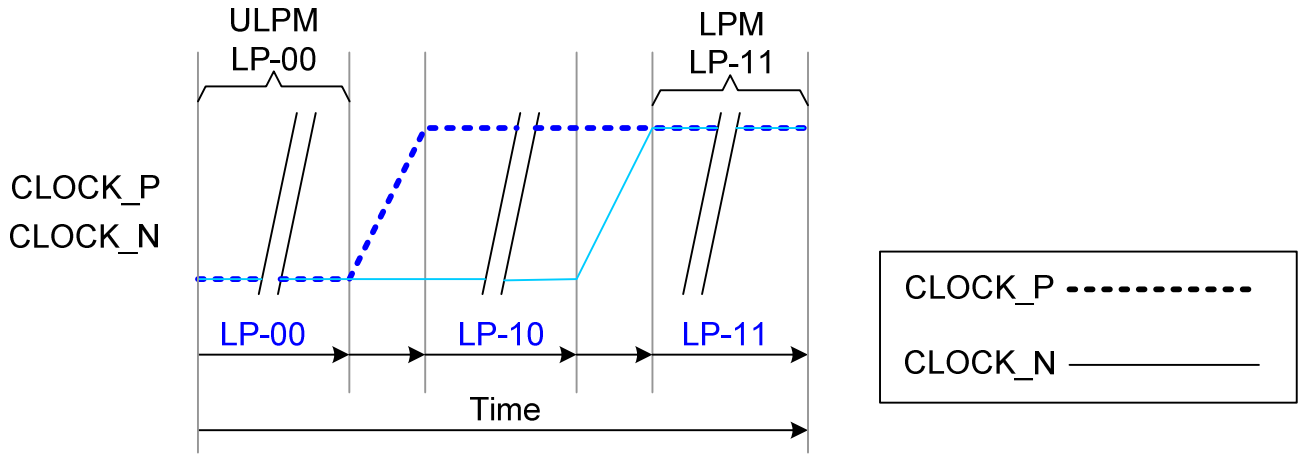


7.3.1.1. Low Power Mode (LPM)

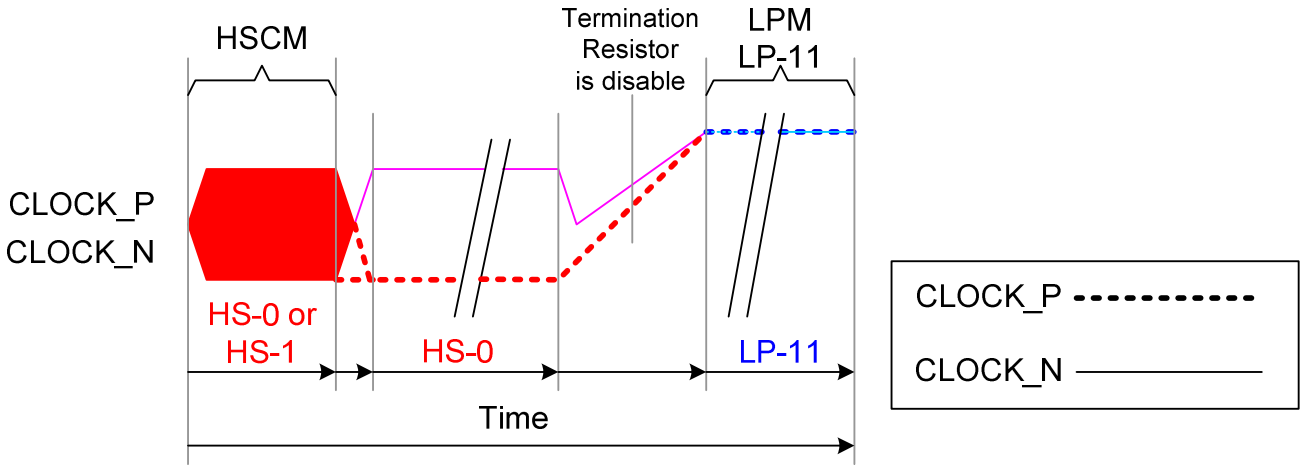
DSI-CLOCK_P/N lanes can be driven to the Low Power Mode (LPM), when DSI-CLOCK lanes are entering LP-11 State Code, in three different ways:

1) After SW Reset, HW Reset or Power On Sequence =>LP-11

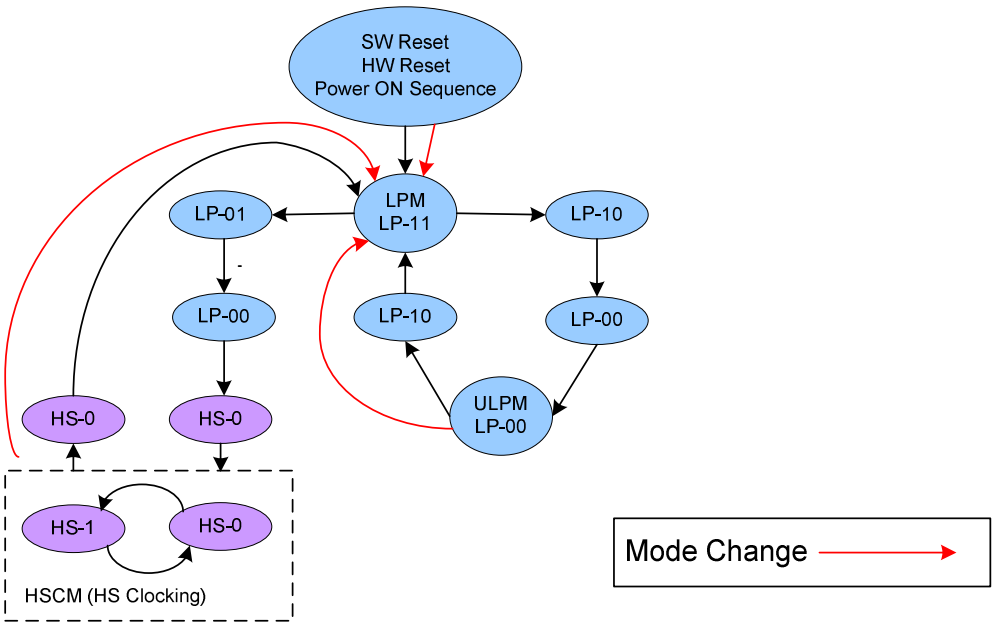
2) After DSI-CLOCK_P/N lanes are leaving Ultra Low Power Mode (ULPM, LP-00 State Code) =>LP-10 =>LP-11 (LPM). This sequence is illustrated below.



3) After DSI-CLK+/- lanes are leaving High Speed Clock Mode (HSCM, HS-0 or HS-1 State Code) =>HS-0 =>LP-11 (LPM). This sequence is illustrated below.



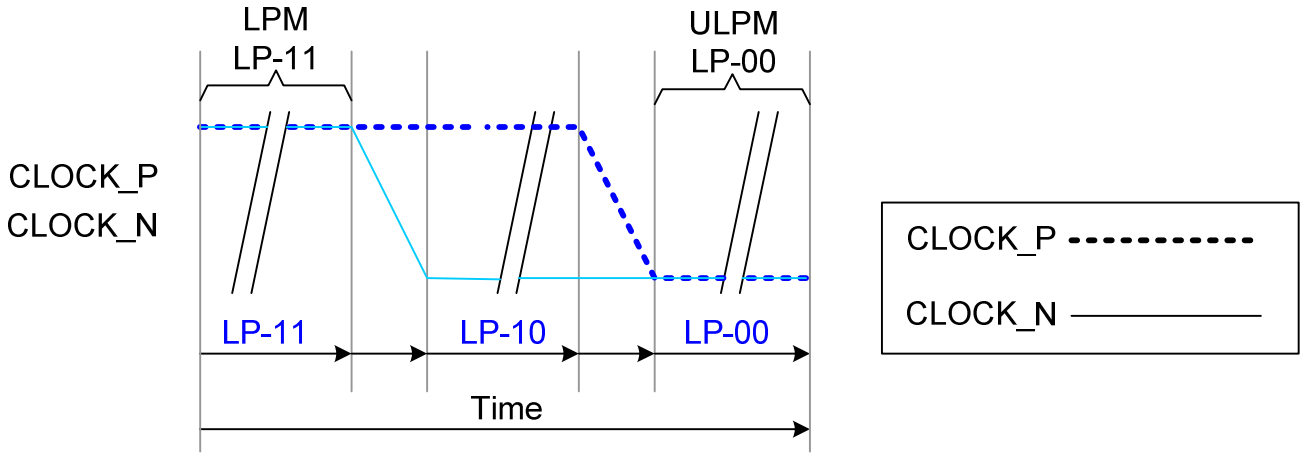
All three mode changes are illustrated a flow chart below.



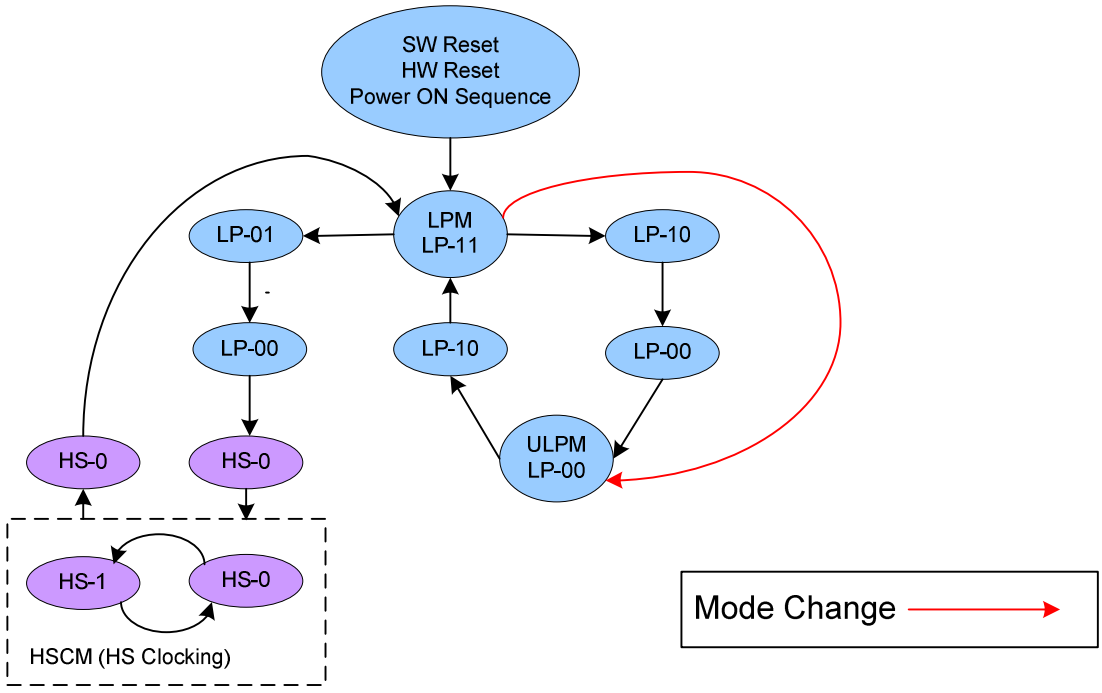
7.3.1.2. Ultra Low Power Mode (ULPM)

DSI-CLOCK_P/N lanes can be driven to the Ultra Low power Mode (ULPM), when DSI-CLOCK lanes are entering LP-00 State Code.

The only entering possibility is from the Low Power Mode (LPM, LP-11 State Code) =>LP-10 =>LP-00 (ULPM). This sequence is illustrated below.



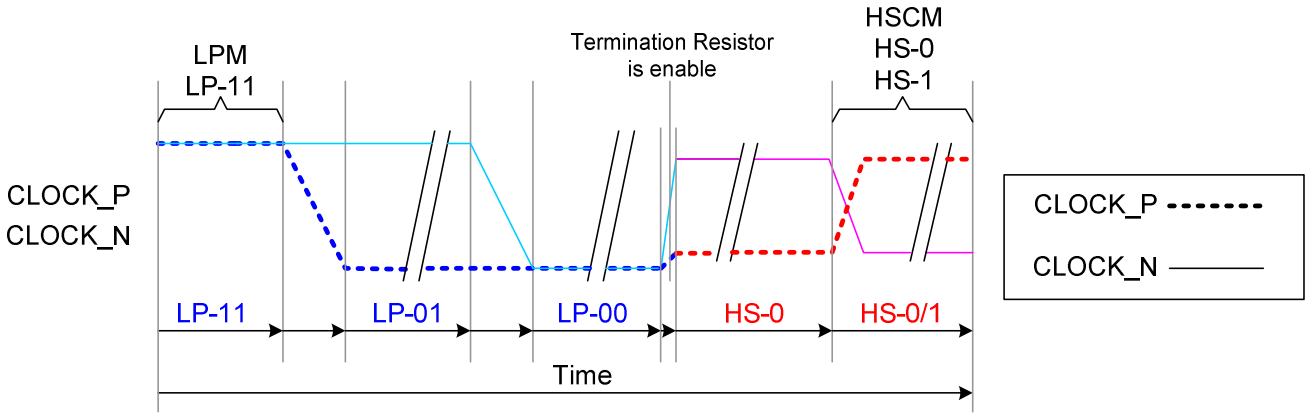
The mode change is also illustrated below.



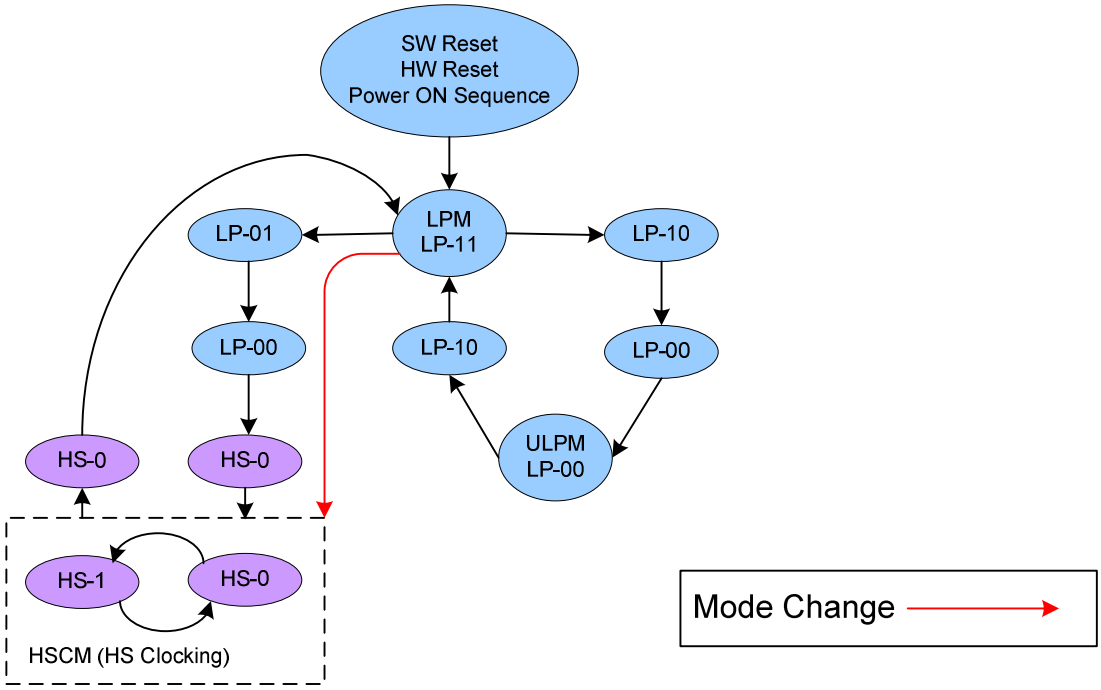
7.3.1.3. High-Speed Clocked Mode (HSCM)

DSI-CLOCK_P/N lanes can be driven to the High Speed Clock Mode (HSCM), when DSI-CLOCK lanes are starting to work between HS-0 and HS-1 State Codes.

The only entering possibility is from the Low Power Mode (LPM, LP-11 State Code) =>LP-01 =>LP-00 =>HS-0 =>HS-0/1 (HSCM). This sequence is illustrated below.

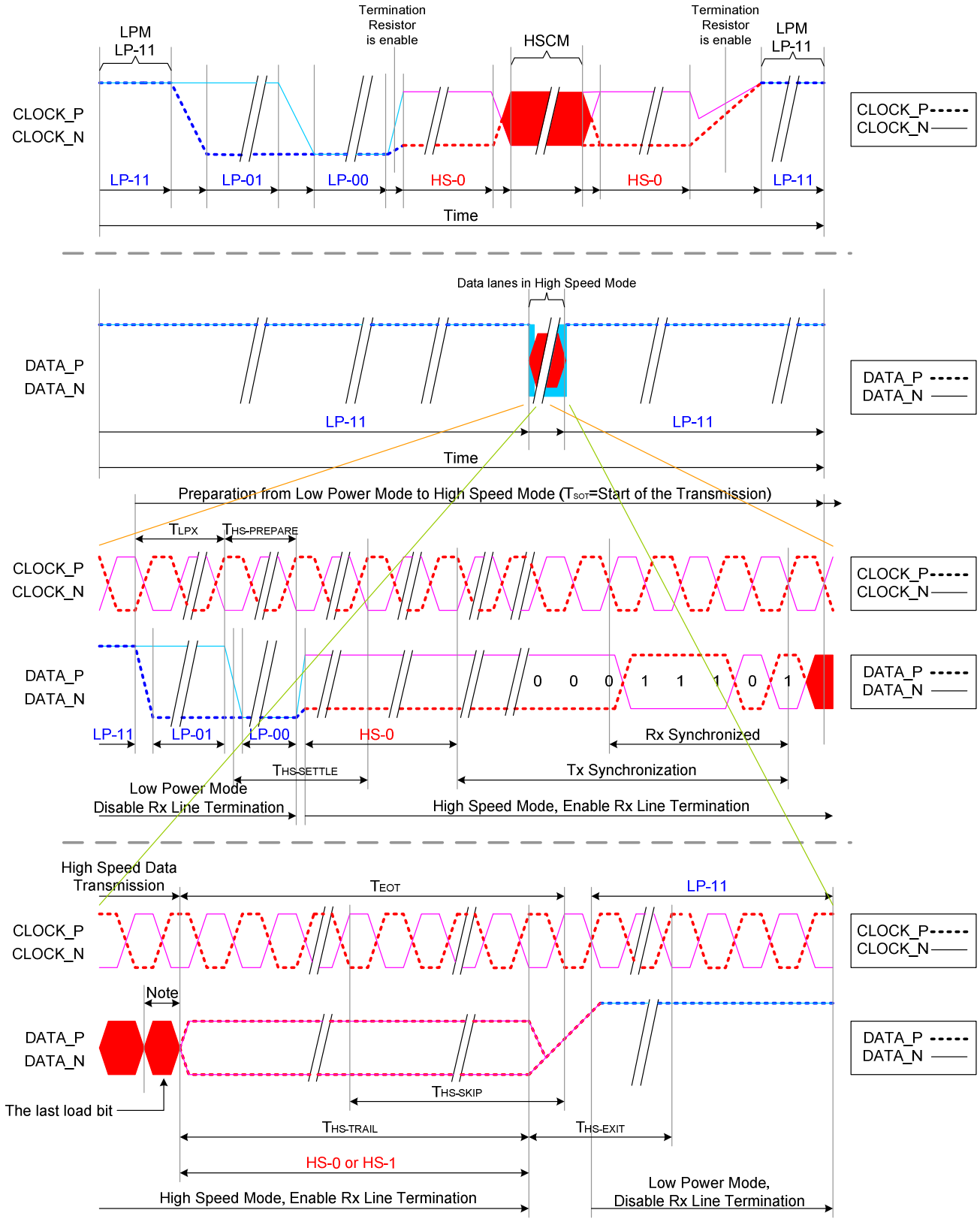


The mode change is also illustrated below.



The high speed clock (DSI-CLOCK_P/N) is started before high speed data is sent via DSI-DATA_P/N lanes. The high speed clock continues clocking after the high speed data sending has been stopped. The burst of the high speed clock consists of:

- Even number of transitions
- Start state is HS-0
- End state is HS-0



Notes: 1. If the last load bit is HS-0, the transmitter changes from HS-0 to HS-1.

2. If the last load bit is HS-1, the transmitter changes from HS-1 to HS-0.

7.3.2. Interface Level Communication – Data Lanes

DSI-DATA_P/N Data Lanes can be driven in different modes which are:

- Escape Mode
- High-Speed Data Transmission
- Bus Turnaround Request

These modes and their entering codes are defined on the following table.

Mode	Entering Mode Sequence	Leaving Mode Sequence
Escape Mode	LP-11 → LP-10 → LP-00 → LP-01 → LP-00	LP-00 → LP-10 → LP-11 (Mark-1)
High-Speed Data Transmission	LP-11 → LP-01 → LP-00 → HS-0	(HS-0 or HS-1) → LP-11
Bus Turnaround Request	LP-11 → LP-10 → LP-00 → LP-10 → LP-00	Hi-Z

7.3.2.1. Escape Modes

Data lanes (DSI-DATA_P/N) can be used in different Escape Modes when data lanes are in Low Power (LP) mode.

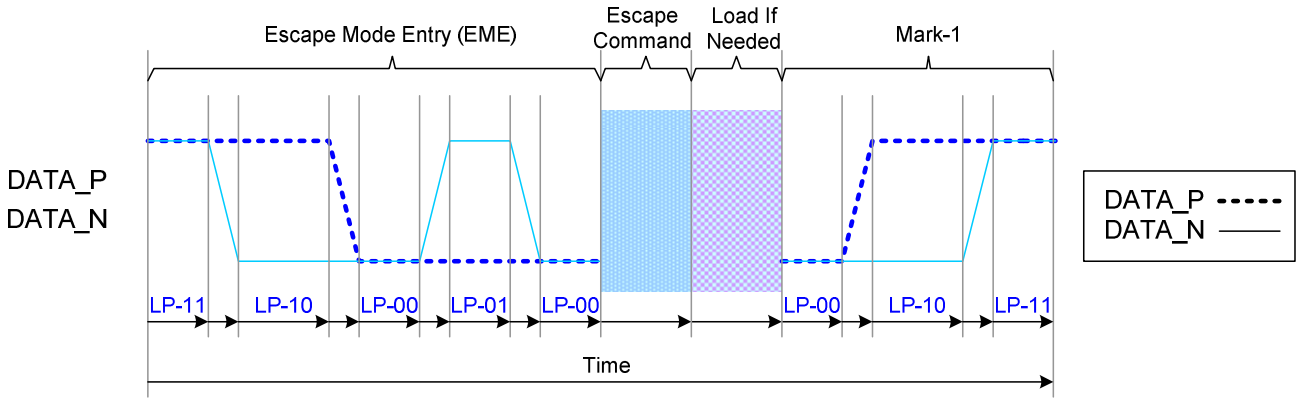
These Escape Modes are used to:

- Send “Low-Power Data Transmission” (LPDT) e.g. from the MCU to ILI9486,
- Drive data lanes to “Ultra-Low Power State” (ULPS),
- Indicate “Remote Application Reset” (RAR), which is resetting ILI9486,
- • Indicate “Tearing Effect” (TEE), which is used for a TE line event from ILI9486 to the MCU,
- Indicate “Acknowledge” (ACK), which is used for a non-error event from ILI9486 to the MCU.

The basic sequence of the Escape Mode is as follow

- Start: LP-11
- Escape Mode Entry (EME): LP-11 =>LP-10 =>LP-00 =>LP-01 =>LP-00
- Escape Command (EC), which is coded, when one of the data lanes is changing from low-to-high-to-low then this changed data lane is presenting a value of the current data bit (DSI-DATA_P = 1, DSI-DATA_N- = 0) e.g. When DSI-DATA_N is changing from low-to-high-to-low, the receiver is latching a data bit, which value is logical 0. The receiver is using this low-to-high-to-low transition for its internal clock.
- A load if it is needed
- Exit Escape (Mark-1) LP-00 =>LP-10 =>LP-11
- End: LP-11

This basic construction is illustrated below:



There are a total of eight Escape Command(EC) divided into two types, Modes and Triggers(see below table),

An example of a Mode type Escape Command is “Ultra-Low Power Mode” where the MCU instructs the display module to enter it’s Ultra-Low Power Mode.

An example of Trigger type Escape Command is ‘Tearing Effect’. In this case the MCU has already instructed The display module to provide this trigger and is waiting for the reponse. The display module then sends a TE Trigger(TEE) on the next V-sync event.

Escape commands are defined on the next table.

Escape command	Command Type Mode / Trigger	Entry command Pattern (First ➔ Last Bit Transmitted)
Low-Power Data Transmission	Mode	1110 0001 b
Ultra-Low Power Mode	Mode	0001 1110 b
Undefined-1, Note	Mode	1001 1111 b
Undefined-2, Note	Mode	1101 1110 b
Remote Application Reset	Trigger	0110 0010 b
Tearing Effect	Trigger	0101 1101 b
Acknowledge	Trigger	0010 0001 b
Uknown-5, Note	Trigger	1010 0000 b

Note: This Escape command support has not been implemented on ILI9486.

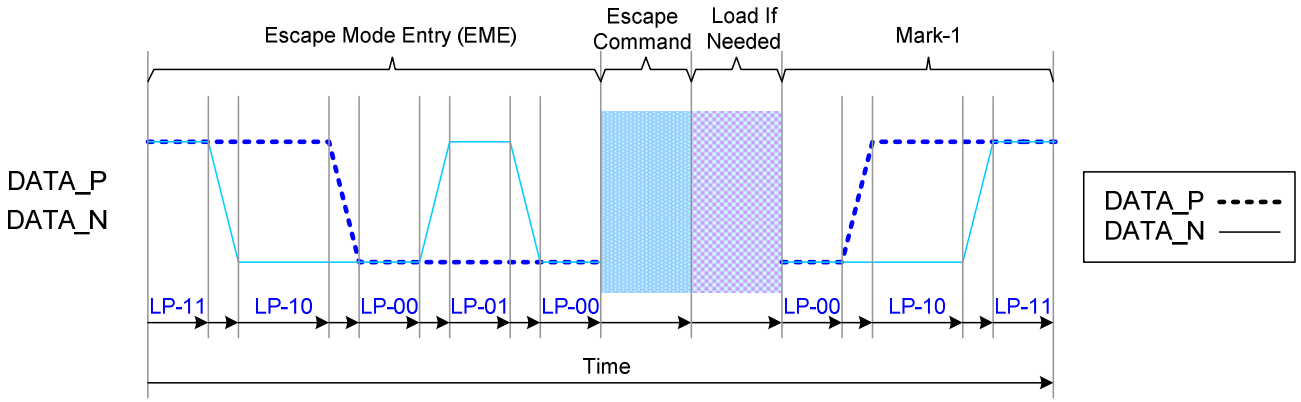
7.3.2.1.1. Low-Power Data Transmission (LPDT)

The MCU can send data to ILI9486 in Low-Power Data Transmission (LPDT) mode when data lanes are entering in Escape Mode and Low-Power Data Transmission (LPDT) command has been sent to ILI9486. ILI9486 is also using the same sequence when it is sending data to the MCU.

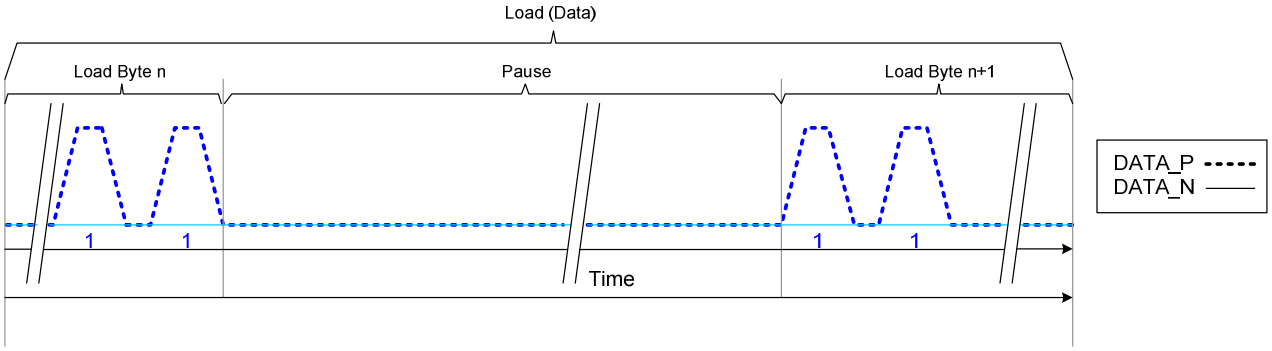
The Low Power Data Transmission (LPDT) is using a following sequence:

- Start: LP-11
- Escape Mode Entry (EME): LP-11 =>LP-10 =>LP-00 =>LP-01 =>LP-00
- Low-Power Data Transmission (LPDT) command in Escape Mode: 1110 0001 (First to Last bit)
- Load (Data):
  - One or more bytes (8 bit)
  - Data lanes are in pause mode when data lanes are stopped (Both lanes are low) between bytes
- Mark-1: LP-00 =>LP-10 =>LP-11
- End: LP-11

This sequence is illustrated for reference purposes below:



Note: Load (Data) is presenting that the first bit is logical '1' in this example.



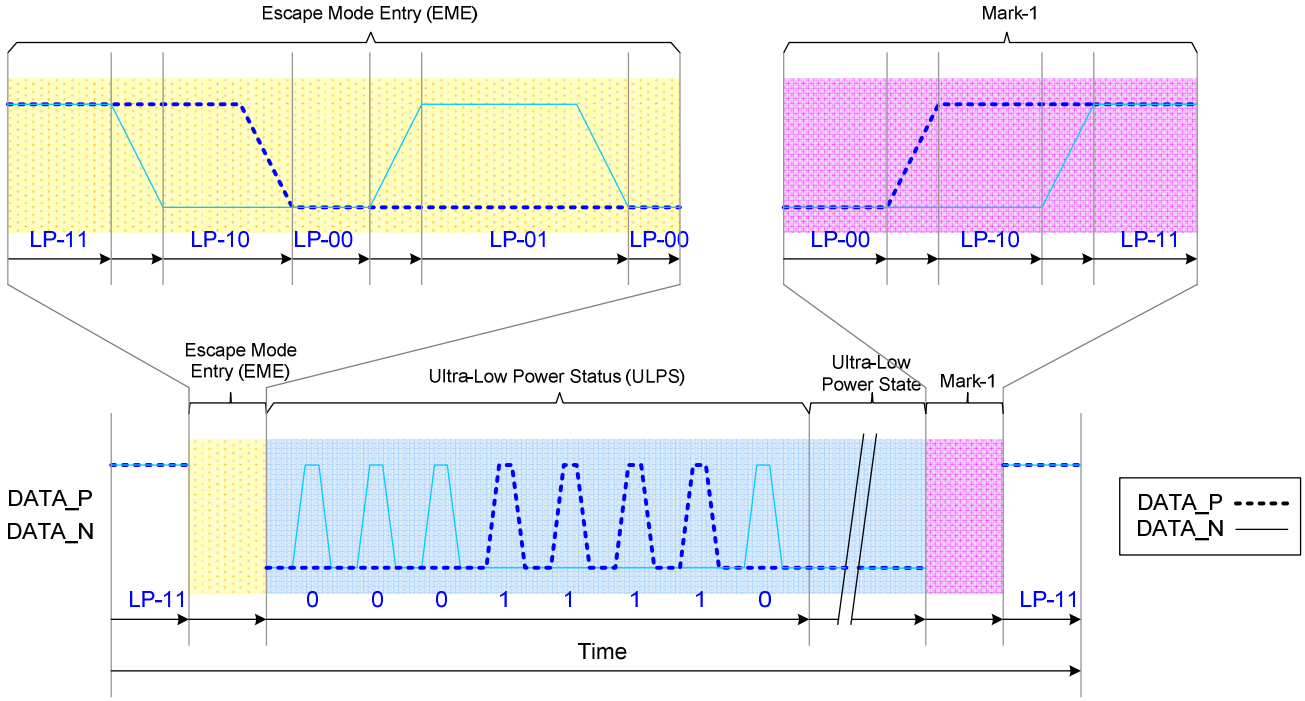
7.3.2.1.2. Ultra-Low Power State (ULPS)

The MCU can force data lanes in Ultra-Low Power State (ULPS) mode when data lanes are entering in Escape Mode.

The Ultra-Low Power State (ULPS) is using a following sequence:

- Start: LP-11
- Escape Mode Entry (EME): LP-11 =>LP-10 =>LP-00 =>LP-01 =>LP-00
- Ultra-Low Power State (ULPS) command in Escape Mode: 0001 1110 (First to Last bit)
- Ultra-Low Power State (ULPS) when the MCU is keeping data lanes low
- Mark-1: LP-00 =>LP-10 =>LP-11
- End: LP-11

This sequence is illustrated for reference purposes below:



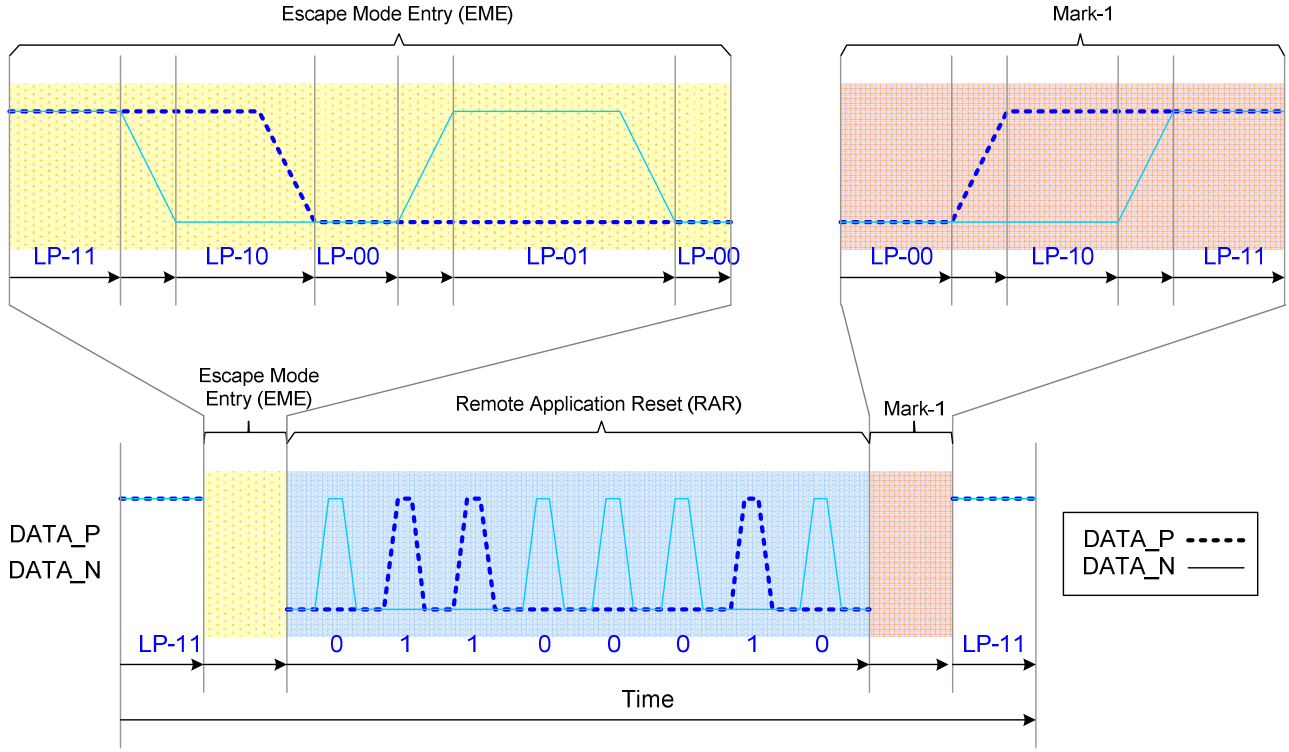
7.3.2.1.3. Remote Application Reset (RAR)

The MCU can inform to ILI9486 that it should be reset in Remote Application Reset (RAR) trigger when data lanes are entering in Escape Mode.

The Remote Application Reset (RAR) is using a following sequence:

- Start: LP-11
- Escape Mode Entry (EME): LP-11 =>LP-10 =>LP-00 =>LP-01 =>LP-00
- Remote Application Reset (RAR) command in Escape Mode: 0110 0010 (First to Last bit)
- Mark-1: LP-00 =>LP-10 =>LP-11
- End: LP-11

This sequence is illustrated for reference purposes below:



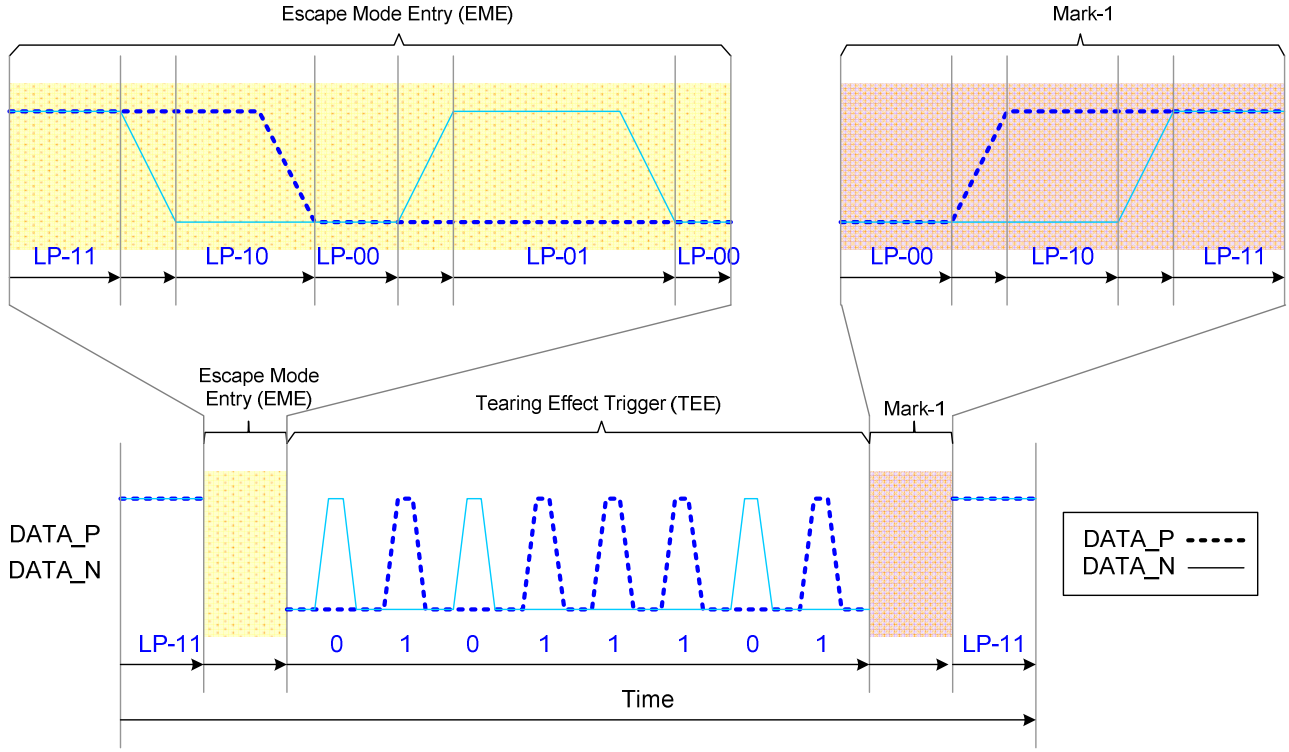
7.3.2.1.4. Tearing Effect (TEE)

ILI9486 can inform to the MCU when a tearing effect event (New V-synch) has been happen on the display module by Tearing Effect (TEE).

The Tearing Effect (TEE) is using a following sequence:

- Start: LP-11
- Escape Mode Entry (EME): LP-11 =>LP-10 =>LP-00 =>LP-01 =>LP-00
- Tearing Effect (TEE) trigger in Escape Mode: 0101 1101 (First to Last bit)
- Mark-1: LP-00 =>LP-10 =>LP-11
- End: LP-11

This sequence is illustrated for reference purposes below:



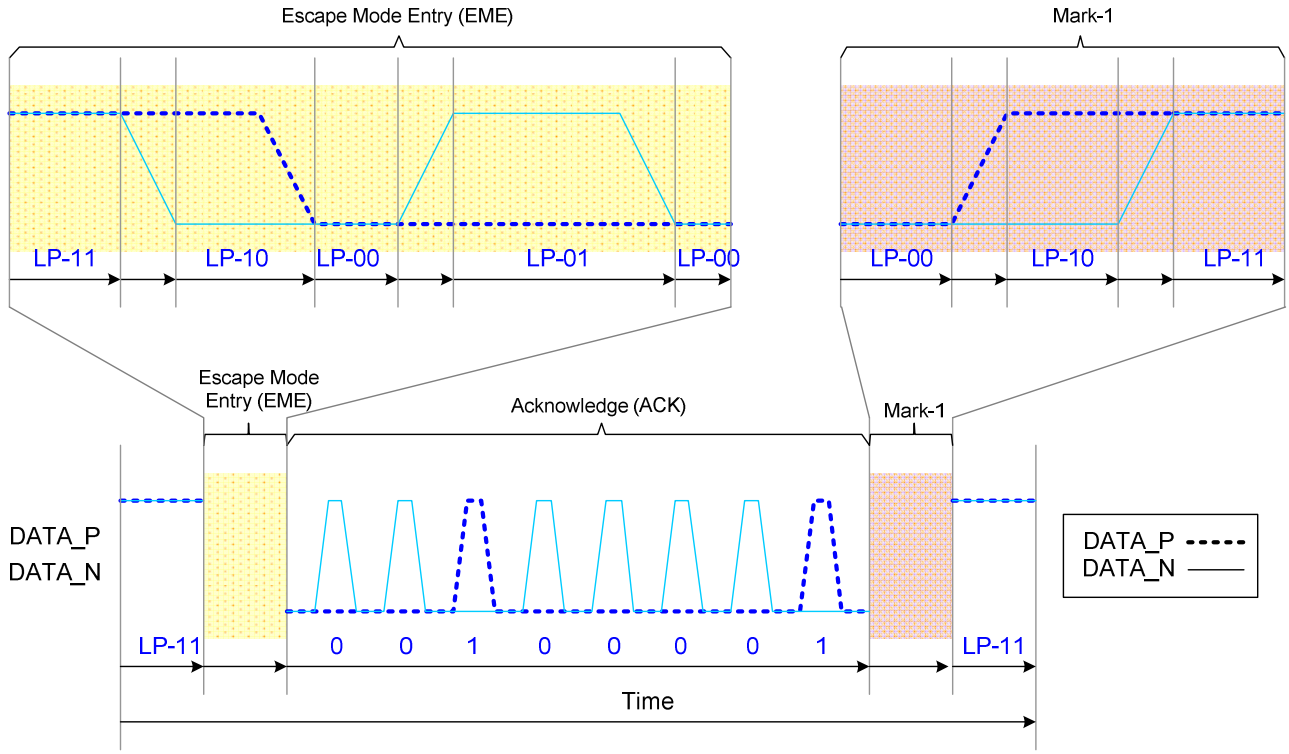
7.3.2.1.5. Acknowledge (ACK)

ILI9486 can inform to the MCU when an error has not recognized on it by Acknowledge (ACK).

The display module is sending the Acknowledge (ACK) what is using a following sequence:

- Start: LP-11
- Escape Mode Entry (EME): LP-11 =>LP-10 =>LP-00 =>LP-01 =>LP-00
- Acknowledge (ACK) command in Escape Mode: 0010 0001 (First to Last bit)
- Mark-1: LP-00 =>LP-10 =>LP-11
- End: LP-11

This sequence is illustrated for reference purposes below:



7.3.2.2. High-Speed Data Transmission (HSDT)

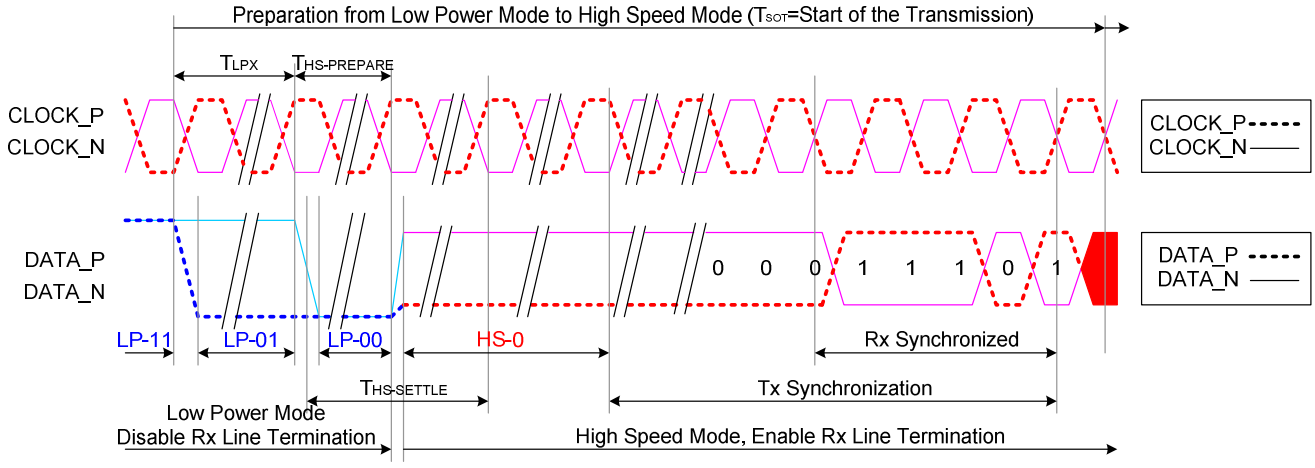
7.3.2.2.1. Entering High-Speed Data Transmission (T_{SOT} of HSDT)

ILI9486 is entering High-Speed Data Transmission (HSDT) when Clock lanes DSI-CLOCK_P/N have already been entered in the High-Speed Clock Mode (HSCM) by the MCU.

Data lanes DSI-DATA_P/N of ILI9486 are entering (T_{SOT}) in the High-Speed Data Transmission (HSDT) as follows

- Start: LP-11
- HS-Request: LP-01
- HS-Settle: LP-00 => HS-0 (Rx: Lane Termination Enable)
- Rx Synchronization: 011101 (Tx (= MCU) Synchronization: 0001 1101)
- End: High-Speed Data Transmission (HSDT) – Ready to receive High-Speed Data Load

This same entering High-Speed Data Transmission (T_{SOT} of HSDT) sequence is illustrated below:



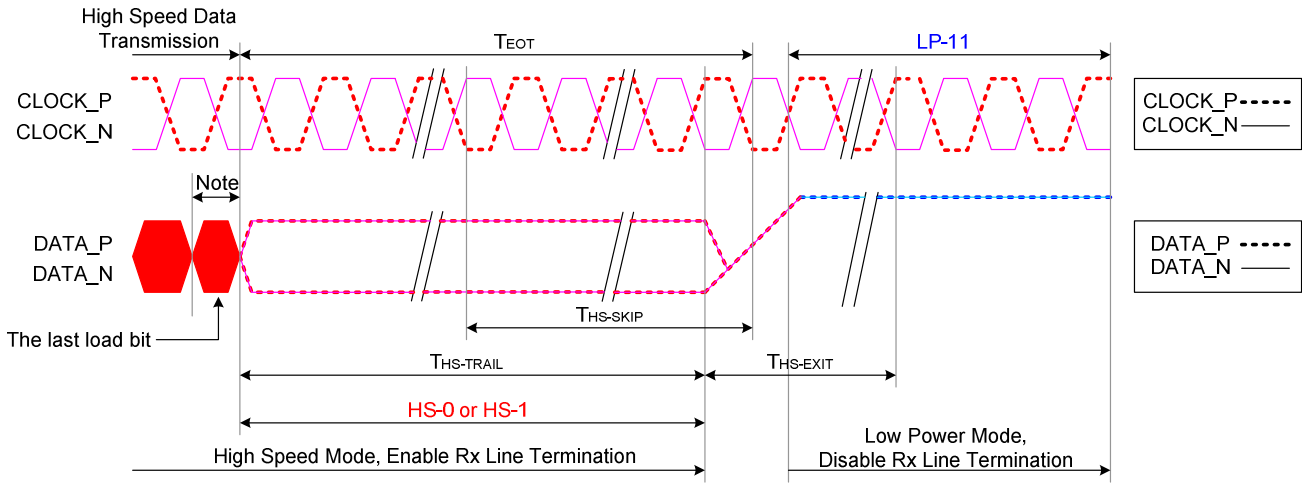
7.3.2.2.2. Leaving High-Speed Data Transmission (T_{EOT} of HSDT)

ILI9486 is leaving the High-Speed Data Transmission (T_{EOT} of HSDT) when Clock lanes DSI-CLOCK_P/N are in the High-Speed Clock Mode (HSCM) by the MCU and this HSCM is kept until data lanes DSI-DATA_P/N are in LP-11 mode.

Data lanes DSI-DATA_P/N of the display module are leaving from the High-Speed Data Transmission (T_{EOT} of HSDT) as follows

- Start: High-Speed Data Transmission (HSDT)
- Stops High-Speed Data Transmission
  - MCU changes to HS-1, if the last load bit is HS-0
  - MCU changes to HS-0, if the last load bit is HS-1
- End: LP-11 (Rx: Lane Termination Disable)

This same leaving High-Speed Data Transmission (T_{EOT} of HSDT) sequence is illustrated below



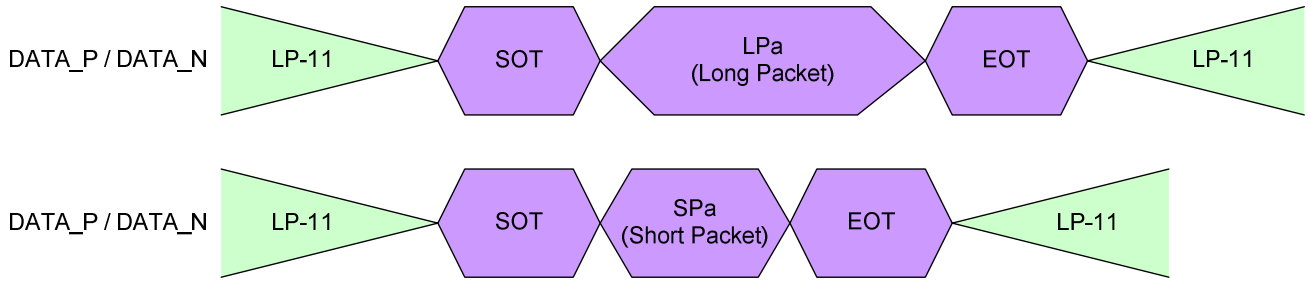
Note: 1. If the last load bit is HS-0, the transmitter changes from HS-0 to HS-1.

2. If the last load bit is HS-1, the transmitter changes from HS-1 to HS-0.

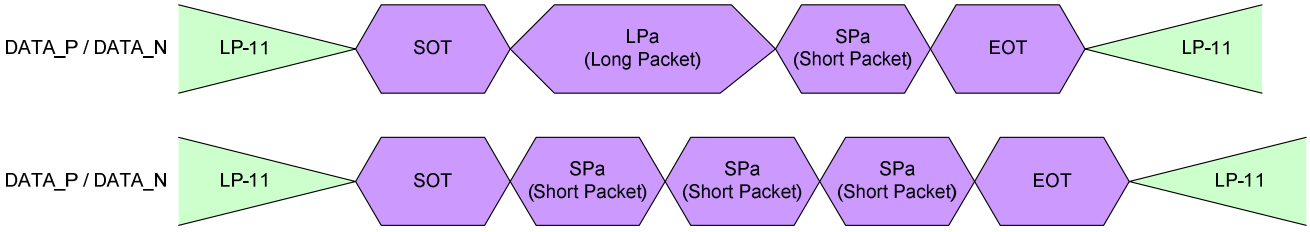
7.3.2.2.3. Burst of the High-Speed Data Transmission (HSDT)

The burst of the high-speed data transmission (HSDT) can consist of one data packet or several data packets. These data packets can be Long (LPa) or Short (SPa) packets. These packets are defined on chapter "7.3.3.1 Short Packet (SPa) and Long Packet (LPa) Structures".

The single packet in High-Speed Data Transmission is illustrated for reference purposes below:



The multiple packets in High-Speed Data Transmission is illustrated for reference purposes below:



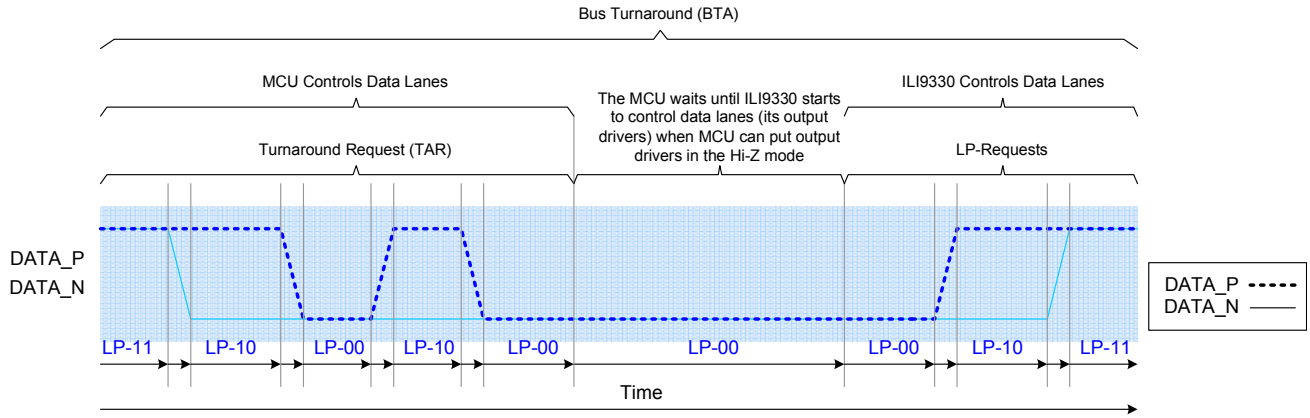
Abbreviation	Explanation
EOT	End of the Transmission
LPa	Long Packet
LP-11	Low Power Mode, Both of Data lanes are '1's (Stop Mode)
SPa	Short Packet
SOT	Start of the Transmission

7.3.2.3. Bus Turnaround (BTA)

The MCU or ILI9486, which is controlling DSI-DATA_P/N Data Lanes, can start a bus turnaround procedure when it wants information from a receiver, which can be the MCU or ILI9486. The MCU and ILI9486 are using the same sequence when this bus turnaround procedure is used. This sequence is described for reference purposes, when the MCU wants to do the bus turnaround procedure to ILI9486, as follows.

- Start (MCU): LP-11
- Turnaround Request (MCU): LP-11 =>LP-10 =>LP-00=>LP-10=>LP-00
- The MCU waits until ILI9486 is starting to control DSI-DATA_P/N data lanes and the MCU stops to control DSI-DATA_P/N data lanes (= High-Z)
- ILI9486 changes to the stop mode: LP-00 =>LP-10 =>LP-11

The same bus turnaround procedure (From the MCU to ILI9486) is illustrated below :



7.3.3. Packet Level Communication

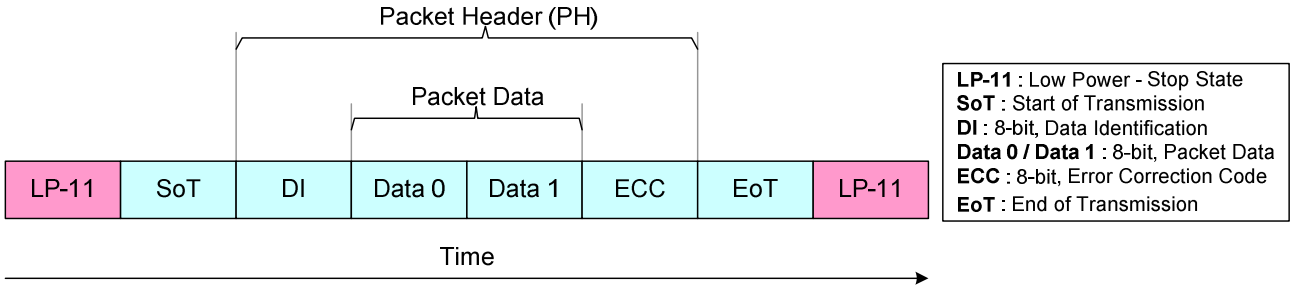
7.3.3.1. Short Packet and Long Packet Structures

Short Packet (SPa) and Long Packet (LPa) are always used when data transmission is done in Low Power Data Transmission (LPDT) or High-Speed Data Transmission (HSDT) modes.

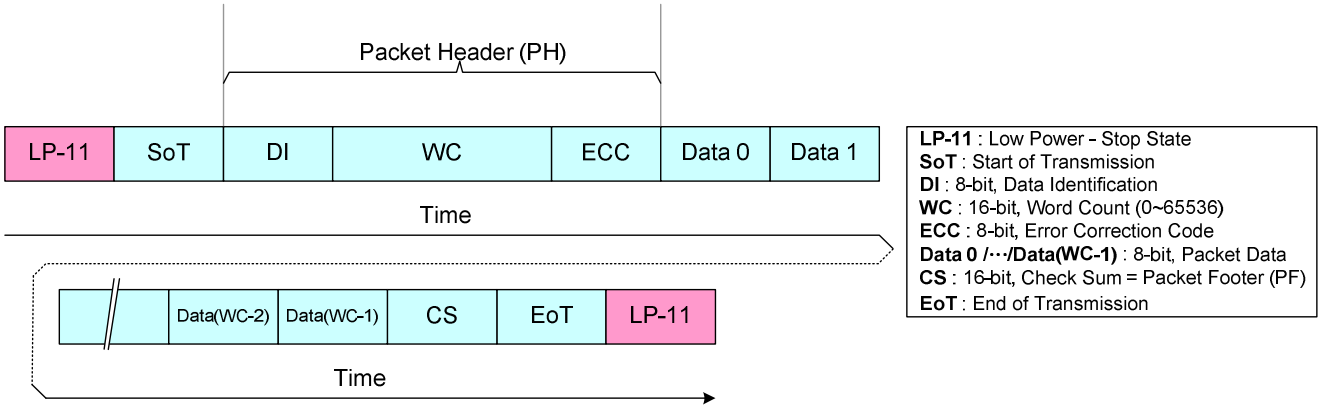
The lengths of the packets are

- Short Packet (SPa): 4 bytes
- Long Packet (LPa): From 6 to 65,541 bytes

The type (SPa or LPa) of the packet can be recognized from their package headers (PH). The Short Packet structure is illustrated as below:



The Long Packet structure is illustrated as below:



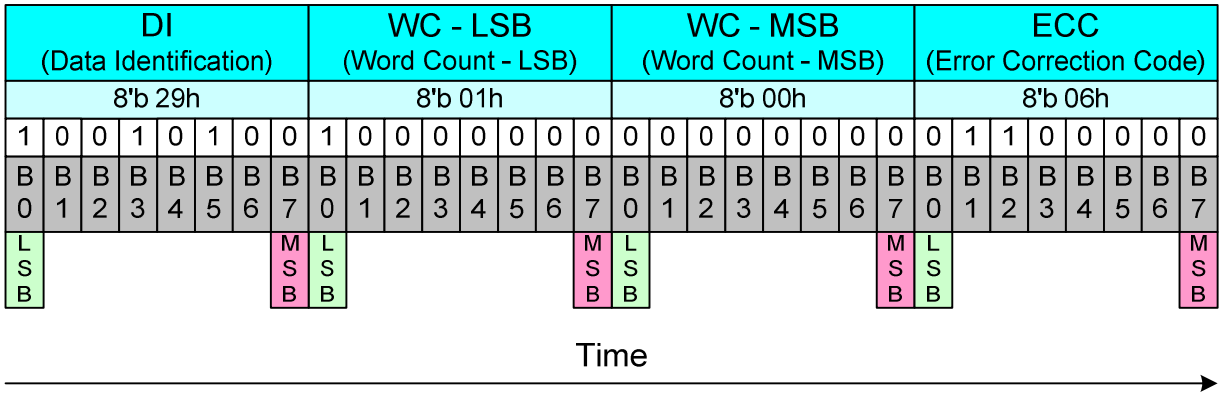
The other possibility is that there is not needed SoT, EoT and LP-11 between packets if packets have sent in multiple packet format e.g.

- LP-11 =>SoT =>SPa =>LPa =>SPa =>SPa =>EoT =>LP-11
- LP-11 =>SoT =>SPa =>SPa =>SPa =>EoT =>LP-11
- LP-11 =>SoT =>LPa =>LPa =>LPa =>EoT =>LP-11

7.3.3.1.1. Bit Order of the Byte on Packets

The bit order of the byte, what is used on packets, is that the Least Significant Bit (LSB) of the byte is sent in the first and the Most Significant Bit (MSB) of the byte is sent in the last.

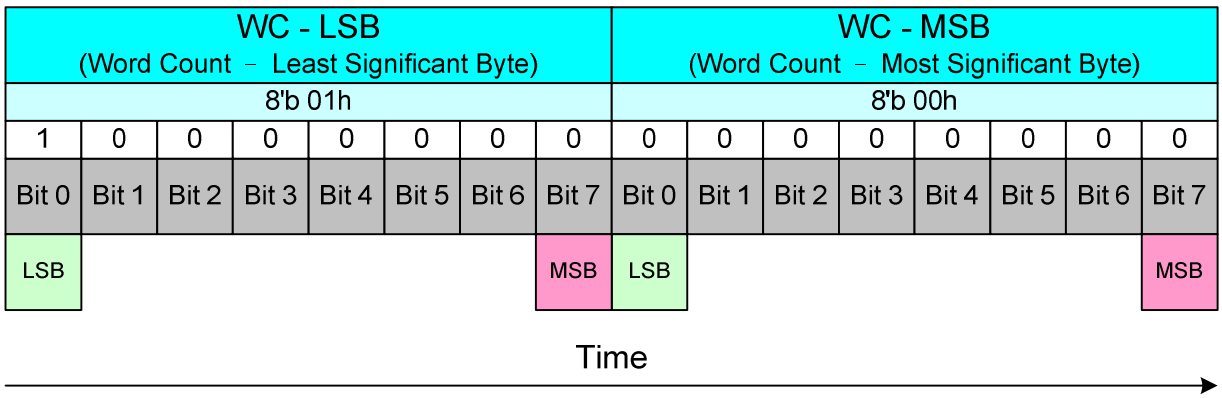
This same order is illustrated for reference purposes below.



7.3.3.1.2. Byte Order of the Multiple Byte Information on Packets

Byte order of the multiple bytes information, what is used on packets, is that the Least Significant (LS) Byte of the information is sent in the first and the Most Significant (MS) Byte of the information is sent in the last e.g. Word Count (WC) consists of 2 bytes (16 bits) when the LS byte is sent in the first and the MS byte is sent in the last.

This same order is illustrated for reference purposes below.

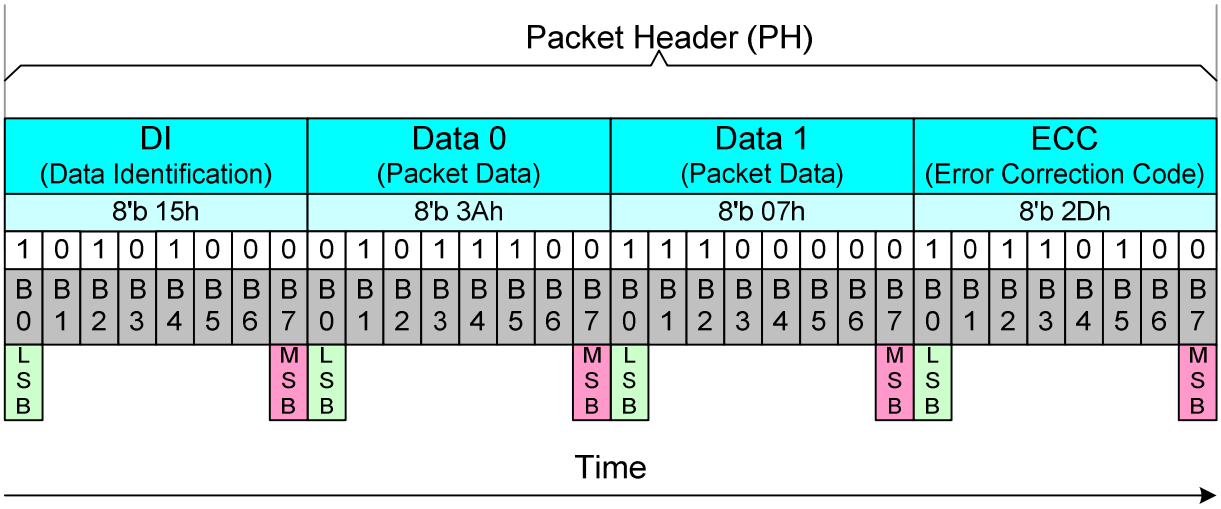


7.3.3.1.3. Packet Header (PH)

The packet header is always consisting of 4 bytes. The content of these 4 bytes are different if it is used to Short Packet (SPa) or Long Packet (LPa).

Short Packet (SPa):

- 1st byte: Data Identification (DI) => Identification that this is Short Packet (SPa)
- 2nd and 3rd bytes: Packet Data (PD), Data 0 and 1
- 4th byte: Error Correction Code (ECC)

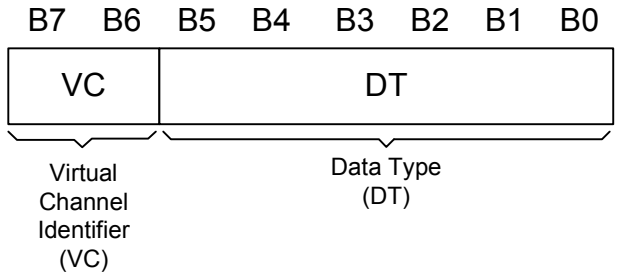


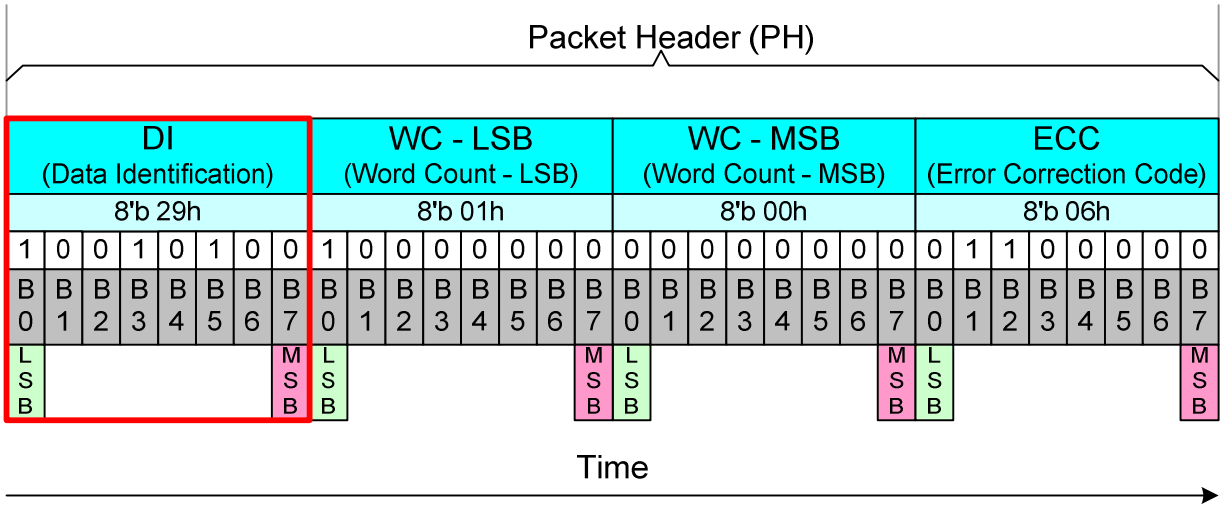
7.3.3.1.3.1. Data Identification (DI)

Data Identification (DI) is a part of Packet Header (PH) and it consists of 2 parts:

- Virtual Channel (VC), 2 bits, DI [7...6]
- Data Type (DT), 6 bits, DI [5…0]

The Data Identification (DI) structure is illustrated on a diagram below.

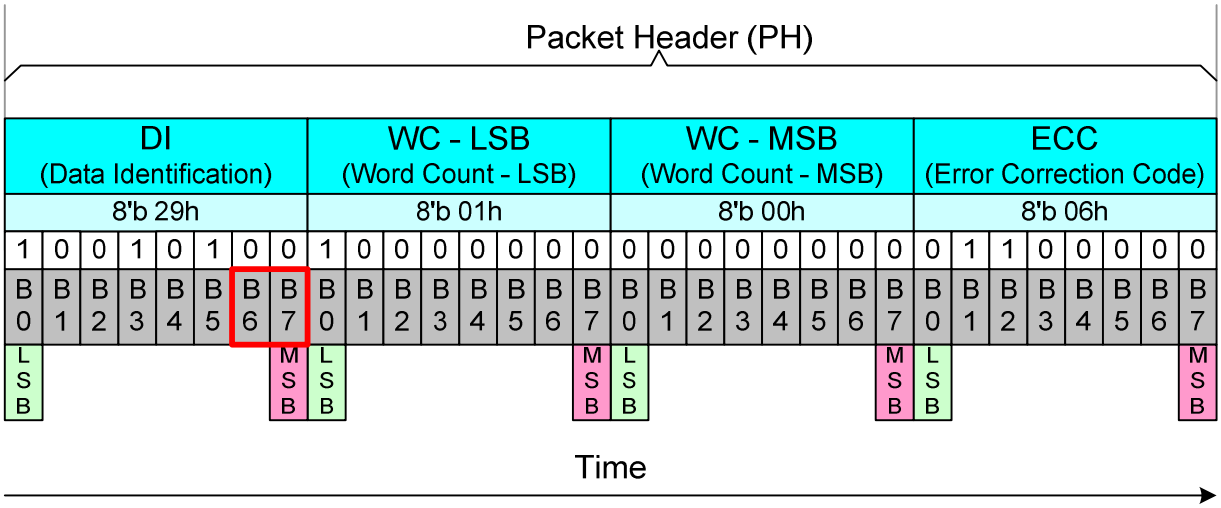




7.3.3.1.3.1.1. Virtual Channel (VC)

A processor may service up to four peripherals with tagged commands or blocks of data, using the Virtual Channel ID field of the header for packets targeted at different peripherals. The Virtual Channel ID enables one serial stream to service two or more virtual peripherals by multiplexing packets onto a common transmission channel. Note that packets sent in a single transmission each have their own Virtual Channel assignment and can be directed to different peripherals.

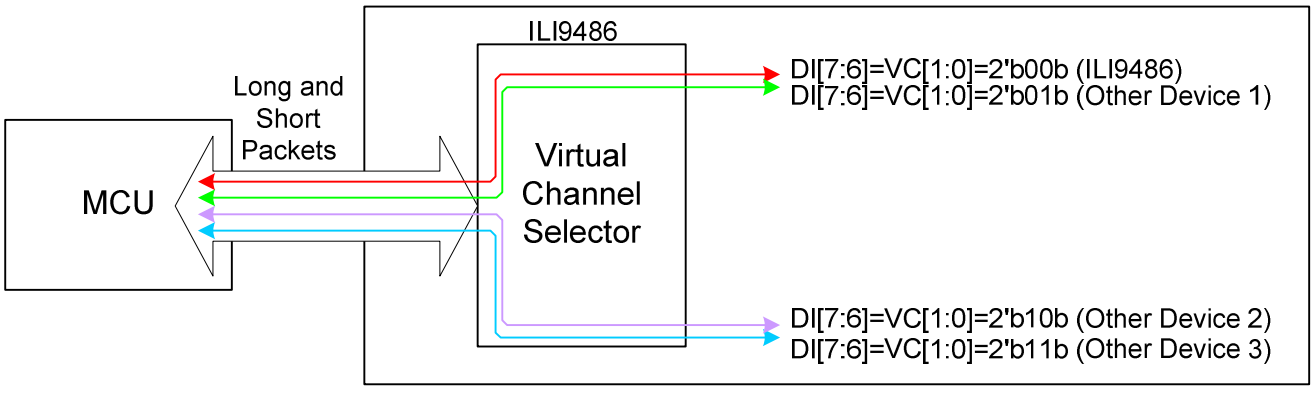
Virtual Channel (VC) is a part of Data Identification (DI [7…6]) structure and it is used to address where a packet is wanted to send from the MCU. Bits of the Virtual Channel (VC) are illustrated for reference purposes below.



Virtual Channel (VC) can address 4 different channels for e.g. 4 different display modules. Devices are using the same virtual channel what the MCU is using to send packets to them e.g.

- The MCU is using the virtual channel 0 when it sends packets to this display module
- This display module is also using the virtual channel 0 when it sends packets to the MCU

This functionality is illustrated below.



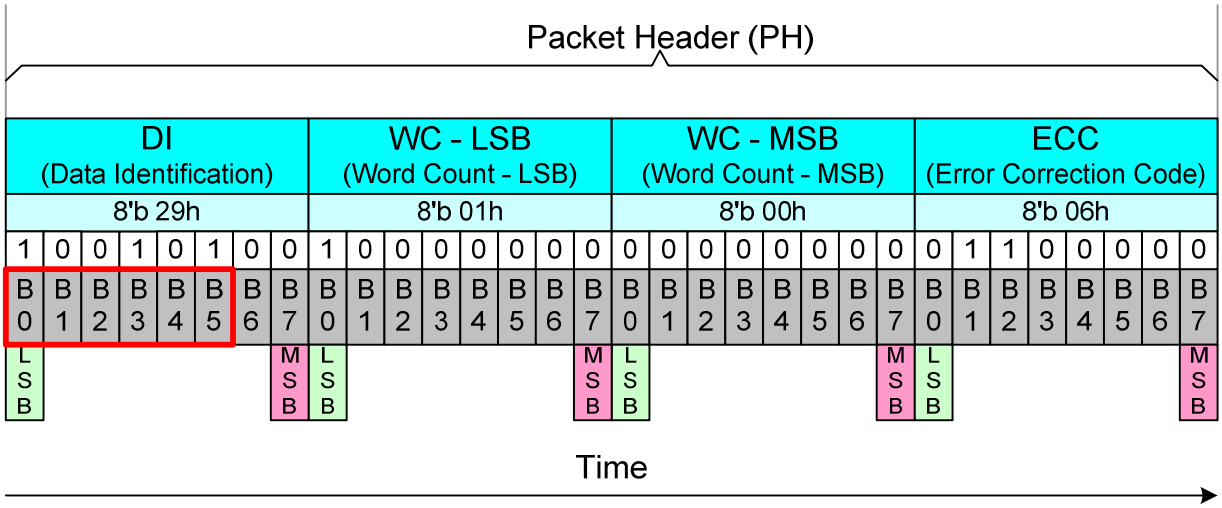
Virtual Channel (VC) is always 0 (DI[7..6]=VC[1..0]=00_b) when the MCU is sending “End of Transmission Packet” to the display module.

7.3.3.1.3.1.2. Data Type (DT)

The Data Type field specifies if the packet is a Long or Short packet type and the packet format. The Data Type field, along with the Word Count field for Long packets, informs the receiver of how many bytes to expect in the remainder of the packet. This is necessary because there are no special packet start / end sync codes to indicate the beginning and end of a packet. This permits packets to convey arbitrary data, but it also requires the packet header to explicitly specify the size of the packet.

When the receiving logic has counted down to the end of a packet, it shall assume the next data is either the header of a new packet or the EoT (End of Transmission) sequence.

Data Type (DT) is a part of Data Identification (DI [5…0]) structure and it is used to define a type of the used data on a packet. Bits of the Data Type (DT) are illustrated for reference purposes below.



This Data Type (DT) also defines what the used packet is: Short Packet (SPa) or Long Packet (LPa). Data Types (DT) are different from the MCU to the display module (or other devices) and vice versa. These Data Type (DT) are defined on tables below

From the MCU to ILI9486									
Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Hex	Description	Short/Long Packet	Abbreviation
0	0	1	0	0	0	08	End of Transmission Packet, Note1	SPa (Short Packet)	EoTP
0	0	0	1	0	1	05	DCS Write, No Parameter	SPa (Short Packet)	DCSWN-S
0	1	0	1	0	1	15	DCS Write, 1 Parameter	SPa (Short Packet)	DCSW1-S
0	0	0	1	1	0	06	DCS Read, No Parameter	SPa (Short Packet)	DCSRN-S
1	1	0	1	1	1	37	Set Maximum Return Packet Size	SPa (Short Packet)	SMRPS-S
0	0	1	0	0	1	09	Null Packet, No Data, Note2	LPa (Long Packet)	NP-L
1	1	1	0	0	1	39	DCS Write Long	LPa (Long Packet)	DCSW-L

Notes: 1. This can be used when the MCU wants to secure that there is the end of the transmission in High Speed Data Transferring (HSDT) mode.

2. This can be used when data lanes are wanted to keep in High Speed Data Transferring (HSDT) Mode.

3. The receiver is ignored other Data Type (DT) if they are not defined on tables.

From ILI9486 to the MCU									
Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Hex	Description	Short/Long Packet	Abbreviation
0	0	0	0	1	0	02	Acknowledge with Error Report	SPa (Short Packet)	AwER
0	1	1	1	0	0	1C	DCS Read Long Response	LPa (Long Packet)	DCSRR-L
1	0	0	0	0	1	21	DCS Read Short Response, 1 byte returned	SPa (Short Packet)	DCSRR1-S
1	0	0	0	1	0	22	DCS Read Short Response, 2 byte returned	SPa (Short Packet)	DCSRR2-S

Notes: 1. The receiver is ignored other Data Type (DT) if they are not defined on tables.

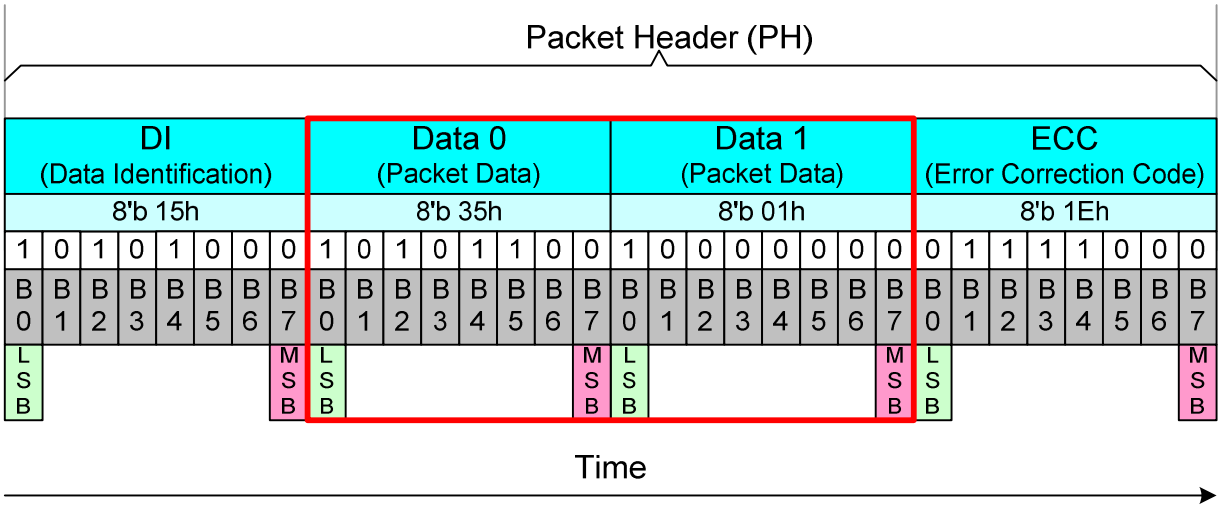
7.3.3.1.3.2. Packet Data on the Short Packet

Packet Data (PD) of the Short Packet (SPa) is defined after Data Type (DT) of the Data Identification (DI) has indicated that Short Packet (SPa) is wanted to send. Packet Data (PD) of the Short Packet (SPa) consists of 2 data bytes: Data 0 and Data 1. Packet Data (PD) sending order is that Data 0 is sent in the first and the Data 1 is sent in the last. Bits of Data 1 are set to '0' if the information length is 1 byte.

Packet Data (PD) of the Short Packet (SPa), when the length of the information is 1 or 2 bytes are illustrated for reference purposes below, when Virtual Channel (VC) is 0.

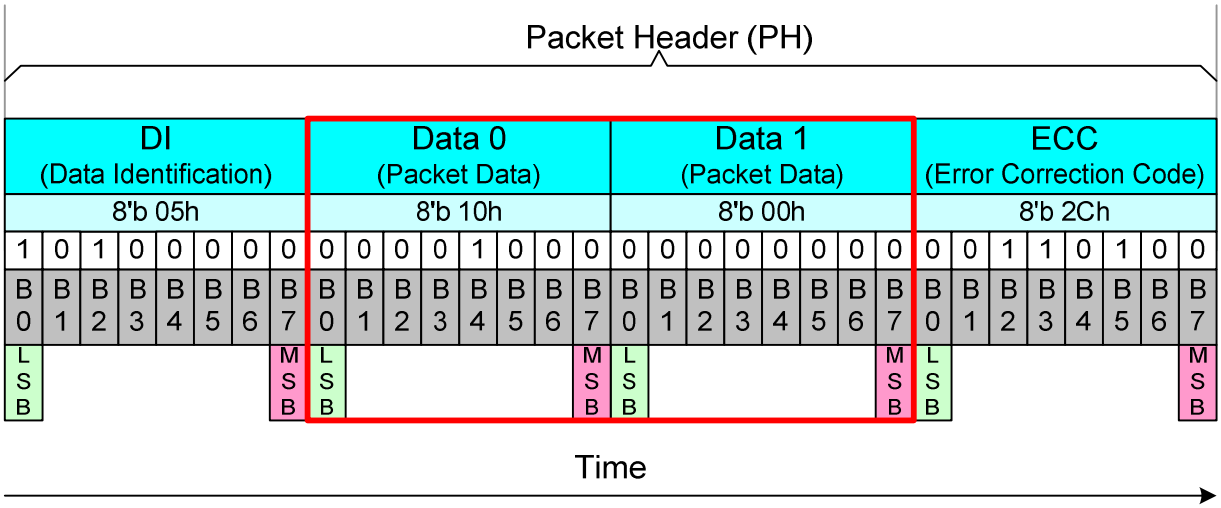
Packet Data (PD) information:

- Data 0: 35hex (Display Command Set (DCS) with 1 Parameter => DI (Data Type (DT)) = 15hex)
- Data 1: 01hex (DCS's parameter)



Packet Data (PD) information:

- Data 0: 10hex (DCS without parameter => DI (Data Type (DT)) = 05hex)
- Data 1: 00hex (Null)



7.3.3.1.3.3. Word Count on the Long Packet

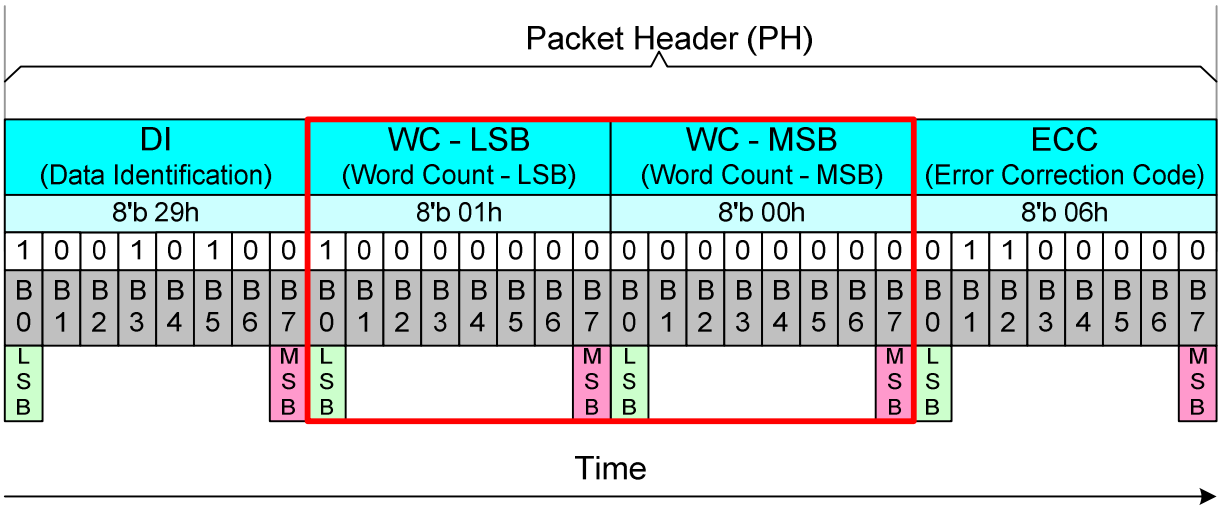
Word Count (WC) of the Long Packet (LPa) is defined after Data Type (DT) of the Data Identification (DI) has indicated that Long Packet (LPa) is wanted to send.

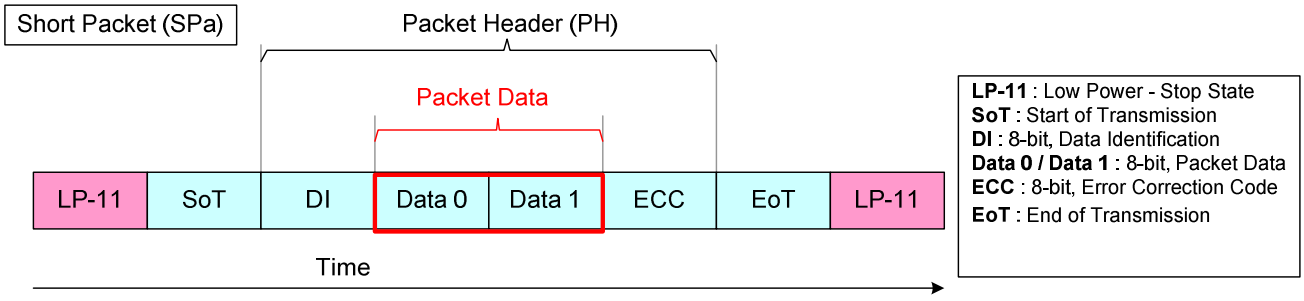
Word Count (WC) indicates a number of the data bytes of the Packet Data (PD) what is wanted to send after Packet Header (PH) versus Packet Data (PD) of the Short Packet (SPa) are placed in the Packet Header (PH).

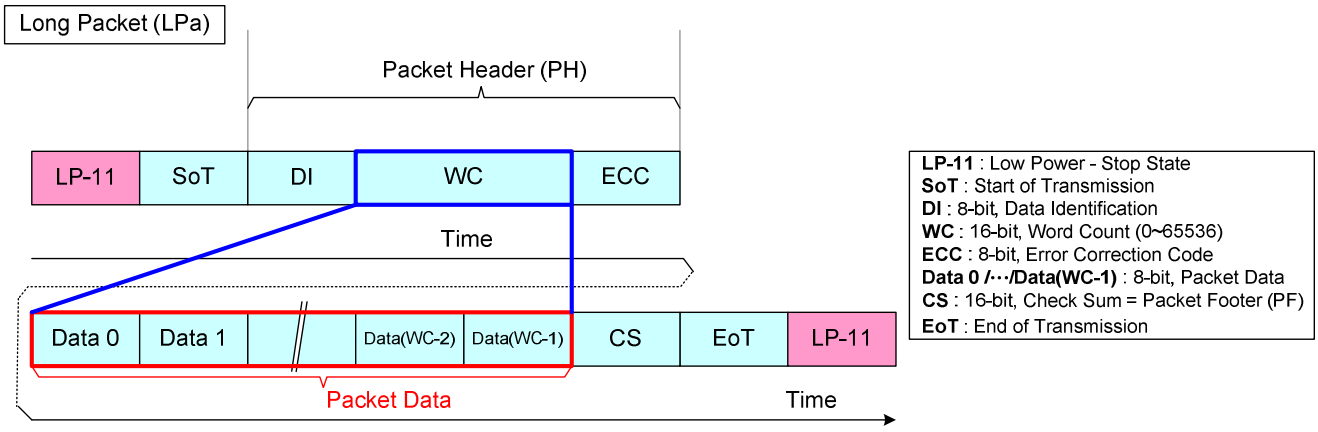
Word Count (WC) of the Long Packet (LPa) consists of 2 bytes.

These 2 bytes of the Word Count (WC) sending order is that the Least Significant (LS) Byte is sent in the first and the Most Significant (MS) Byte is sent in the last.

Word Count (WC) of the Long Packet (LPa) is illustrated for reference purposes below.







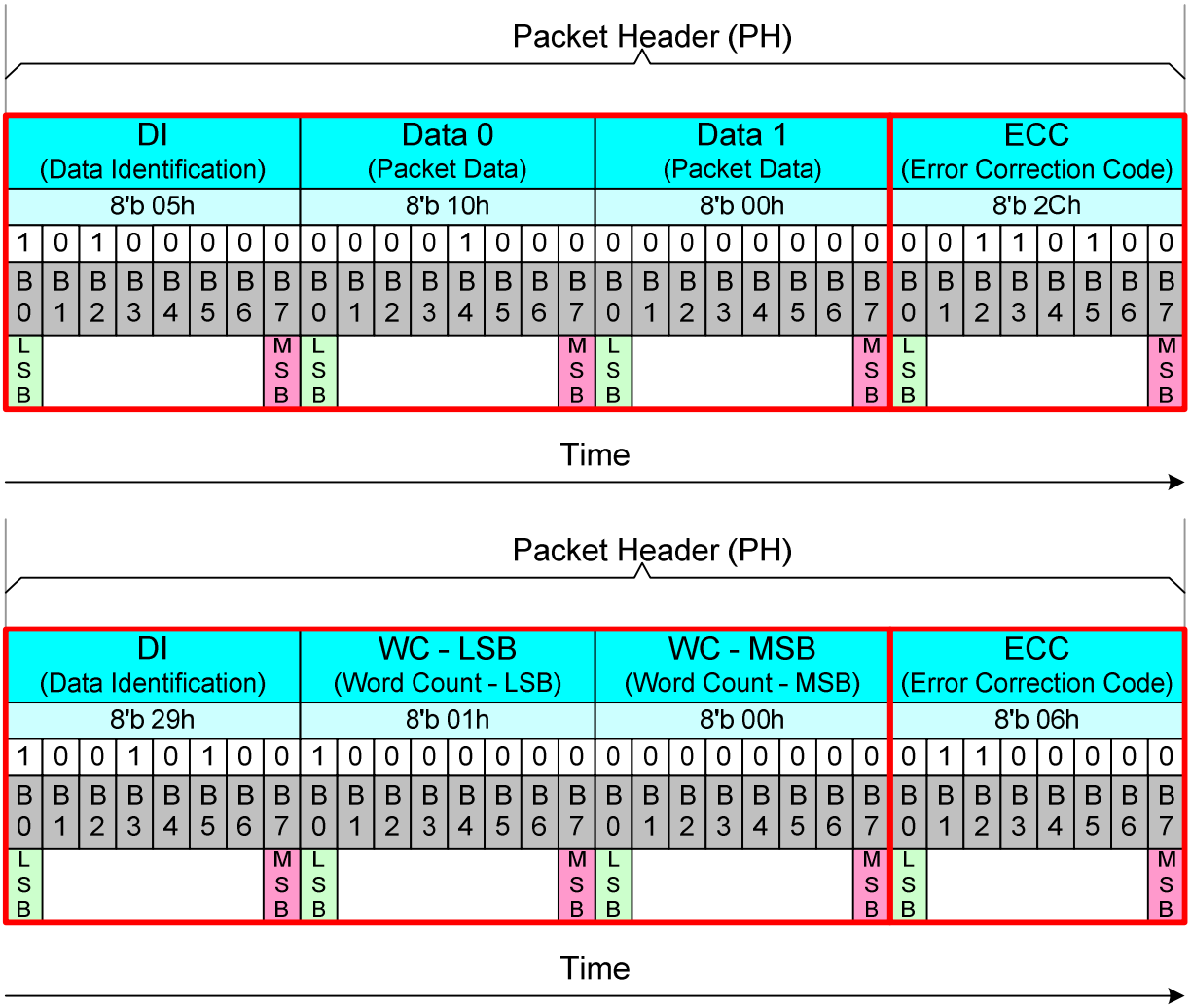
7.3.3.1.3.4. Error Correction Code (ECC)

The Error Correction Code allows single-bit errors to be corrected and 2-bit errors to be detected in the Packet Header. The host processor shall always calculate and transmit an ECC byte and ILI9486 supports ECC in both forward- and reverse-direction communications.

Error Correction Code (ECC) is a part of Packet Header (PH) and its purpose is to identify an error or errors:

- Short Packet (SPa): Data Identification (DI) and Packet Data (PD) bytes (24 bits: D [23…0])
- Long Packet (LPa): Data Identification (DI) and Word Count (WC) bytes (24 bits: D [23…0])

D [23…0] is illustrated for reference purposes below.



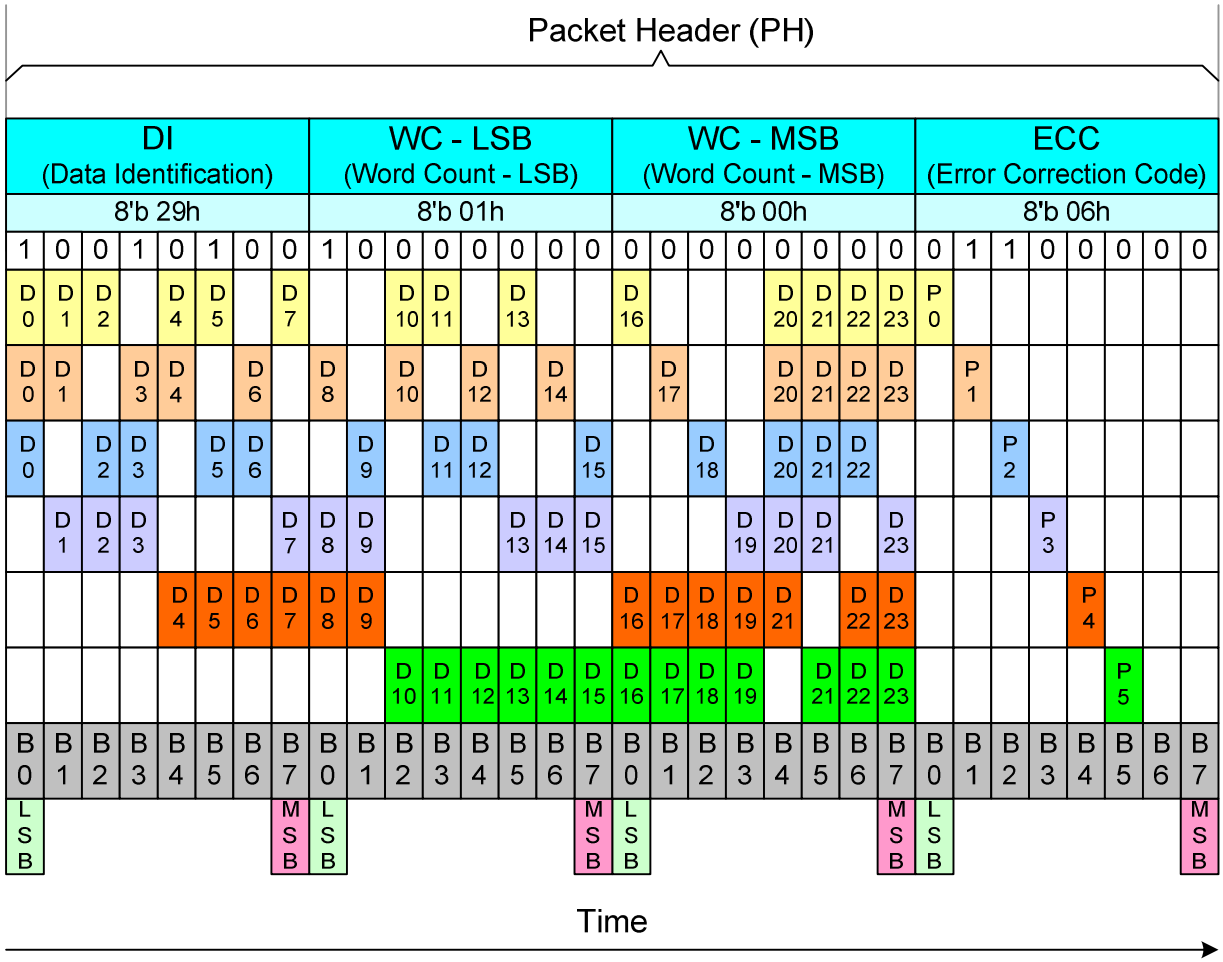
Error Correction Code (ECC) can recognize one error or several errors and makes correction in one bit error case.

Bits (P[7…0]) of the Error Correction Code (ECC) are defined, where the symbol '^' is presenting XOR function (Pn is '1' if there is odd number of '1's and Pn is '0' if there is even number of '1's), as follows.

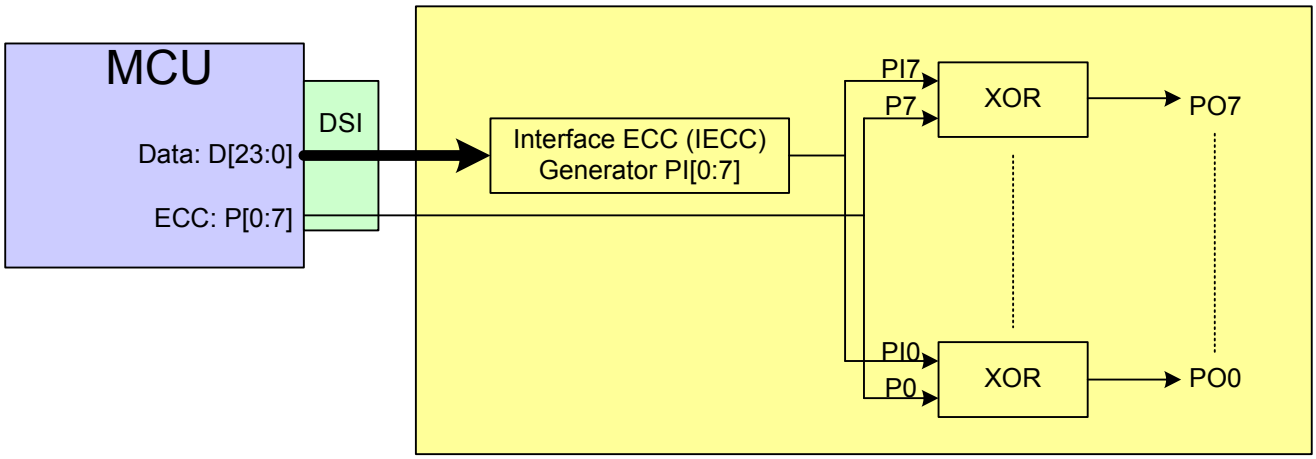
- P7 = 0
- P6 = 0
- P5 = D10^D11^D12^D13^D14^D15^D16^D17^D18^D19^D21^D22^D23
- P4 = D4^D5^D6^D7^D8^D9^D16^D17^D18^D19^D20^D22^D23
- P3 = D1^D2^D3^D7^D8^D9^D13^D14^D15^D19^D20^D21^D23

- P2 = D0^D2^D3^D5^D6^D9^D11^D12^D15^D18^D20^D21^D22
- P1 = D0^D1^D3^D4^D6^D8^D10^D12^D14^D17^D20^D21^D22^D23
- P0 = D0^D1^D2^D4^D5^D7^D10^D11^D13^D16^D20^D21^D22^D23

P7 and P6 are set to '0' because Error Correction Code (ECC) is based on 64 bit value ([D63…0]), but this implementation is based on 24 bit value (D [23…0]). Therefore, there is only needed 6 bits (P [5…0]) for Error Correction Code (ECC).



The transmitter (The MCU or ILI9486) is sending data bits D [23…0] and Error Correction Code (ECC) P [7…0]. The receiver (ILI9486 or the MCU) is calculate an Internal Error Correction Code (IECC) and compares the received Error Correction Code (ECC) and the Internal Error Correction Code (IECC). This comparison is done when each power bit of ECC and IECC have been done XOR function. The result of this function is PO [7…0]. This functionality, where the transmitter is the MCU and the receiver is ILI9486, is illustrated for reference purposes below.



The sent data bits (D[23…0]) and ECC (P[7…0]) are received correctly, if a value of the PO[7…0]) is 00h.

The sent data bits (D[23…0]) and ECC (P[7…0]) are not received correctly, if a value of the PO[7…0]) is not 00h.

ECC P[7:0]	1	1	0	0	0	0	0	0	03h
IECC PI[7:0]	1	1	0	0	0	0	0	0	03h
(ECC) ⊕ (IECC) ➔ PO[7:0]	0	0	0	0	0	0	0	0	=00h ➔ No Error
	LSB							MSB	

ECC P[7:0]	1	1	0	0	0	0	0	0	03h
IECC PI[7:0]	1	1	1	1	0	0	0	0	0Fh
(ECC) ⊕ (IECC) ➔ PO[7:0]	0	0	1	1	0	0	0	0	=0Ch ➔ Error
	LSB							MSB	

The received Error Correction Code (ECC) can be 00h when the Error Correction Code (ECC) functionality is not used for data values D[23…0] on the transmitter side.

The number of the errors (one or more) can be defined when the value of the PO [7…0] is compared to values on the following table.

Data Bit	PO7	PO6	PO5	PO4	PO3	PO2	PO1	PO0	Hex
D[0]	0	0	0	0	0	1	1	1	07h
D[1]	0	0	0	0	1	0	1	1	0Bh
D[2]	0	0	0	0	1	1	0	1	0Dh
D[3]	0	0	0	0	1	1	1	0	0Eh
D[4]	0	0	0	1	0	0	1	1	13h
D[5]	0	0	0	1	0	1	0	1	15h
D[6]	0	0	0	1	0	1	1	0	16h
D[7]	0	0	0	1	1	0	0	1	19h
D[8]	0	0	0	1	1	0	1	0	1Ah
D[9]	0	0	0	1	1	1	0	0	1Ch
D[10]	0	0	1	0	0	0	1	1	23h
D[11]	0	0	1	0	0	1	0	1	25h
D[12]	0	0	1	0	0	1	1	0	26h
D[13]	0	0	1	0	1	0	0	1	29h
D[14]	0	0	1	0	1	0	1	0	2Ah
D[15]	0	0	1	0	1	1	0	0	2Ch
D[16]	0	0	1	1	0	0	0	1	31h
D[17]	0	0	1	1	0	0	1	0	32h
D[18]	0	0	1	1	0	1	0	0	34h
D[19]	0	0	1	1	1	0	0	0	38h
D[20]	0	0	0	1	1	1	1	1	1Fh
D[21]	0	0	1	0	1	1	1	1	2Fh
D[22]	0	0	1	1	0	1	1	1	37h
D[23]	0	0	1	1	1	0	1	1	3Bh

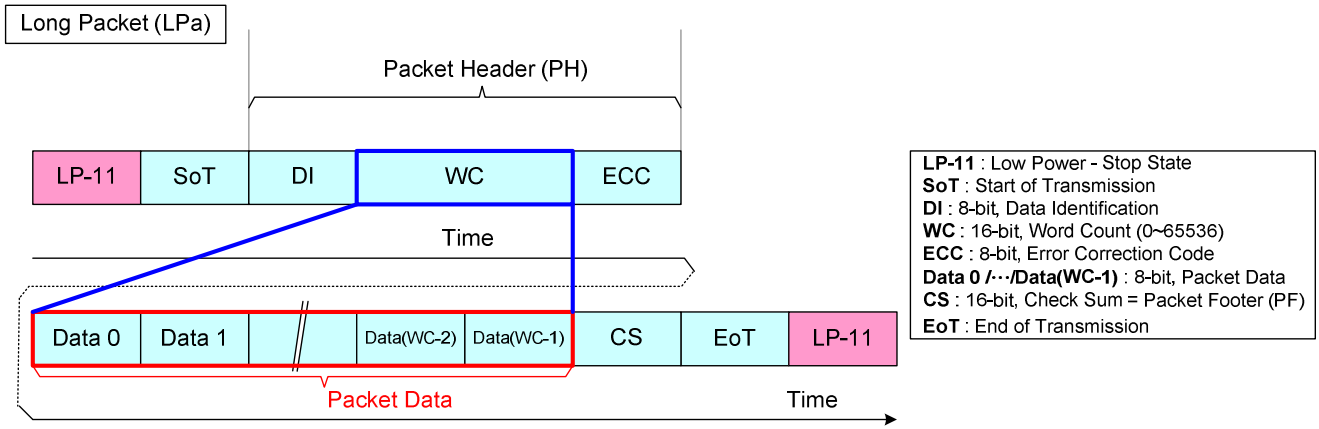
One error is detected if the value of the PO [7…0] is on the above table : One Bit Error Value of the Error Correction Code (ECC) and the receiver can correct this one bit error because this found value also defines what is a location of the corrupt bit e.g.

- PO [7…0] = 0Eh
- The bit of the data (D [23…0]), what is not correct, is D[3]

More than one error is detected if the value of the PO [7…0] is not on the above table: One Bit Error Value of the Error Correction Code (ECC) e.g. PO [7…0] = 0Ch.

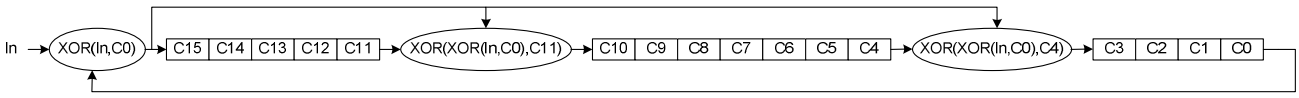
7.3.3.1.4. Packet Data on the Long Packet

Packet Data (PD) of the Long Packet (LPa) is defined after Packet Header (PH) of the Long Packet (LPa). The number of the data bytes is illustrated as below:



7.3.3.1.5. Packet Footer on the Long Packet

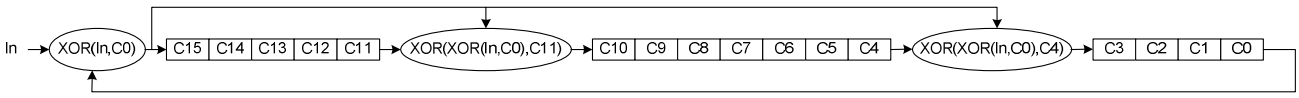
Packet Footer (PF) of the Long Packet (LPa) is defined after the Packet Data (PD) of the Long Packet (LPa). The Packet Footer (PF) is a checksum value what is calculated from the Packet Data of the Long Packet (LPa). The checksum is using a 16-bit Cyclic Redundancy Check (CRC) value which is generated with a polynomial $X_{16}+X_{12}+X_5+X_0$ as it is illustrated below.

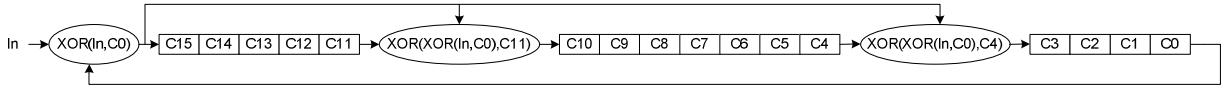


The 16-bit Cyclic Redundancy Check (CRC) generator is initialized to FFFFh before calculations.

The Most Significant Bit (MSB) of the data byte of the Packet Data (PD) is the first bit what is inputted into the 16-bit Cyclic Redundancy Check (CRC).

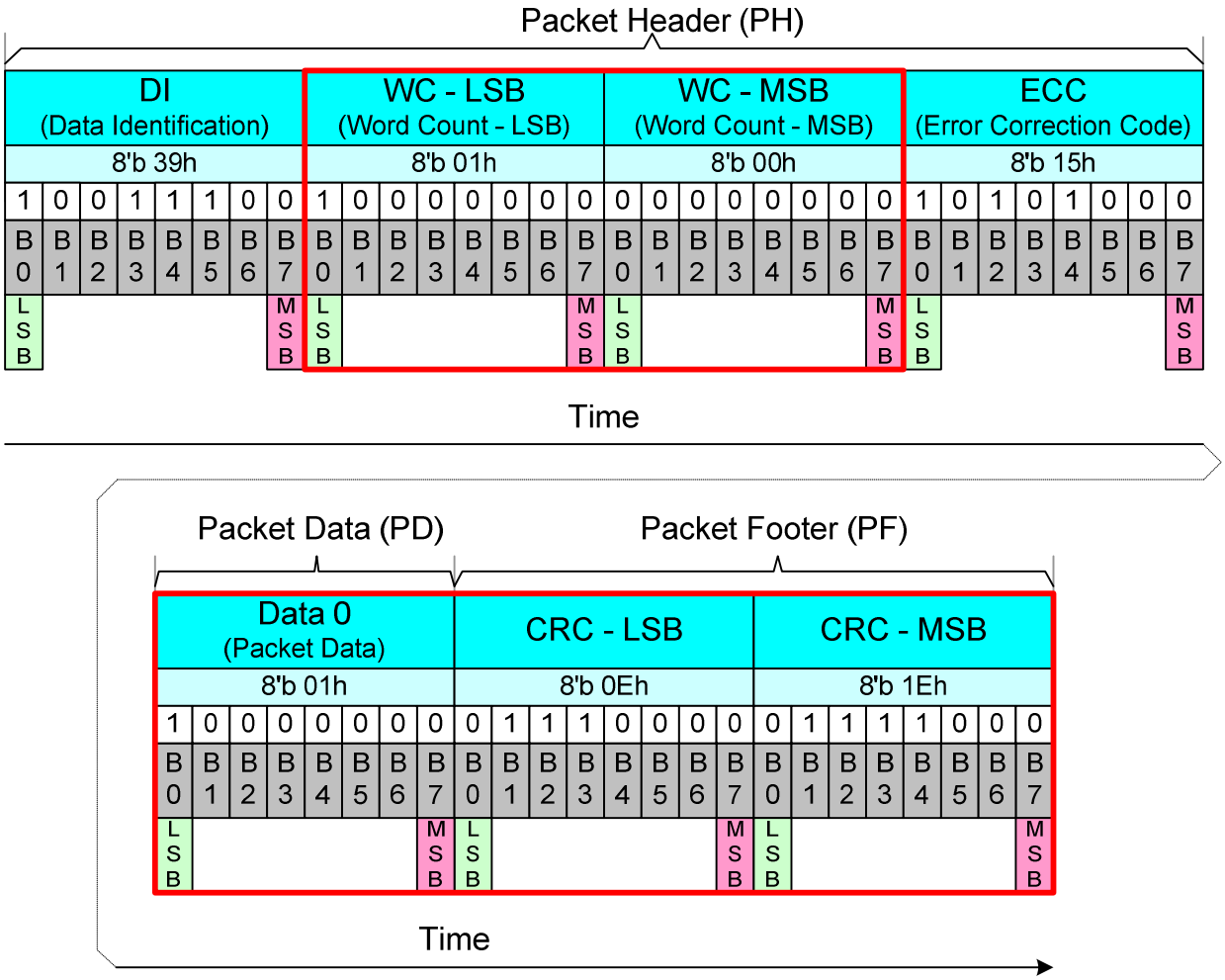
An example of the 16-bit Cyclic Redundancy Check (CRC), where the Packet Data (PD) of the Long Packet (LPa) is 01h, is illustrated (step-by-step) below.





Step	In	XOR(In,C0)	C15	C14	C13	C12	C11	XOR(XOR(In,C0),C11(Step-1))	C10	C9	C8	C7	C6	C5	C4	XOR(XOR(In,C0),C4(Step-1))	C3	C2	C1	C0	C0
0	X	X	1	1	1	1	1	X	1	1	1	1	1	1	1	X	1	1	1	1	X
1	1(LSB)	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
2	0	1	1	0	1	1	1	0	0	1	1	1	1	1	1	0	0	1	1	1	1
3	0	1	1	1	0	1	1	0	0	0	1	1	1	1	1	0	0	0	1	1	1
4	0	1	1	1	1	0	1	0	0	0	0	1	1	1	1	0	0	0	0	1	1
5	0	1	1	1	1	1	0	0	0	0	0	0	1	1	1	0	0	0	0	0	0
6	0	0	0	1	1	1	1	0	0	0	0	0	0	1	1	1	1	0	0	0	0
7	0	0	0	0	1	1	1	1	1	0	0	0	0	0	1	1	1	1	0	0	0
8	0(MSB)	0	0	0	0	1	1	1	1	1	0	0	0	0	0	1	1	1	1	0	0
	1 byte	CRC result	0	0	0	1	1		1	1	0	0	0	0	0		1	1	1	0	
			MSB																	LSB	

A value of the Packet Footer (PF) is 1E0Eh in this example. This example (Command 01h has been sent) is illustrated below.



The receiver is calculated own checksum value from received Packet Data (PD). The receiver compares own checksum and the Packet Footer (PF) what the transmitter has sent.

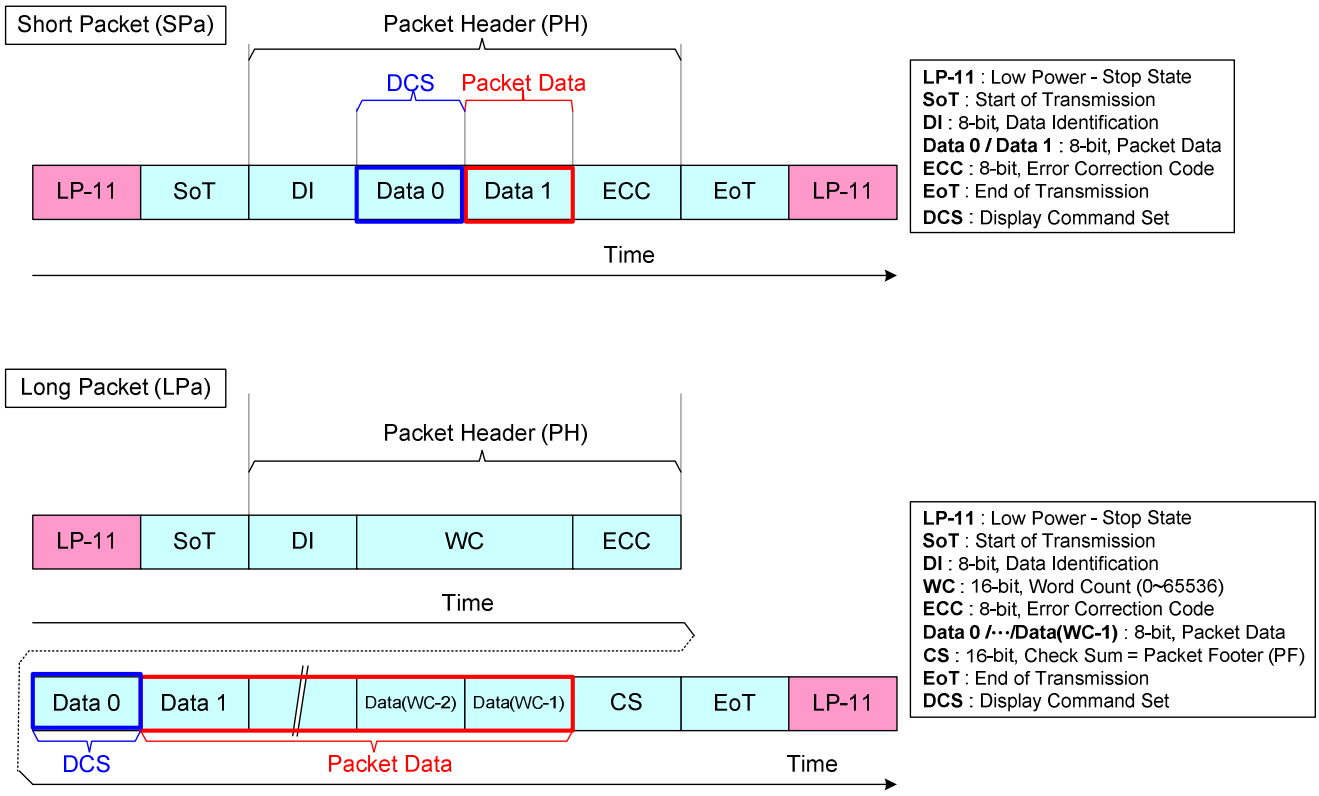
The received Packet Data (PD) and Packet Footer (PF) are correct if the own checksum of the receiver and Packet Footer (PF) is equal and vice versa the received Packet Data (PD) and Packet Footer (PF) are not correct if the own checksum of the receiver and Packet Footer (PF) are not equal.

7.3.3.2. Packet Transmissions

7.3.3.2.1. Packet form the MCU to ILI9486

7.3.3.2.1.1. Display Command Set (DCS)

Display Command Set (DCS), which is defined on next chapter, is used from the MCU to ILI9486. This Display Command Set (DCS) is always defined on the Data 0 of the Packet Data (PD), which is included in Short Packet (SPa) and Long packet (LPa) as these are illustrated as below.



7.3.3.2.1.2. Display Command Set Write, no Parameter (DCSWN-S)

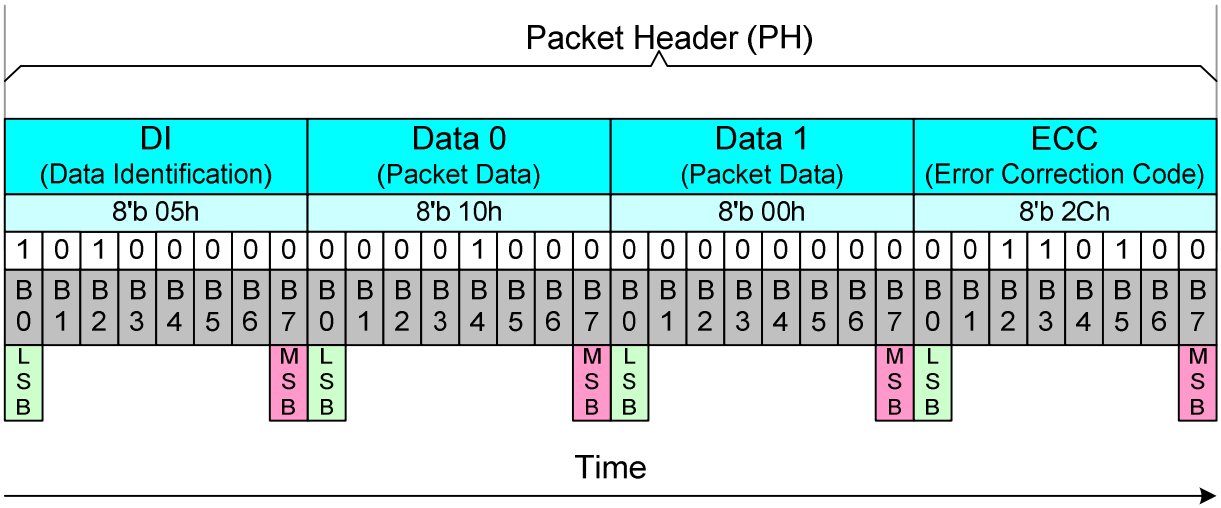
"Display Command Set (DCS) Write, No Parameter" is always using a Short Packet (SPa), what is defined on Data Type (DT, 00 0101b), from the MCU to ILI9486. These commands are defined on a table below.

Command
NOP (00h)
Software Reset (01h)
Sleep IN(10h)
Sleep Out (11h)
Partial Mode ON (12h)
Normal Display Mode ON (13h)
Display OFF (28h)
Display ON (29h)
Tearing Effect Line OFF (34h)
Idle Mode OFF (38h)
Idle Mode ON (39h)

Short Packet (SPa) is defined e.g.

- Data Identification (DI)
  - ◯Virtual Channel (VC, DI[7…6]): 00b
  - ◯Data Type (DT, DI[5…0]): 00 0101b
- Packet Data (PD)
  - ◯Data 0: "Sleep In (10h)", Display Command Set (DCS)
  - ◯Data 1: Always 00hex
- Error Correction Code (ECC)

This is defined on the Short Packet (SPa) as follows.



7.3.3.2.1.3. Display Command Set Write, 1 Parameter (DCSW1-S)

"Display Command Set (DCS) Write, 1 Parameter" (DCSW1-S) is always using a Short Packet (SPa), what is defined on Data Type (DT, 01 0101b), from the MCU to ILI9486. These commands are defined on a table below.

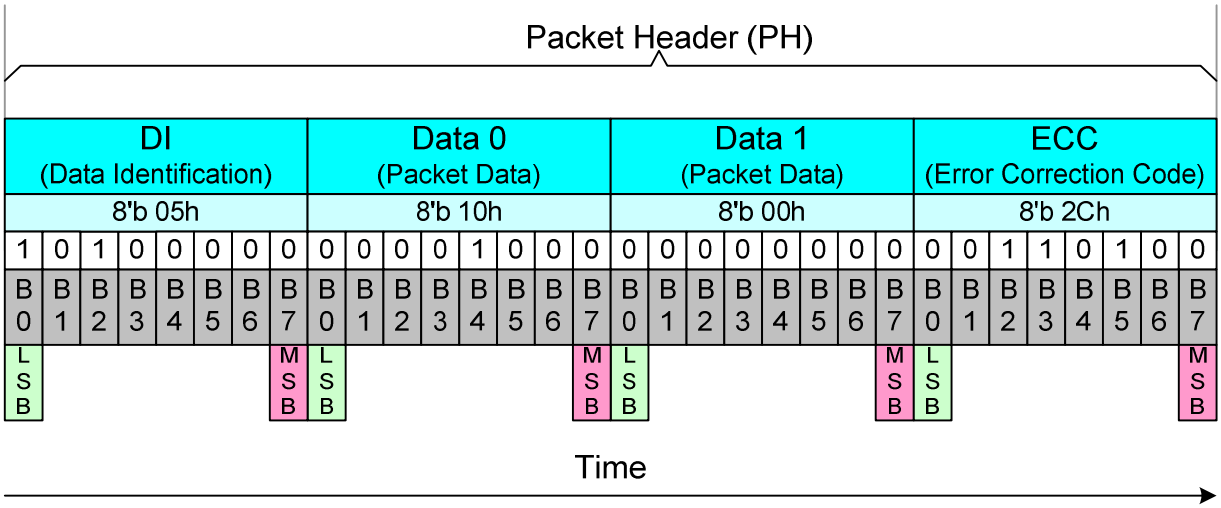
Command
Gamma Set
Memory Write (2Ch), Note
Tearing Effect Line ON (35h)
Memory Access Control (36h)
Interface Pixel Format (3Ah)
Memory Write Continue (3Ch), Note
Write Display Brightness (51h)
Write CTRL Display (53h)
Write Content Adaptive Brightness control (55h)
Write CABC Minimum Brightness (5Eh)

Note: One Subpixel has been written

Short Packet (SPa) is defined e.g.

- Data Identification (DI)
  - Virtual Channel (VC, DI[7…6]): 00b
  - Data Type (DT, DI[5…0]): 01 0101b
- Packet Data (PD)
  - Data 0: "Gamma Set (26h)", Display Command Set (DCS)
  - Data 1: 01hex, Parameter of the DCS
- Error Correction Code (ECC)

This is defined on the Short Packet (SPa) as follows.



7.3.3.2.1.4. Display Command Set Write Long (DCSW-L)

"Display Command Set (DCS) Write Long" (DCSW-L) is always using a Long Packet (LPa), what is defined on Data Type (DT, 11 1001b), from the MCU to ILI9486. Command (No Parameters) and Write (1 or more parameters) are defined on a table below.

Command
NOP (00h) , Note 1
Software Reset (01h) , Note 1
Sleep IN(10h) , Note 1
Sleep Out (11h) , Note 1
Partial Mode ON (12h) , Note 1
Normal Display Mode ON (13h) , Note 1
Gamma Set (26h), Note 2
Display OFF (28h) , Note 1
Display ON (29h) , Note 1
Column Address Set (2Ah)
Page Address Set (2Bh)
Memory Write (2Ch), Note 2
Partial Area (30h)
Tearing Effect Line OFF (34h), Note 1
Tearing Effect Line ON (35h), Note 2
Memory Access Control (36h), Note 2
Idle Mode OFF (38h) , Note 1
Idle Mode ON (39h) , Note 1
Interface Pixel Format(3Ah)
Memory Write Continue (3Ch), Note 2
Write Display Brightness (51h) , Note 2
Write CTRL Display (53h) , Note 2
Write Content Adaptive Brightness control (55h) , Note 2
Write CABC Minimum Brightness (5Eh)

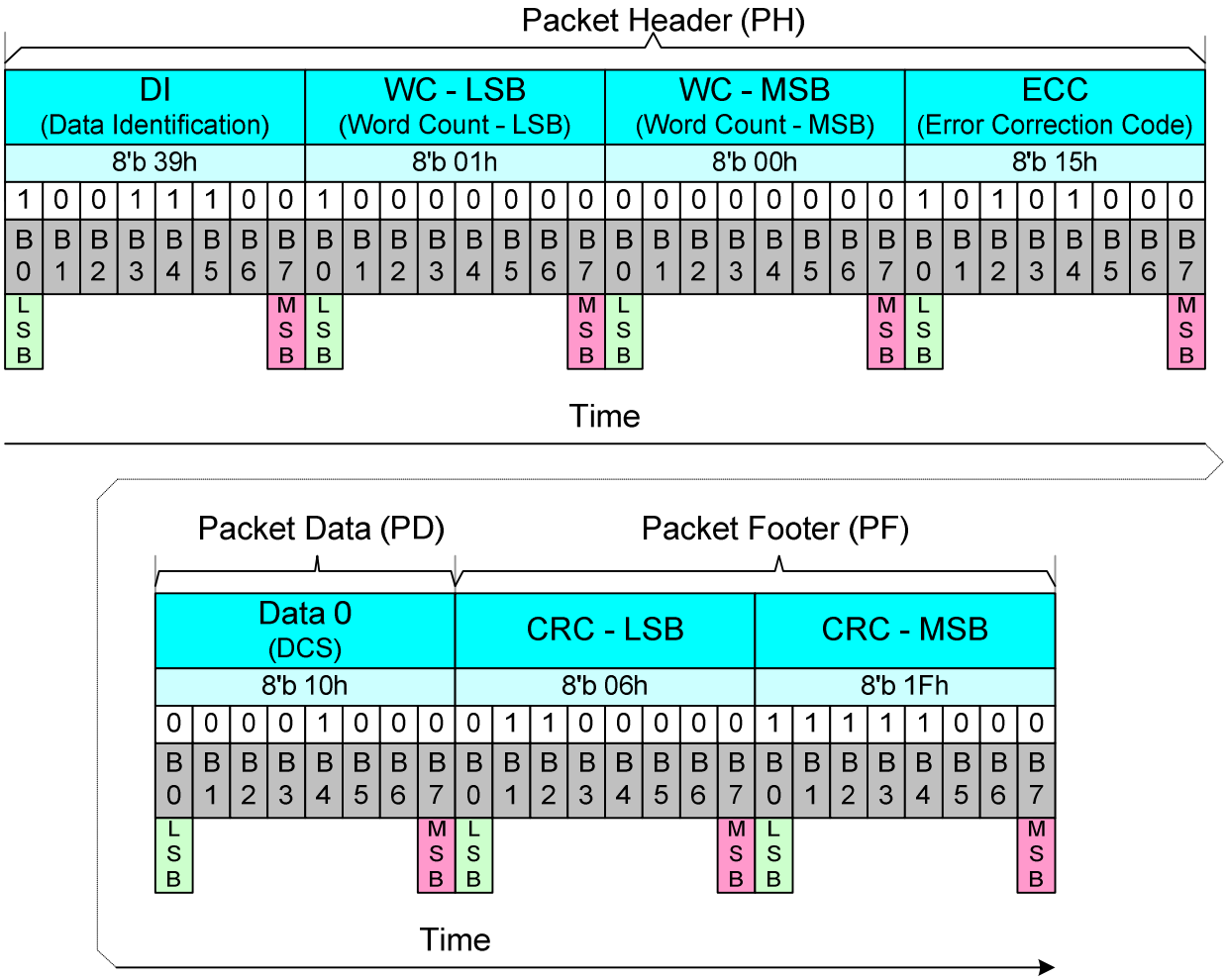
Notes: (1) Also Short Packet (SPa) can be used; See chapter "7.3.3.2.1.1.1 Display Command Set (DCS) Write, No Parameter"

(2) Also Short Packet (SPa) can be used; See chapter "7.3.3.2.1.1.2 Display Command Set (DCS) Write, 1 Parameter"

Long Packet (LPa), when a command (No Parameter) was sent, is defined e.g.

- Data Identification (DI)
  - Virtual Channel (VC, DI [7…6]): 00b
  - Data Type (DT, DI [5…0]): 11 1001b
- Word Count (WC)
  - Word Count (WC): 0001h
- Error Correction Code (ECC)
- Packet Data (PD): Data 0: “Sleep In (10h)”, Display Command Set (DCS)
- Packet Footer (PF)

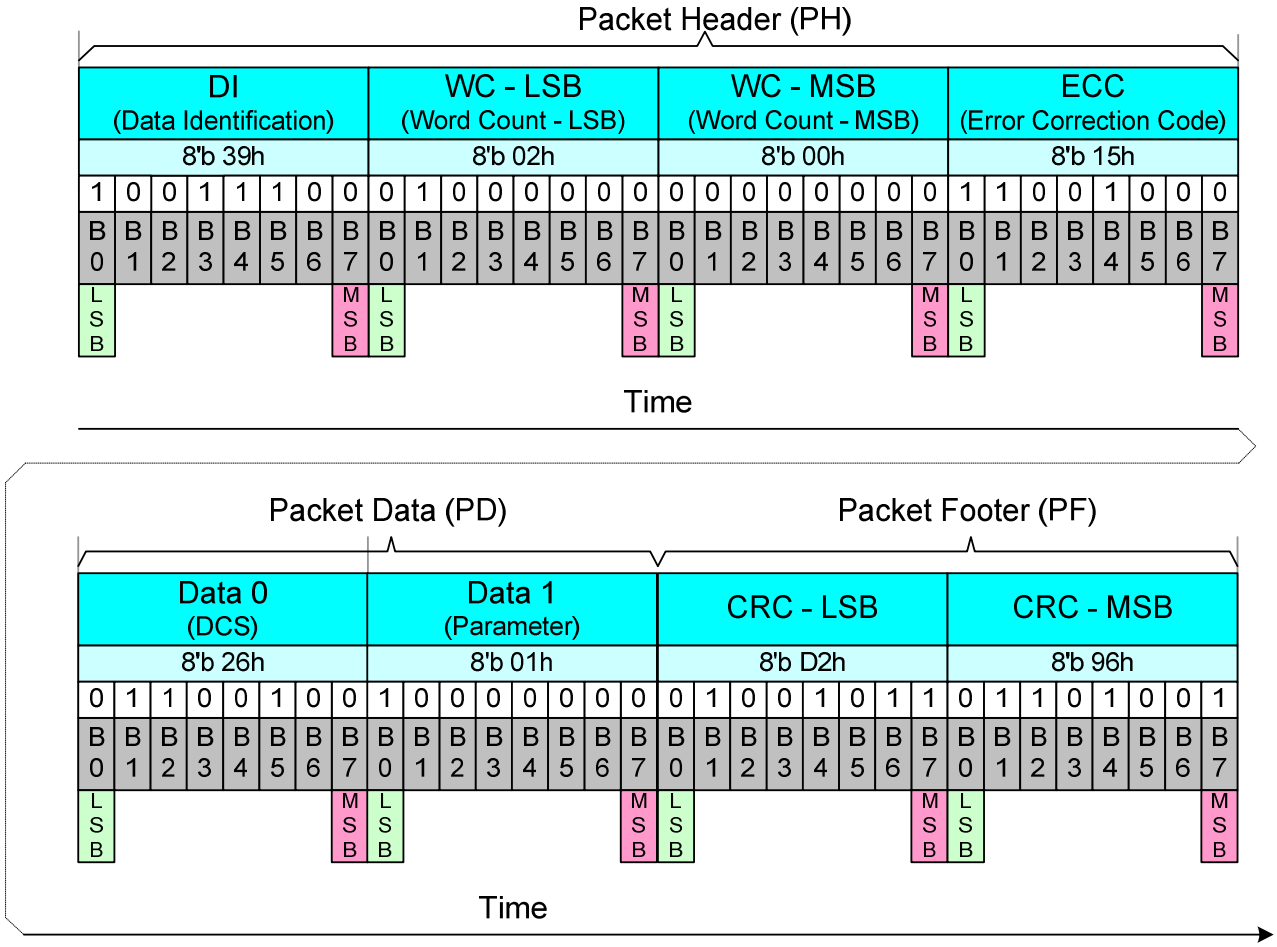
This is defined on the Long Packet (LPa) as follows.



Long Packet (LPa), when a Write (1 parameter) was sent, is defined e.g.

- Data Identification (DI)
  - Virtual Channel (VC, DI [7…6]): 00b
  - Data Type (DT, DI [5…0]): 11 1001b
- Word Count (WC)
  - Word Count (WC): 0002h
- Error Correction Code (ECC)
- Packet Data (PD):
  - Data 0: “Gamma Set (26h)”, Display Command Set (DCS)
  - Data 1: 01hex, Parameter of the DCS
- Packet Footer (PF)

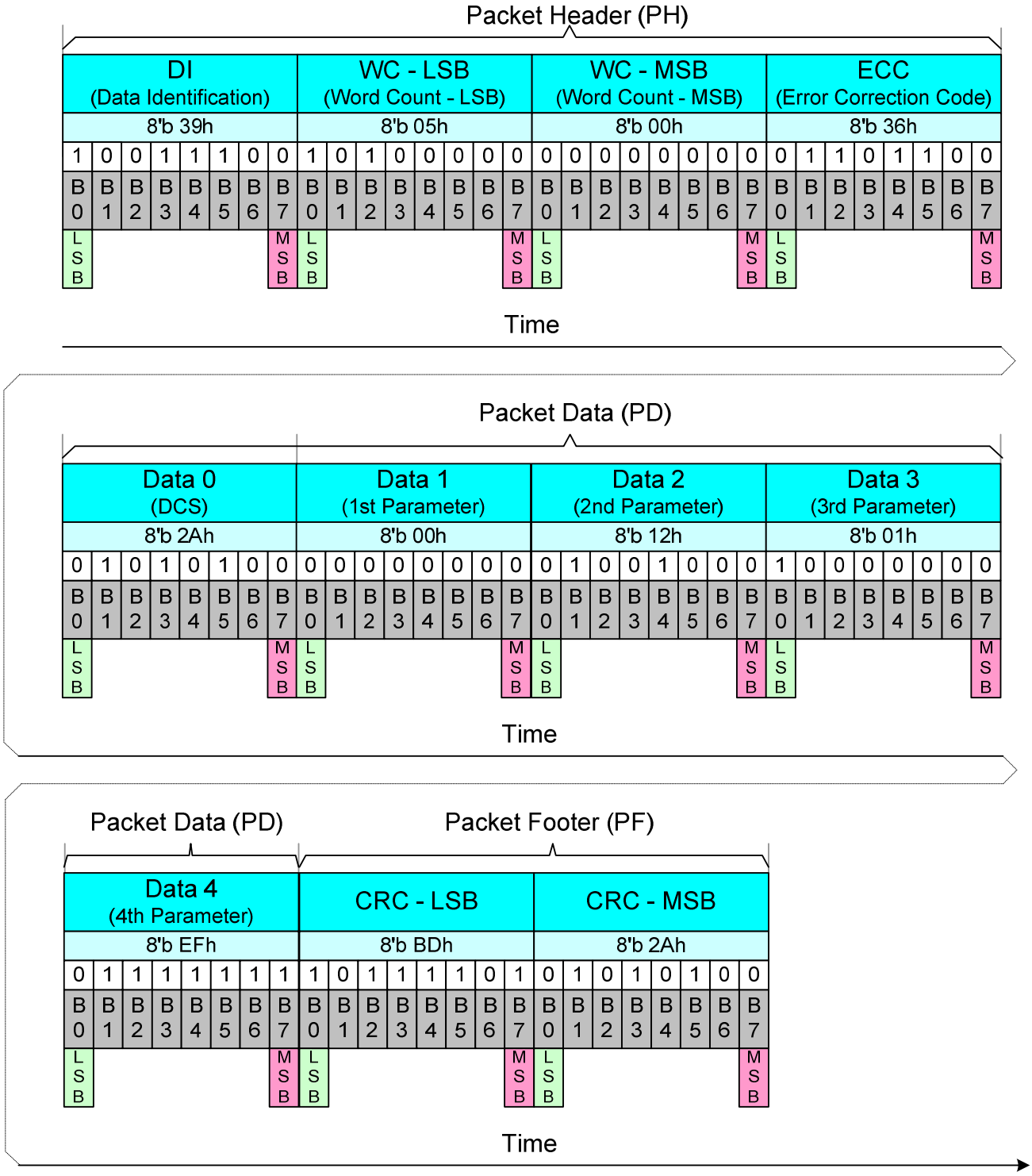
This is defined on the Long Packet (LPa) as follows



Long Packet (LPa), when a Write (4 parameters) was sent, is defined e.g.

- Data Identification (DI)
  - Virtual Channel (VC, DI [7…6]): 00b
  - Data Type (DT, DI [5…0]): 11 1001b
- Word Count (WC)
  - Word Count (WC): 0005h
- Error Correction Code (ECC)
- Packet Data (PD):
  - Data 0: “Column Address Set (2Ah)”, Display Command Set (DCS)
  - Data 1: 00hex, 1st Parameter of the DCS, Start Column SC [15…8]
  - Data 2: 12hex, 2nd Parameter of the DCS, Start Column SC [7…0]
  - Data 3: 01hex, 3rd Parameter of the DCS, End Column EC [15…8]
  - Data 4: EFhex, 4th Parameter of the DCS, End Column EC [7…0]
- Packet Footer (PF)

This is defined on the Long Packet (LPa) as follows.



7.3.3.2.1.5. Display Command Set Read, No Parameter (DCSRN-S)

"Display Command Set (DCS) Read, No Parameter" (DCSRN-S) is always using a Short Packet (SPa), what is defined on Data Type (DT, 00 0110b), from the MCU to ILI9486. These commands are defined on a table below. The 1st parameter (Dummy Data) is not returned as it is done in MCU parallel interface. The first returned parameter is the 2nd parameter in DSI case.

Command
Read Number of the Errors on DSI (05h)
Read Display Power Mode (0Ah)
Read Display MADCTL (0Bh)
Read Display Pixel Format (0Ch)
Read Display Image Mode (0Dh)
Read Display Signal Mode (0Eh)
Read Display Self-Diagnostic Result (0Fh)
Memory Read (2Eh)
Memory Read Continue (3Eh)
Read Display Brightness Value (52h)
Read CTRL Value Display (54h)
Read Black/White Low Bits (70h)
Read Bkx (71h)
Read Bky(72h)
Read Wx (73h)
Read Wy (74h)
Read Red/Green Low Bits (75h)
Read Rx (76h)
Read Ry (77h)
Read Gx (78h)
Read Gy (79h)
Read Blue/A Color Low Bits (7Ah)
Read Bx (7Bh)
Read By (7Ch)
Read Ax (7Dh)
Read Ay (7Eh)
Read DDB Start (A1h)
Read DDB Continue (A8h)
First Checksum (AAh)
Read Continue Checksum (Afh)
Read ID1 (DAh)
Read ID2 (DBh)
Read ID3 (DCh)

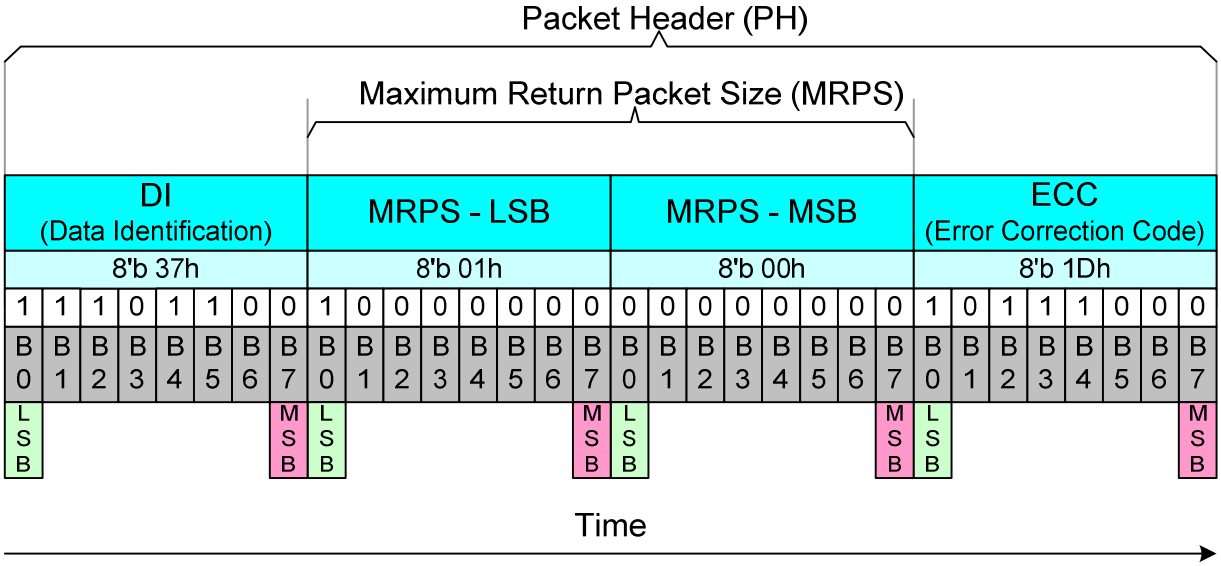
The MCU has to define to ILI9486, what is the maximum size of the return packet. A command, what is used for this purpose, is "Set Maximum Return Packet Size" (SMRPS-S), which Data Type (DT) is 11 0111b and which is using Short Packet (SPa) before the MCU can send "Display Command Set (DCS) Read, No Parameter" to ILI9486. This same sequence is illustrated for reference purposes below.

Step 1:

- The MCU sends "Set Maximum Return Packet Size" (Short Packet (SPa)) (SMRPS-S) to ILI9486 when it wants to return one byte from ILI9486
- Data Identification (DI)
  - Virtual Channel (VC, DI[7…6]): 00b
  - Data Type (DT, DI[5…0]): 11 0111b
- Maximum Return Packet Size (MRPS)

- Data 0: 01hex
- Data 1: 00hex

• Error Correction Code (ECC)



Step 2:

• The MCU wants to receive a value of the “Read ID1 (DAh)” from the display module when the MCU sends “Display Command Set (DCS) Read, No Parameter” to ILI9486

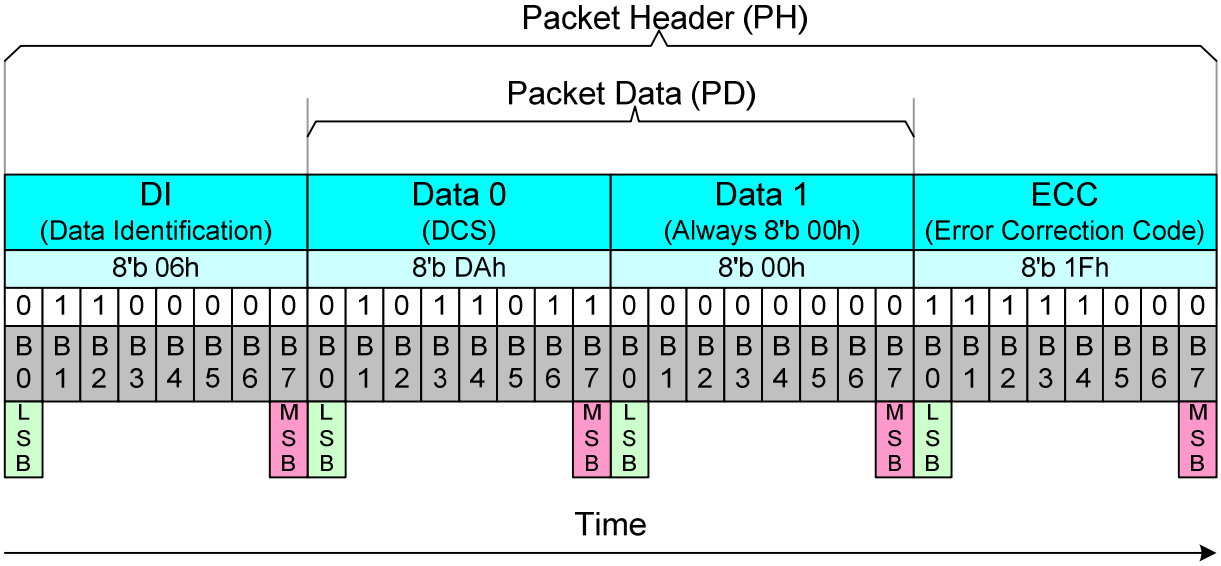
• Data Identification (DI)

- Virtual Channel (VC, DI [7…6]): 00b
- Data Type (DT, DI [5…0]): 00 0110b

• Packet Data (PD)

- Data 0: “Read ID1 (DAh)”, Display Command Set (DCS)
- Data 1: Always 00hex

• Error Correction Code (ECC)



Step 3: ILI9486 can send 2 different informations to the MCU after Bus Turnaround (BTA)

1. An acknowledge with Error Report (AwER), which is using a Short Packet (SPa), if there is an error to receive a command.
2. Information of the received command. Short Packet (SPa) or Long Packet (LPa)

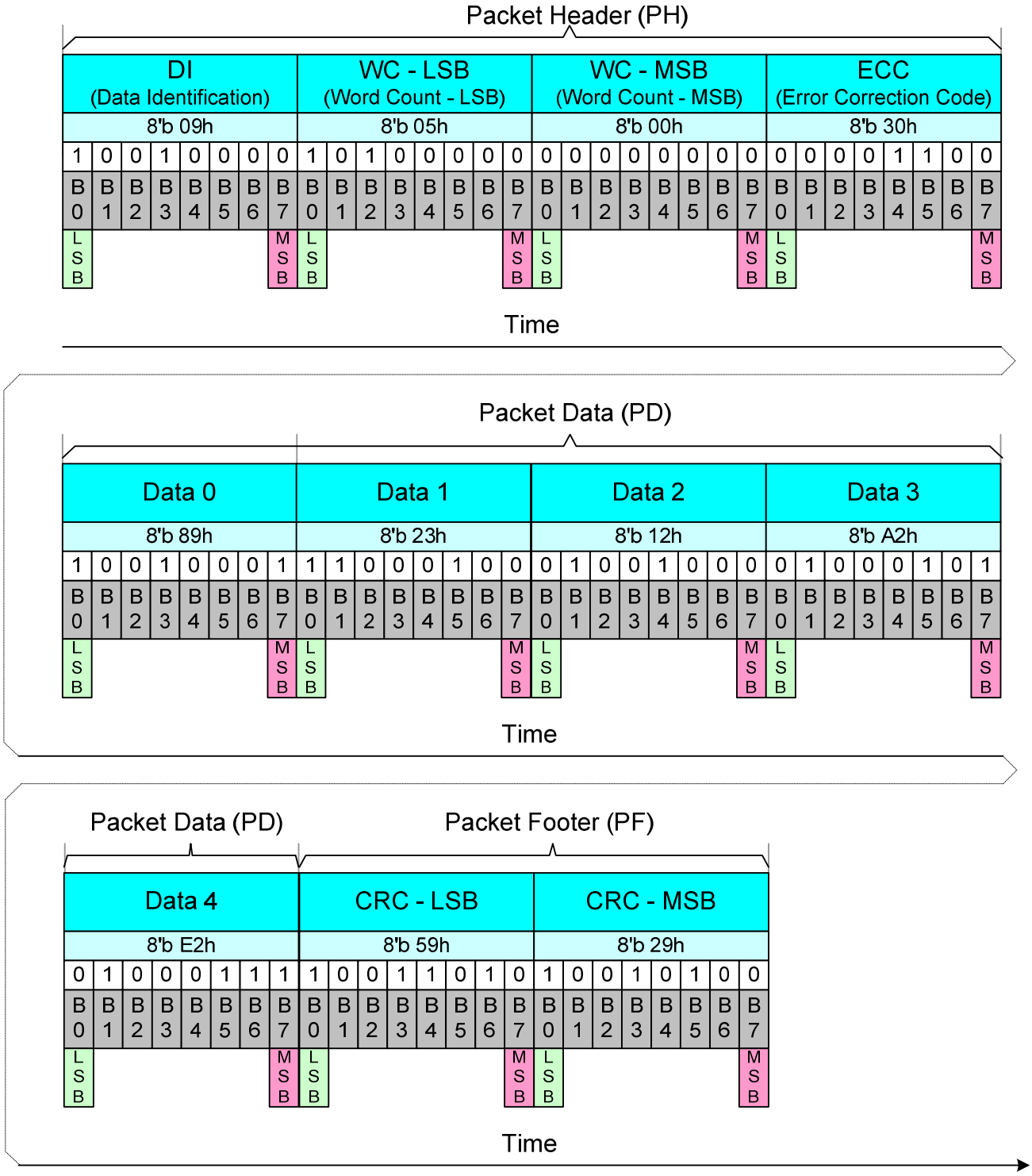
7.3.3.2.1.6. Null Packet, No Data (NP-L)

"Null Packet, No Data" (NP-L) is always using a Long Packet (LPa), what is defined on Data Type (DT, 00 1001b), from the MCU to ILI9486. The purpose of this command is keeping data lanes in the high speed mode (HSDT), if it is needed. ILI9486 is ignored Packet Data (PD) what the MCU is sending.

Long Packet (LPa), when 5 random data bytes of the Packet Data (PD) were sent, is defined e.g.

- Data Identification (DI)
  - Virtual Channel (VC, DI [7…6]): 00b
  - Data Type (DT, DI [5…0]): 00 1001b
- Word Count (WC)
  - Word Count (WC): 0005hex
- Error Correction Code (ECC)
- Packet Data (PD):
  - Data 0: 89hex (Random data)
  - Data 1: 23hex (Random data)
  - Data 2: 12hex (Random data)
  - Data 3: A2hex (Random data)
  - Data 4: E2hex (Random data)
- Packet Footer (PF)

This is defined on the Long Packet (LPa) as follows.



7.3.3.2.1.7. End of Transmission Packet (EoTP)

"End of Transmission Packet" (EoTP) is always using a Short Packet (SPa), what is defined on Data Type (DT, 00 1000b), from the MCU to ILI9486. The purposes of this command is terminated the high Speed Data Transmission (HSDT) mode properly when there is added this extra packet after the last payload packet before "End of Transmission" (EoT), which is an interface level functionality.

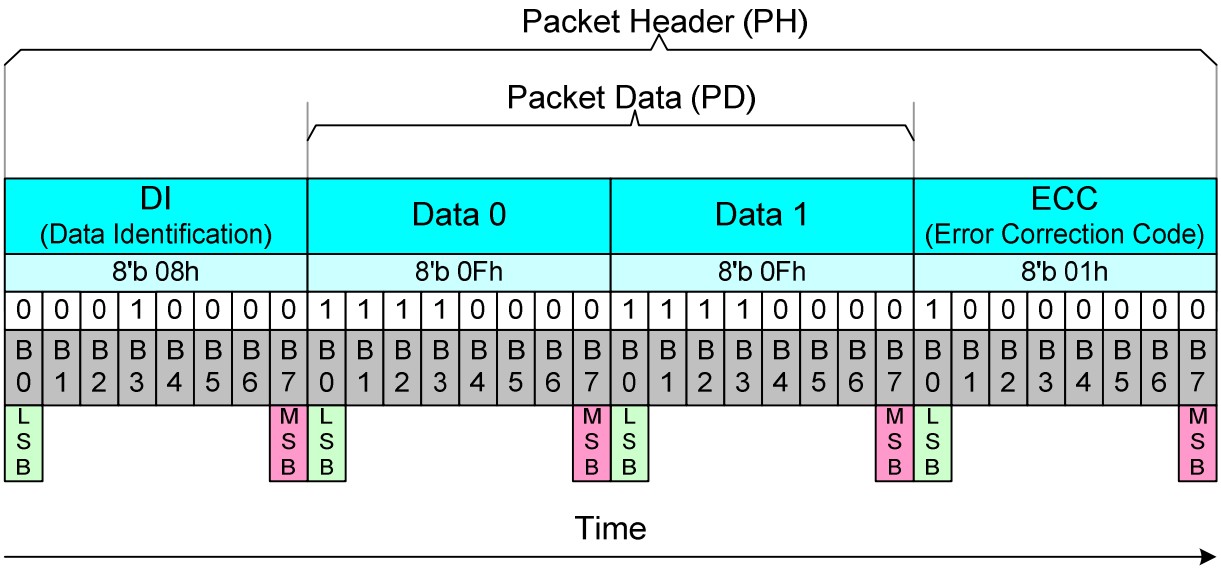
"End of Transmission Packet" (EoTP) should also be supported in the Low Power Data Transmission (LPDT) mode on ILI9486e even if this functionality has not been designed for this purposes.

The MCU can decide if it wants to use these "End of Transmission Packet" (EoTP) or not but ILI9486 has to be supporting both modes: With or Without "End of Transmission Packet" (EoTP).

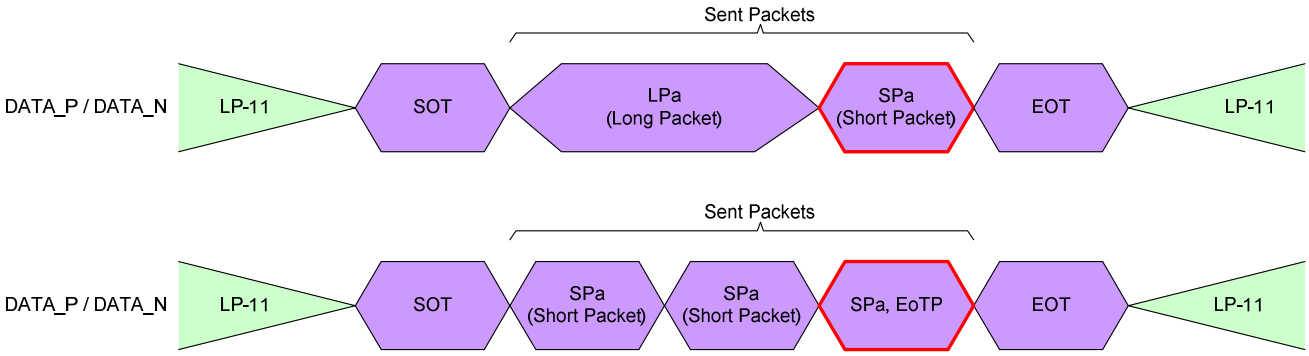
Short Packet (SPa) is using a fixed format as follows

- Data Identification (DI)
  - Virtual Channel (VC, DI [7…6]): 00b
  - Data Type (DT, DI [5…0]): 00 1000b
- Packet Data (PD)
  - Data 0: 0Fhex
  - Data 1: 0Fhex
- Error Correction Code (ECC)
  - ECC: 01hex

This is defined on the Short Packet (SPa) as follows.



Some use cases of the "End of Transmission Packet" (EoTP) are illustrated only for reference purposes below.

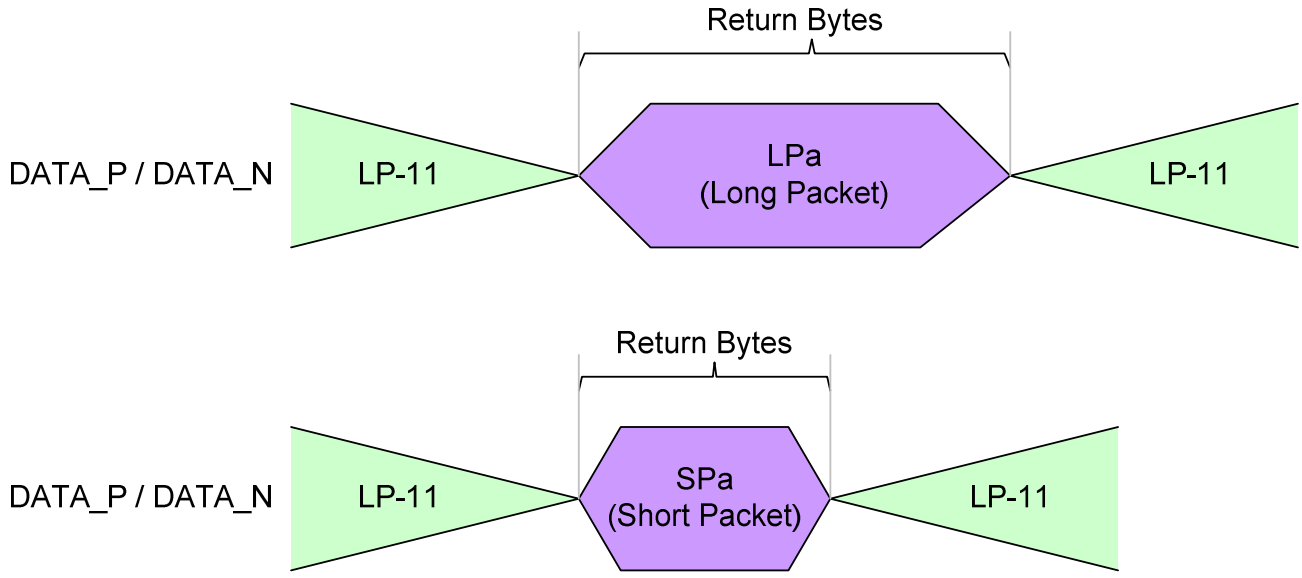


7.3.3.2.2. Packet from ILI9486 to MCU

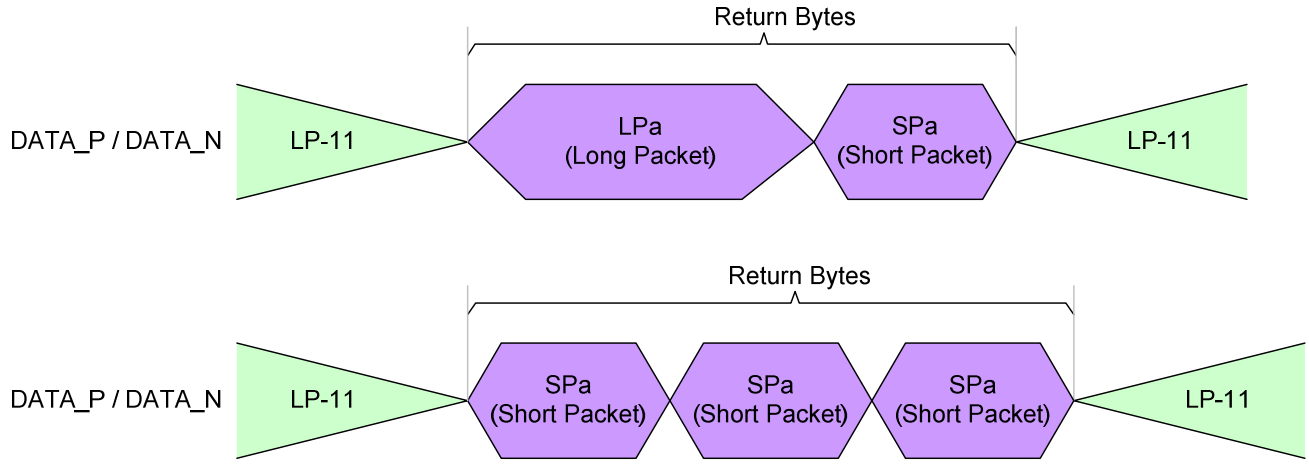
7.3.3.2.2.1. Used Packet Types

ILI9486 is always using Short Packet (SPa) or Long Packet (LPa), when it is returning information to the MCU after the MCU has requested information from ILI9486. This information can be a response of the Display Command Set (DCS) or an Acknowledge with Error Report (AwER). The used packet type is defined on Data Type (DT).

It is not possible that ILI9486 is sending return bytes in several packets even if the maximum size of the Packet Data (PD) could be sent in one packet.
The return bytes on a single packet are illustrated for reference purposes below.



The return bytes on several packets are illustrated for reference purposes below.



7.3.3.2.2.2. Acknowledge with Error Report

"Acknowledge with Error Report" (AwER) is always using a Short Packet (SPa), what is defined on Data Type (DT, 00 0010b), from ILI9486 to the MCU.

The Packet Data (PD) can include bits, which are defining the current error, when a corresponding bit is set to '1', as they are defined on the following table.

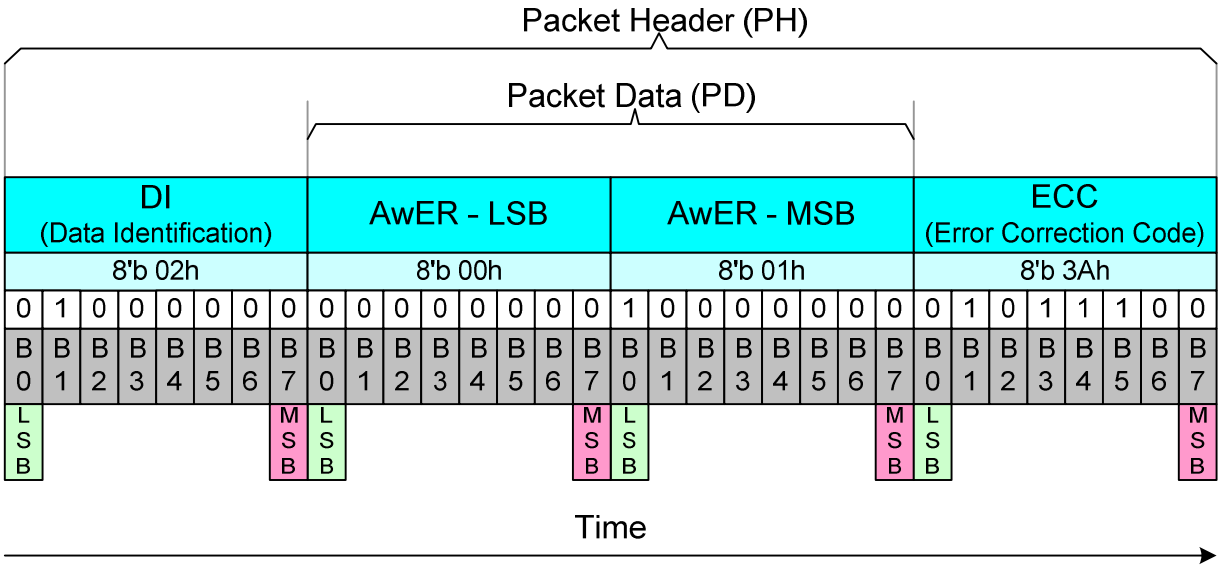
Bit	The Description of Acknowledge Error Report (AwER)	
	Short Packet	Long Packet
0	SoT Error	SoT Error
1	SoT Sync Error	SoT Sync Error
2	EoT Sync Error	EoT Sync Error
3	Escape Mode Entry Command Error	Escape Mode Entry Command Error
4	Low-Power Transmit Error	Low-Power Transmit Error
5	Any Protocol Timer-Out	Any Protocol Timer-Out
6	False Control Error	False Control Error
7	Contention is Detected on the Display Module	Contention is Detected on the Display Module
8	ECC Error, Single-Bit (Detected and Corrected)	ECC Error, Single-Bit (Detected and Corrected)
9	ECC Error, Multi-Bit (Detected, Not Corrected)	ECC Error, Multi-Bit (Detected, Not Corrected)
10	Reserved, Set to '0' internally	Checksum Error
11	DSI Data Type (DT), Not Recognized	DSI Data Type (DT), Not Recognized
12	DSI Virtual Channel (VC) ID Invalid	DSI Virtual Channel (VC) ID Invalid
13	DSI Protocol Violation	DSI Protocol Violation
14	Reserved, Set to '0' internally	Reserved, Set to '0' internally
15	Reserved, Set to '0' internally	Reserved, Set to '0' internally

These errors are included from all packages what has been received from the MCU to ILI9486, before Bus Turnaround (BTA). ILI9486 ignores the received packet which includes error or errors.

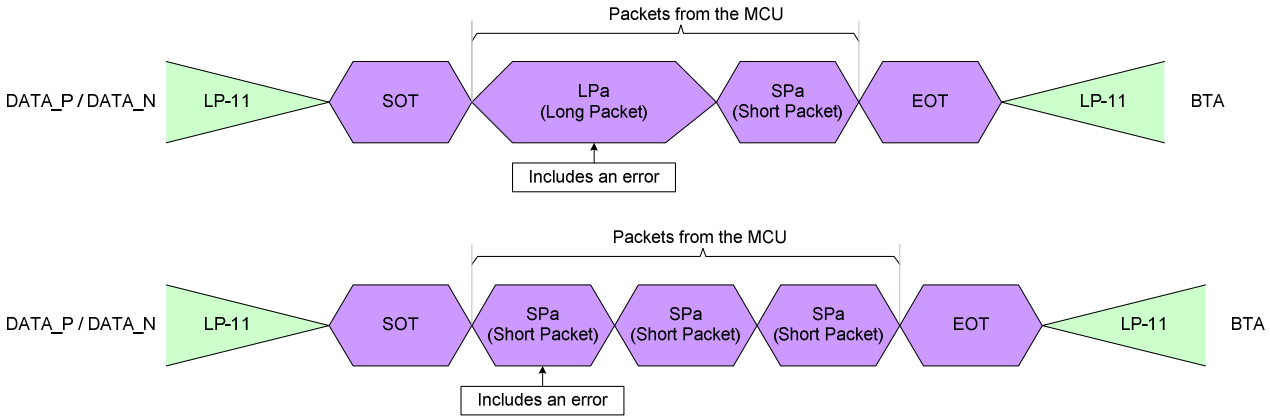
Acknowledge with Error Report (AwER) of the Short Packet (SPa) is defined e.g.

- Data Identification (DI)
  - Virtual Channel (VC, DI[7…6]): 00b
  - Data Type (DT, DI[5…0]): 00 0010b
- Packet Data (PD)
  - Bit 8: ECC Error, single-bit (detected and corrected)
  - AwER: 0100h
- Error Correction Code (ECC)

This is defined on the Short Packet (SPa) as follows.



It is possible that ILI9486 has received several packets, which have included errors, from the MCU before the MCU is doing Bus Turnaround (BTA). Some examples are illustrated for reference purposes below.

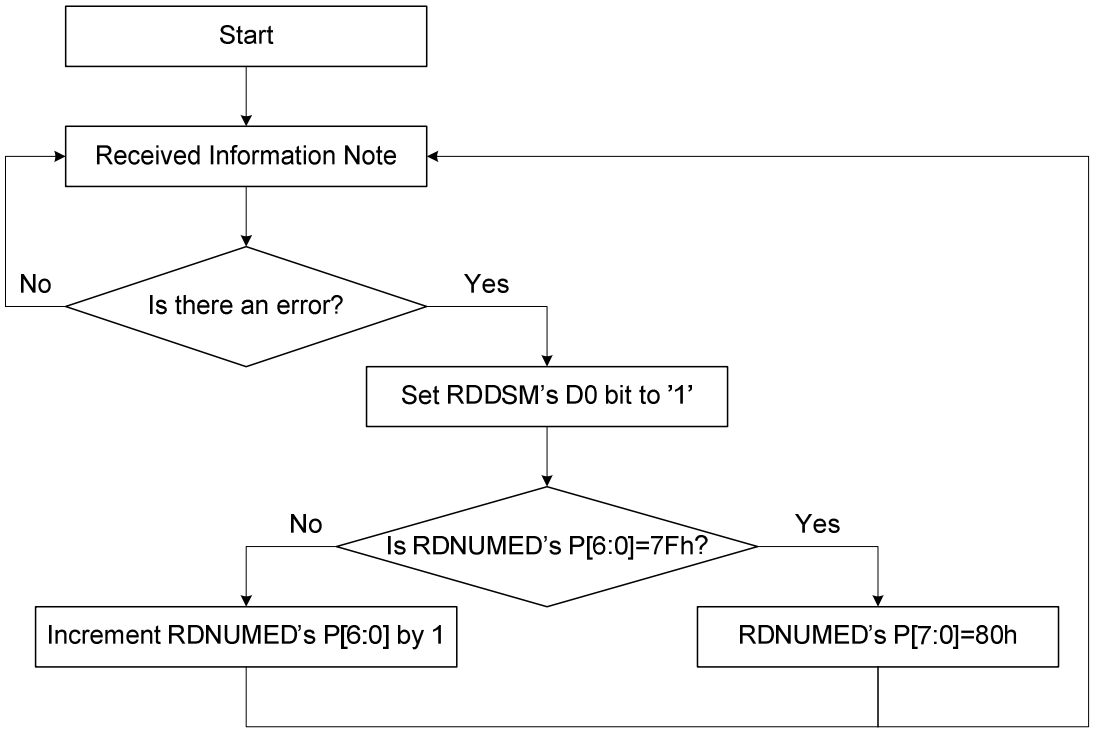


Therefore, there is needed a method to check if there has been errors on the previous packets. These errors of the previous packets can check “Read Display Signal Mode (0Eh)” and “Read Number of the Errors on DSI (05h)” commands.

The bit D0 of the “Read Display Signal Mode (0Eh)” command has been set to ‘1’ if a received packet includes an error.

The numbers of the packets, which are including an error, are calculated on the RDNUMED register, which can read “Read Number of the Errors on DSI (05h)” command. This command also sets the RDNUMED register to 00h as well as set the bit D0 of the “Read Display Signal Mode (0Eh)” command to ‘0’ after the MCU has read the RDNUMED register from ILI9486.

The functionality of the RDNUMED register is illustrated for reference purposes below.



Note: This information can Interface or Packet Level Communication but it is always from the MCU to ILI9486 in this case.

7.3.3.2.2.3. DCS Read Long Response (DCSRR-L)

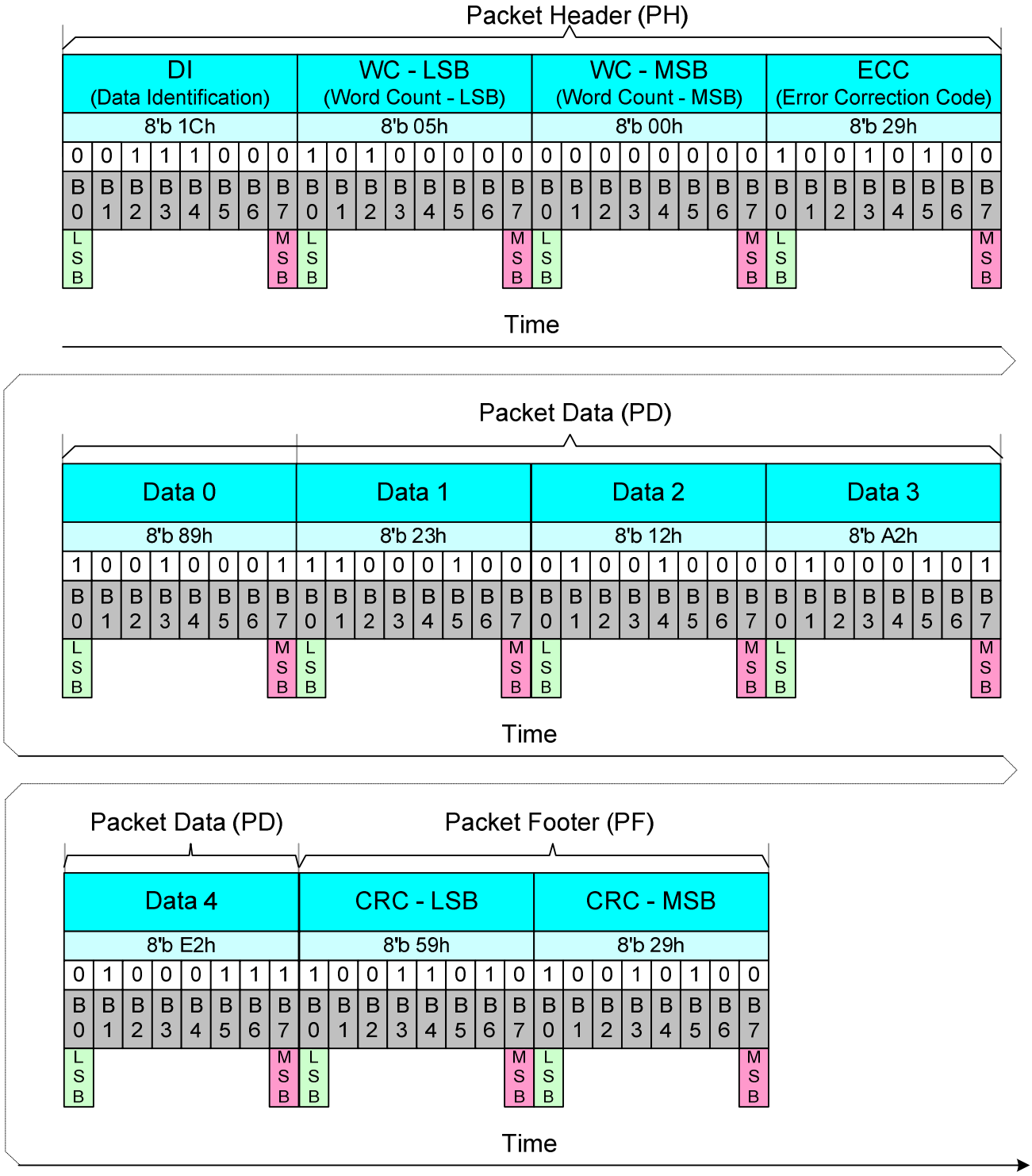
"DCS Read Long Response" (DCSRR-L) is always using a Long Packet (LPa), what is defined on Data Type (DT, 01 1100b), from ILI9486 to the MCU.

"DCS Read Long Response" (DCSRR-L) is used when ILI9486 wants to response a DCS Read command, which the MCU has sent to ILI9486.

Long Packet (LPa), which includes 5 data bytes of the Packet Data (PD), is defined e.g.

- Data Identification (DI)
- Virtual Channel (VC, DI [7…6]): 00b
    - Data Type (DT, DI [5…0]): 01 1100b
- Word Count (WC)
    - Word Count (WC): 0005hex
- Error Correction Code (ECC)
- Packet Data (PD):
    - Data 0: 89hex
    - Data 1: 23hex
    - Data 2: 12hex
    - Data 3: A2hex
    - Data 4: E2hex
- Packet Footer (PF)

This is defined on the Long Packet (LP) as follows.



7.3.3.2.2.4. DCS Read Short Response, 1 Byte Returned (DCSRR1-S)

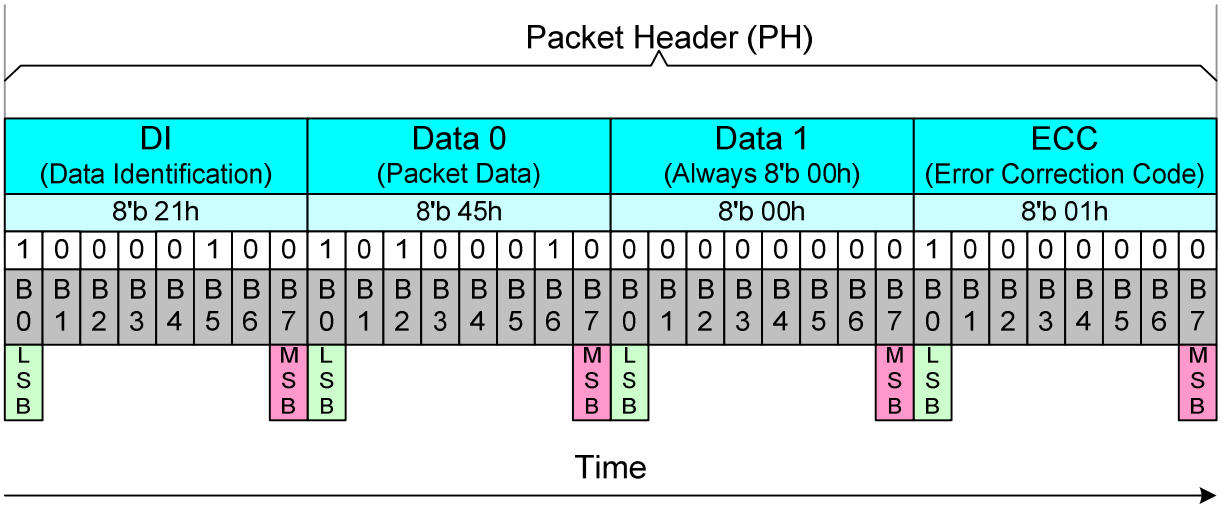
"DCS Read Short Response, 1 Byte Returned" (DCSRR1-S) is always using a Short Packet (SPa), what is defined on Data Type (DT, 10 0001b), from ILI9486 to the MCU.

"DCS Read Short Response, 1 Byte Returned" (DCSRR1-S) is used when ILI9486 wants to response a DCS Read command, which the MCU has sent to ILI9486.

Short Packet (SPa) is defined e.g.

- Data Identification (DI)
  - Virtual Channel (VC, DI [7…6]): 00b
  - Data Type (DT, DI [5…0]): 10 0001b
- Packet Data (PD)
  - Data 0: 45hex
  - Data 1: 00hex (Always)
- Error Correction Code (ECC)

This is defined on the Short Packet (SP) as follows.



7.3.3.2.2.5. DCS Read Short Response, 2 Bytes Returned (DCSRR2-S)

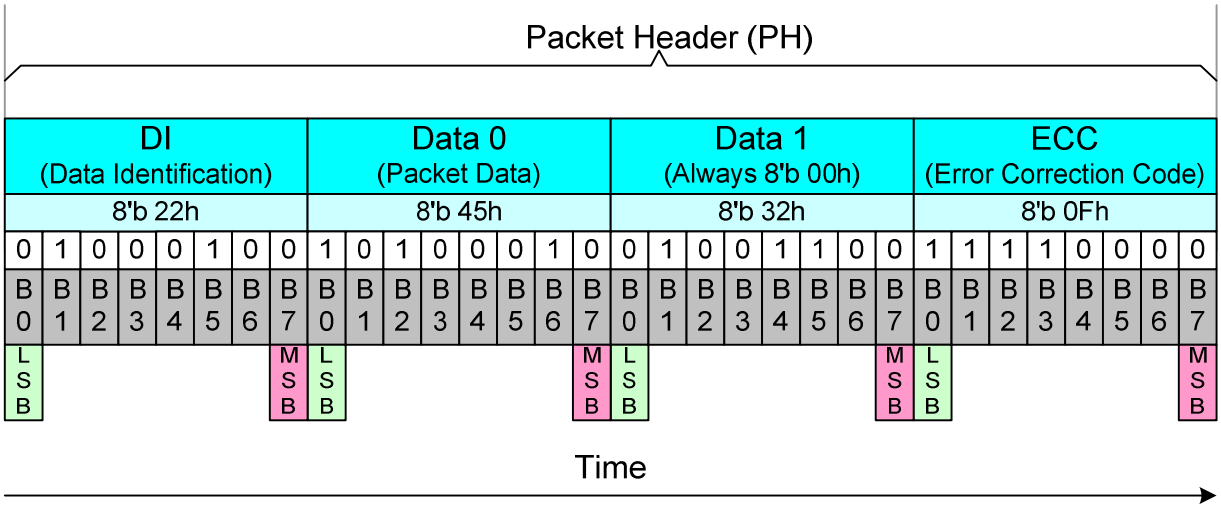
"DCS Read Short Response, 2 Bytes Returned" (DCSRR2-S) is always using a Short Packet (SPa), what is defined on Data Type (DT, 10 0010b), from ILI9486 to the MCU.

"DCS Read Short Response, 2 Bytes Returned" (DCSRR2-S) is used when ILI9486 wants to response a DCS Read command, which the MCU has sent to ILI9486.

Short Packet (SPa) is defined e.g.

- Data Identification (DI)
  - Virtual Channel (VC, DI [7…6]): 00b
  - Data Type (DT, DI [5…0]): 10 0010b
- Packet Data (PD)
  - Data 0: 45hex
  - Data 1: 32hex
- Error Correction Code (ECC)

This is defined on the Short Packet (SPa) as follows.



7.3.3.3. Communication Sequences

The communication sequences can be done on interface or packet levels between the MCU and ILI9486. This communication sequence description is for DSI data lanes (DSI-D0+/-) and it has been assumed that the needed low level communication is done on DSI clock lanes (DSI-CLK+/-) automatically.

Functions of the interface level communication are described on the following table.

Interface Mode	Abbreviation	Interface Action Description
Low Power	LP-11	Stop State
	LPDT	Low Power Data Transmission
	ULPS	Ultra-Low Power State
	RAR	Remote Application Reset
	TEE	Tearing Effect Event
	ACK	Acknowledge (No Error)
	BTA	Bus Turnaround
High Speed	HSDT	High speed Data Transmission

Functions of the packet level communication are described on the following table.

Interface Mode	Abbreviation	Packet Size	Interface Action Description
MCU	DCSW1-S	Short Packet	DCS Write, 1 Parameter
	DCSWN-S	Short Packet	DCS Write, No Parameter
	DCSW-L	Long Packet	DCS Write Long
	DCSRN-S	Short Packet	DCS Read, No Parameter
	SMRPS-S	Short Packet	Set Maximum Return Packet Size
	NP-L	Long Packet	Null Packet, No Data
	EoTP	Short Packet	End of Transmission Packet
ILI9486	AwER	Short Packet	Acknowledge with Error Packet
	DCSRR-L	Long Packet	DCS Read Long Response
	DCSRR1-S	Short Packet	DCS Read Short Response
	DCSRR2-S	Short Packet	DCS Read Short Response

7.3.3.3.1. DCS Write, 1 Parameter Sequence (DCSRR2-S)

A Short Packet (SPa) of "Display Command Set (DCS) Write, 1 Parameter (DCSW1-S)" is defined on chapter "7.3.3.2.1.3 Display Command Set (DCS) Write, 1 Parameter (DCSW1-S)" and example sequences, how this packet is used, is described on following tables.

DCS Write, 1 Parameter Sequence – Example 1						
Line	MCU		Information Direction	ILI9486		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	--	LP-11	→	--	--	Start
2	DCSW1-S	LPDT	→	--	--	
3	--	LP-11	→	--	--	End

DCS Write, 1 Parameter Sequence – Example 2						
Line	MCU		Information Direction	ILI9486		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	--	LP-11	→	--	--	Start
2	DCSW1-S	HSDT	→	--	--	
3	EoTP	HSDT	→			End of Transmission Packet
4	-	LP-11	→	--	--	End

DCS Write, 1 Parameter Sequence – Example 3						
Line	MCU		Information Direction	ILI9486		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	--	LP-11	→	--	--	Start
2	DCSW1-S	HSDT	→	--	--	
3	EoTP	HSDT	→	--	--	End of Transmission Packet
4	--	LP-11	→	--	--	
5	--	BTA	⇔	BTA	--	Interface Control Change from MCU to ILI9486
6	--	--	←	LP-11		If No Error → Go to Line 8 If Error Occurs → Go to Line 13
7						
8	--	--	←	ACK	--	No Error
9	--	--	←	LP-11	--	
10	--	BTA	⇔	BTA	--	Interface Control Change from the ILI9486 to MCU
11	--	LP-11	→	--	--	End
12						
13	--	--	←	LPDT	AwER	Error Report
14	--	--	←	LP-11	--	
15	--	BTA	⇔	BTA	--	
16	--	LP-11	→	--	--	End

7.3.3.3.2. DCS Write, No Parameter Sequence

A Short Packet (SPa) of "Display Command Set (DCS) Write, No Parameter (DCSWN-S)" is defined on chapter "7.3.3.2.1.2 Display Command Set (DCS) Write, No Parameter (DCSWN-S)" and example sequences, how this packet is used, is described on following tables.

DCS Write, No Parameter Sequence – Example 1						
Line	MCU		Information Direction	ILI9486		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	--	LP-11	→	--	--	Start
2	DCSWN-S	LPDT	→	--	--	
3	--	LP-11	→	--	--	End

DCS Write, No Parameter Sequence – Example 2						
Line	MCU		Information Direction	ILI9486		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	--	LP-11	→	--	--	Start
2	DCSWN-S	HSDT	→	--	--	
3	EoTP	HSDT	→			End of Transmission Packet
4	--	LP-11	→	--	--	End

DCS Write, 1 Parameter Sequence – Example 3						
Line	MCU		Information Direction	ILI9486		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	--	LP-11	→	--	--	Start
2	DCSWN-S	HSDT	→	--	--	
3	EoTP	HSDT	→	--	--	End of Transmission Packet
4	--	LP-11	→	--	--	
5	--	BTA	⇔	BTA	--	Interface Control Change from MCU to ILI9486
6	--	--	←	LP-11	--	If No Error → Go to Line 8 If Error Occurs → Go to Line 13
7						
8	--	--	←	ACK	--	No Error
9	--	--	←	LP-11	--	
10	--	BTA	⇔	BTA	--	Interface Control Change from the ILI9486 to MCU
11	--	LP-11	→	--	--	End
12						
13	--	--	←	LPDT	AwER	Error Report
14	--	--	←	LP-11	--	
15	--	BTA	⇔	BTA	--	
16	--	LP-11	→	--	--	End

7.3.3.3.3. DCS Write, No Parameter Sequence

A Long Packet (LPa) of "Display Command Set (DCS) Write Long (DCSW-L)" is defined on chapter "7.3.3.2.1.4 Display Command Set (DCS) Write Long (DCSW-L)" and example sequences, how this packet is used, is described on following tables.

DCS Write Long Sequence – Example 1						
Line	MCU		Information Direction	ILI9486		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	--	LP-11	→	--	--	Start
2	DCSW-L	LPDT	→	--	--	
3	--	LP-11	→	--	--	End

DCS Write Long Sequence – Example 2						
Line	MCU		Information Direction	ILI9486		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	--	LP-11	→	--	--	Start
2	DCSW-L	HSDT	→	--	--	
3	EoTP	HSDT	→			End of Transmission Packet
4	--	LP-11	→	--	--	End

DCS Write Long Sequence – Example 3						
Line	MCU		Information Direction	ILI9486		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	--	LP-11	→	--	--	Start
2	DCSW-L	HSDT	→	--	--	
3	EoTP	HSDT	→	--	--	End of Transmission Packet
4	--	LP-11	→	--	--	
5	--	BTA	⇔	BTA	--	Interface Control Change from MCU to ILI9486
6	--	--	←	LP-11	--	If No Error → Go to Line 8 If Error Occurs → Go to Line 13
7						
8	--	--	←	ACK	--	No Error
9	--	--	←	LP-11	--	
10	--	BTA	⇔	BTA	--	Interface Control Change from the ILI9486 to MCU
11	--	LP-11	→	--	--	End
12						
13	--	--	←	LPDT	AwER	Error Report
14	--	--	←	LP-11	--	
15	--	BTA	⇔	BTA	--	
16	--	LP-11	→	--	--	End

DCS Write Long Sequence – Example 4						
Line	MCU		Information Direction	ILI9486		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	--	LP-11	➔	--	--	Start
2	DCSW-L	HSDT	➔	--	--	Memory Write (2Ch)
3	DCSW-L	HSDT	➔	--	--	Memory Write Continue (3Ch)
4	DCSW-L	HSDT	➔	--	--	Memory Write Continue (3Ch)
5	DCSW1-S	HSDT	➔	--	--	Memory Write Continue (3Ch) with 1 Parameter
6	EoTP	HSDT	➔	--	--	End of Transmission Packet
7	--	LP-11	➔	--	--	End

Note: This is an example where is wanted to send image data in 4 packets.

7.3.3.3.4. DCS Read, No Parameter Sequence

A Short Packet (SPa) of "Display Command Set (DCS) Read, No Parameter (DCSRN-S)" is defined on chapter "7.3.3.2.1.5 Display Command Set (DCS) Read, No Parameter (DCSRN-S)" and example sequences, how this packet is used, is described on following tables.

DCS Read, No Parameter Sequence – Example 1						
Line	MCU		Information Direction	ILI9486		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	--	LP-11	→	--	--	Start
2	SMRPS-S	HSDT	→	--	--	Defined how many data byte is wanted to read : 1 byte
3	DCSW-L	HSDT	→	--	--	Wanted to get a response ID1 (DAh)
4	EoTP	HSDT	→			End of Transmission Packet
5	--	LP-11	→	--	--	
6	--	BTA	⇔	BTA	--	Interface Control Change from MCU to ILI9486
7	--	--	←	LP-11	--	If No Error → Go to Line 8 If Error Occurs → Go to Line 13
8						
9	--	--	←	LPDT	DCSRR1-S	Response 1 byte return
10	--	--	←	LP-11	--	
11	--	BTA	⇔	BTA	--	Interface Control Change from the ILI9486 to MCU
12	--	LP-11	→	--	--	End
13						
14	--	--	←	LPDT	AwER	Error Report
15	--	--	←	LP-11	--	
16	--	BTA	⇔	BTA	--	Interface control change from the ILI9486 to MCU
17	--	LP-11	→	--	--	End
18						
19	--	--	←	LPDT	DCSRR1-S	Responsed 1 byte return
20	--	--	←	LPDT	AwER	Error Report (Error is Corrected by ECC)
21	--	--	←	LP-11	--	
22	--	BTA	⇔	BTA	--	Interface Control Change from the ILI9486 to MCU
23	--	LP-11	→	--	--	End

DCS Read, No Parameter Sequence – Example 2						
Line	MCU		Information Direction	ILI9486		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	--	LP-11	→	--	--	Start
2	SMRPS-S	HSDT	→	--	--	Defined how many data byte is wanted to read : 200 bytes
3	DCSW-L	HSDT	→	--	--	Wanted to get a response "Memory Read" (2Eh)
4	EoTP	HSDT	→			End of Transmission Packet
5	--	LP-11	→	--	--	
6	--	BTA	⇔	BTA	--	Interface Control Change from MCU to ILI9486
7	--	--	←	LP-11	--	If No Error → Go to Line 8 If Error Occurs → Go to Line 13 If Error is corrected by ECC =>Go to Line 19
8						
9	--	--	←	LPDT	DCSRR-L	Response 200 byte return
10	--	--	←	LP-11	--	

11	--	BTA	⇔	BTA	--	Interface Control Change from the ILI9486 to MCU
12	--	LP-11	→	--	--	End
13						
14	--	--	←	LPDT	AwER	Error Report
15	--	--	←	LP-11	--	
16	--	BTA	⇔	BTA	--	Interface Control Change from MCU to ILI9486
17	--	LP-11	→	--	--	End
18						
19	--	--	←	LPDT		Responsed 200 bytes return
20	--	--	←	LPDT		Error Report (Error is Corrected by ECC)
21	--	--	←	LP-11	--	
22	--	BTA	⇔	BTA	--	Interface Control Change from the ILI9486 to MCU
23	--	LP-11	→	--	--	End

7.3.3.3.5. Null Packet, No Data Sequence

A Long Packet (LPa) of "Null Packet, No Data (NP-L)" is defined on chapter "7.3.3.2.1.6 Null Packet, No Data (NP-L)" and an example sequence, how this packet is used, is described on the following table.

Null Packet, No Data Sequence – Example						
Line	MCU		Information Direction	ILI9486		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	--	LP-11	→	--	--	Start
2	NP-L	HSDT	→	--	--	Only High Speed Data Transmission is used
3	EoTP	HSDT	→	--	--	End of Transmission Packet
4	--	LP-11	→	--	--	End

7.3.3.3.6. End of Transmission Packet

A Short Packet (SPa) of "End of Transmission Packet (EoTP)" is defined on chapter "7.3.3.2.1.7 End of Transmission Packet (EoTP)" and an example sequence, how this packet is used, is described on the following table.

End of Transmission Packet – Example						
Line	MCU		Information Direction	ILI9486		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	--	LP-11	→	--	--	Start
2	NP-L	HSDT	→	--	--	Only High Speed Data Transmission is used
3	EoTP	HSDT	→	--	--	End of Transmission Packet
4	--	LP-11	→	--	--	End

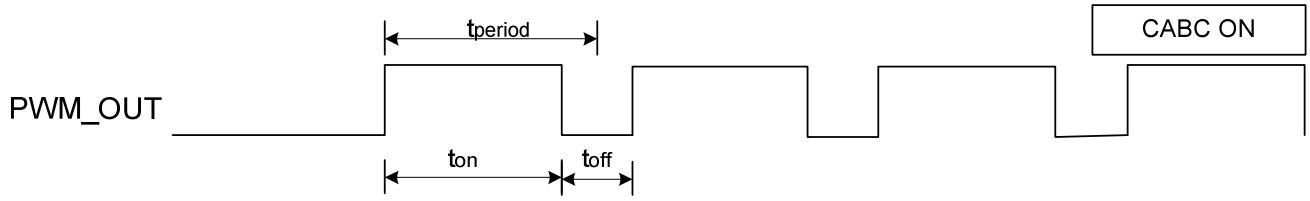
7.4. CABC (Content Adaptive Brightness Control)

ILI9486 provides a dynamic backlight control function as CABC (Content adaptive brightness control) to reduce the power consumption of the luminance source. ILI9486 will refer the gray scale content of display image to output a PWM waveform to LED driver for backlight brightness control. Content adaptation means that the content of gray sale can be increased while simultaneously lowering brightness of the backlight to achieve the same perceived brightness. The adjusted gray level scale and thus the power consumption reduction depend on the content of the image.

ILI9486 can calculate the backlight brightness level and send a PWM pulse to LED driver via PWM_OUT pin for backlight brightness control purpose. The PWM frequency can be adjusted by PWM_DIV parameters and the calculating equation as below:

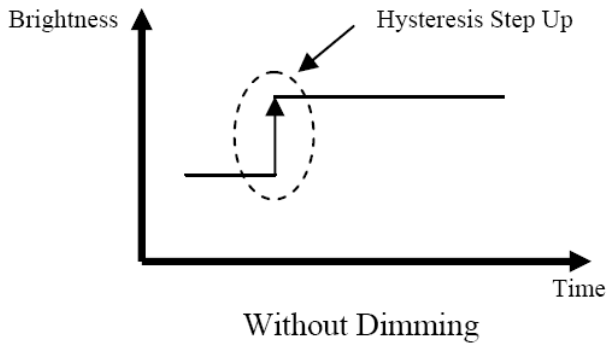
$$f_{PWM\_OUT} = \frac{18MHz}{(PWM\_DIV[7:0]+1)\times 255}$$

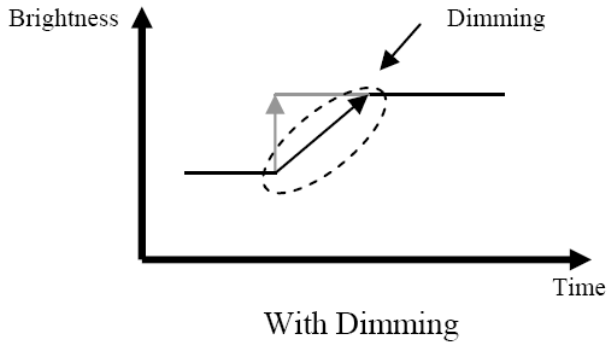
The figure in the following is the basic timing diagram which is applied ILI9486 to control LED driver.



Display Backlight Dimming Control

A dimming function (how fast to change the brightness from old to new level and what are brightness levels during the change) is used when changing from brightness level to another. This dimming function curve is the same in increment and decrement directions. The basic idea is described below.





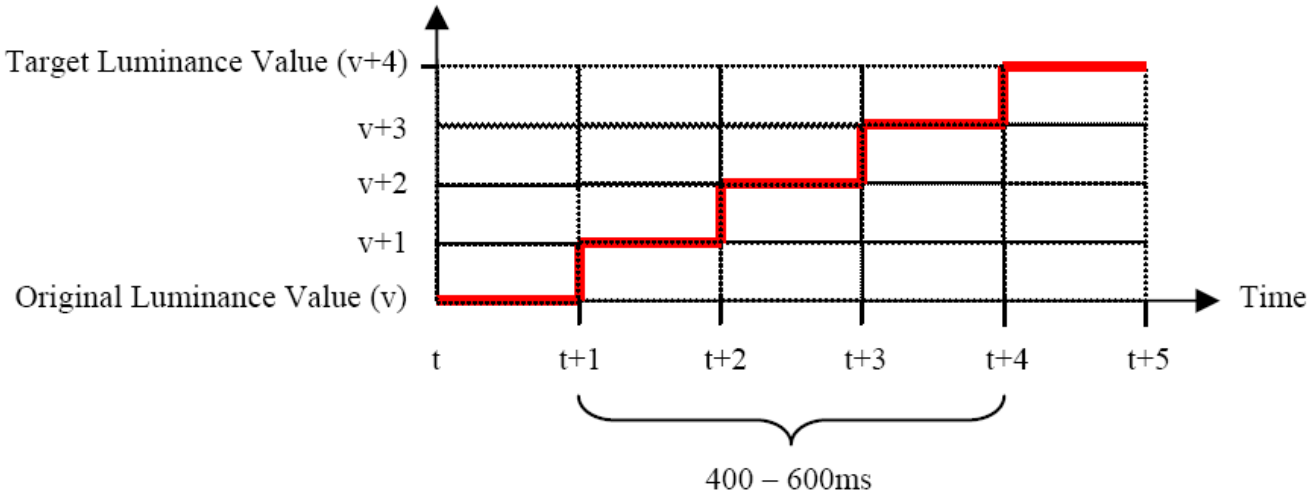
Dimming function can be enabled and disabled. See command “Write CTRL Display(53h), bit3(DD) for more information.

Dimming Requirment

Dimming function in the display module should be implemented so that 400 – 600ms is used for the transition between the original brightness value and the target brightness value. The transferring time steps between these two brightness values are equal making the transition linear.

The dimming function is working similarly in both upward and downward directions.

An upward example is illustrated below.

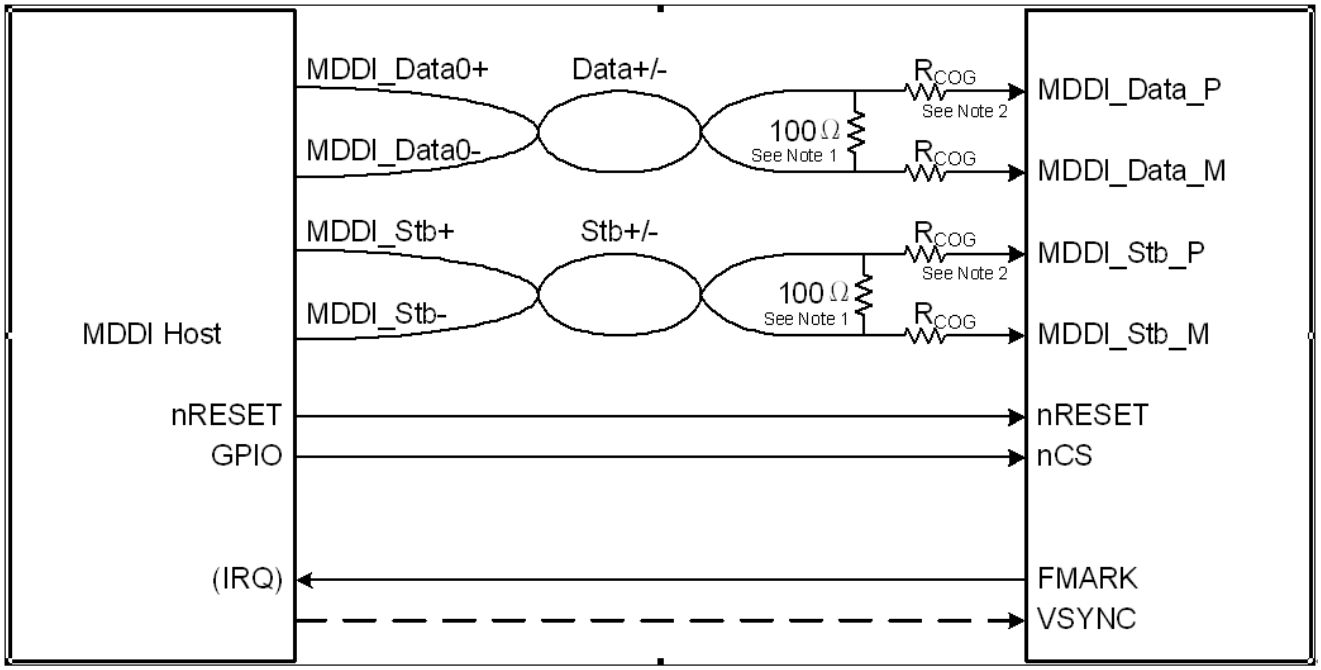


7.5. MDDI (Mobile Display Digital Interface)

MDDI (Mobile display digital interface) is a differential small amplitude serial interface for high-speed data transfer via following 4 lines: Stb+/- (MDDI_STB_P, MDDI_STB_M), Data+/- (MDDI_DATA_P, MDDI_DATA_M). The specifications of MDDI supported by the ILI9486 are compatible to the MDDI specifications disclosed by VESA, Video Electronics Standards Association. The following are the specifications particular to the ILI9486's MDDI.

ILI9486 MDDI Specifications

- MDDI Type-I
- High-speed, differential, small-amplitude data transfer via Stb+/-, Data+/- lines
- MDDI client: the ILI9486 enables direct connection to the base band (BB) chip without bridge chip
- Cost-performance optimized interface for mobile display systems
  1. Only internal mode (one client) and Forward Link are supported
  2. Hibernation mode to save power consumption
  3. Tearing-free moving picture display via FMARK/VSYNC interface
  4. Moving picture display with low power consumption, realized by the features 2 ~ 3
  5. Shutdown mode for saving power consumption in the standby state



Notes:

1. An external end resistor of 100 ohm is necessary between Data+ and Data- lines
2. Make the COG wiring resistances of Data+/-, Stb+/- lines as small as possible (RCOG < 10 ohm).

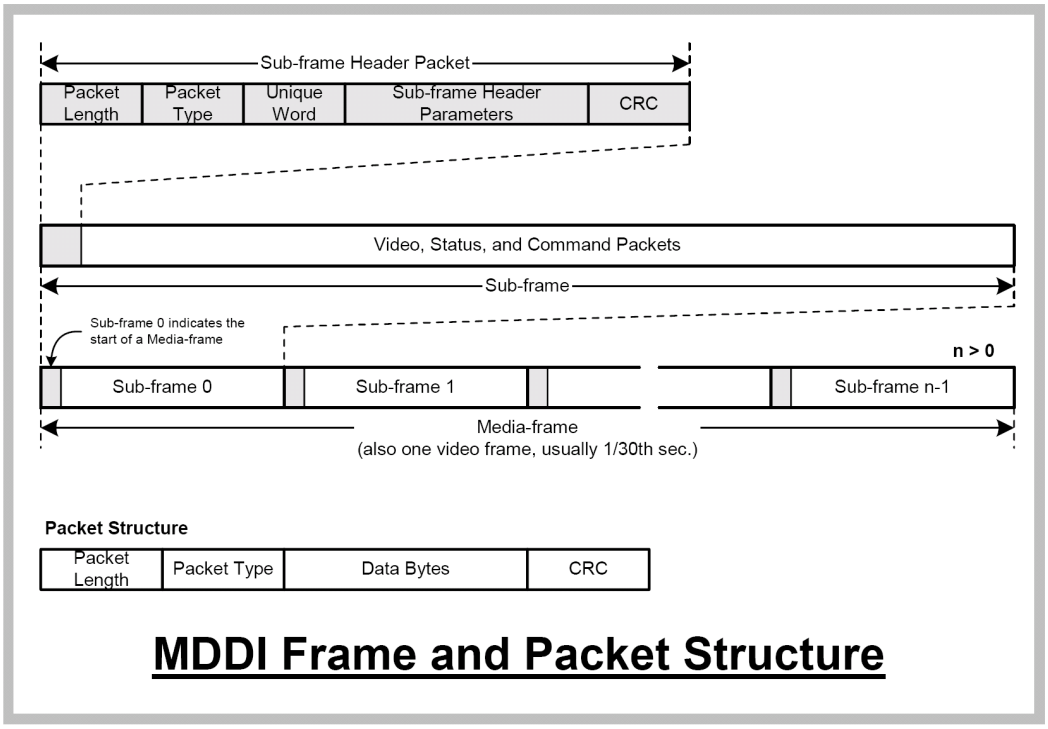
MDDI Link Protocol (Packets Supported by the ILI9486)

The MDDI Link Protocol of the ILI9486 is in line with the MDDI specifications disclosed by VESA. See the MDDI specifications by VESA for details on the MDDI Link Protocol.

The MDDI packets supported by the ILI9486 are as follows. Do not send packets not supported by the ILI9486 in the system incorporating the ILI9486.

Refer to MDDI packet structure, sub-frame header packet is placed in front of a sub-frame and some sub-frame construct media-frame together. The following table describes 9 types of packet which is supported in ILI9486.

Packet	Function	Direction
Sub-frame header packet	Header of each sub frame	Forward
Register access packet	Register setting	Forward
Video stream packet	Video data transfer	Forward
Filler packet	Fill empty packet space	Forward
Reverse link encapsulation packet	Reverse data packet	Reverse
Round-trip delay measurement packet	Host->client->host delay check	Forward/Reverse
Client capability packet	Capability of client check	Reverse
Client request and status packet	Information about client status	Reverse
Link shutdown packet	End of frame	Forward



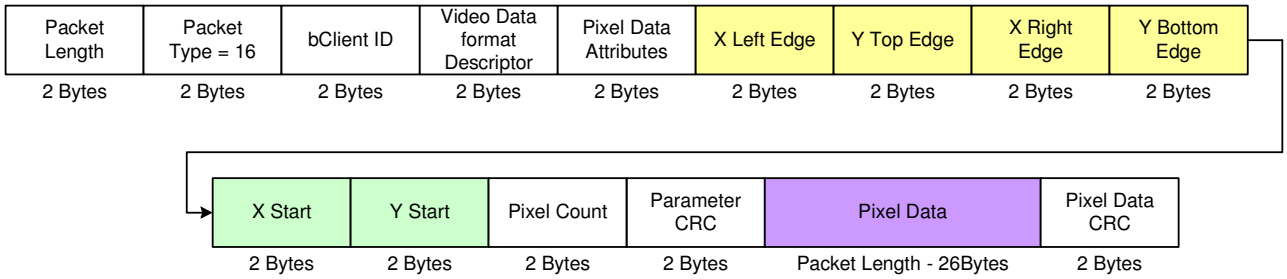
MDDI Frame and Packet Structure

Sub-Frame Header Packet

Bytes	0	1	2	3	4	5	6	7
1	Packet Length							
2	(0x0014)							
3	Packet Type							
4	(0x3bFF)							
5	Unique Word							
6	(0x005A)							
7	Reserved 1							
8	(0x0000)							
9	Sub-Frame Length							
10								
11								
12								
13	Protocol Version							
14	(0x0000)							
15	Sub-frame Count							
16								
17	Media-frame Count							
18								
19								
20								
21	CRC							
22	(0x0000)							

Video Stream Packet

The ILI9486 writes image data to RAM via Video Stream Packet. The window and RAM addresses are set via Register Access Packet.



	0	1	2	3	4	5	6	7
1	Packet Length							
2								
3	Packet Type							
4	(0x0010)							
5	bClient ID							
6	(0x0000)							
7	Video Data Format Descriptor							
8								
9	Bit0	Bit1	Pixel Data Attributes					
10								
11	X Left Edge							
12								
13	Y Top Edge							
14								
15	X Right Edge							
16								
17	Y Bottom Edge							
18								
19	X Start							
20								
21	Y Start							
22								
23	Pixel Count							
24								
25	Parameter CRC							
26								
	Pixel Data (Packet Length - 26 bytes)							
	CRC							

Note: The parameters colored in gray are not supported by the ILI9486.

Video Data Format Descriptor: sets the pixel data format. The ILI9486 supports only the following format. Set the same pixel format (bpp) as selected by DSS[1:0] in Video Data Format Descriptor.

[15:13]	[12]	[11:8]	[7:4]	[3:0]	
010	1	0x5	0x6	0x5	Packed 16bpp RGB format (R:G:B=5:6:5)
010	1	0x6	0x6	0x6	Packed 18bpp RGB format (R:G:B=6:6:6)
Others					Setting disabled

	MDDI Bytes n								MDDI Bytes (n+1)								MDDI Bytes (n+2)							
	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7
Packet	0	1	2	3	4	0	1	2	3	4	5	0	1	2	3	4	0	1	2	3	4	0	1	2
16bpp	Pixel 1 Blue					Pixel 1 Green						Pixel 1 Red					Pixel 2 Blue					Pixel 2		
Packet	0	1	2	3	4	5	0	1	2	3	4	5	0	1	2	3	4	5	0	1	2	3	4	5
18bpp	Pixel 2 Blue						Pixel 2 Green						Pixel 2 Red						Pixel 2 Blue					

Pixel Data Attributes: the image data sent vial Video Stream Packet is recognized as either the data for the main-panel or for the sub-panel according to the setting in [1:0] bits in this field.

Pixel Data Attributes	Bits[1:0]	Description
0x0000	00	The ILI9486 don't support the sub-panel display..
0x0001	01	Setting disabled
0x0002	10	Setting disabled
0x0003	11	The Video Stream Packet data is recognized as the data written in the ILI9486. The Video Stream Packet data is written in the ILI9486 and not outputted via sub-display interface.

Register Access Packet

Register Access Packet is used when setting instruction to the ILI9486.

	0	1	2	3	4	5	6	7
1	Packet Length							
2								
3	Packet Type							
4	(0x0092)							
5	bClient ID							
6	(0x0000)							
7	Read/Write Info.							
8								
9	Register Address							
10								
11								
12								
13	Parameter CRC							
14								
	Register Data (Packet Length - 14 bytes)							
	Register Dara CRC							

Note: The parameters colored in gray are not supported by the ILI9486.

Read/Write Info: Read or Write information in register access. The ILI9486 supports the following access setting.

Bits[15:14]	Bits[13:00]	Description
2'b00	0xn	Write one register by register access packet
2'b01	0xn	Reserved
2'b10	0xn	Read one register by register access packet
2'b11	0xn	Response to read

Register Address: The index of the register to be accessed is set in Register Address area and the Register Address Packet is directed to the ILI9486 or the sub display is determined by the setting in Register Address area.

Bits[31:16]	Description
16'h0000	The Register Access Packet is directed to the ILI9486 via main-display interface.
16'h0002 ~ 16'h7FFF	Setting disabled

Bits[15:0]	Description
16'h0000~FFFF	Bits [15:0] are used as index [15:0].

Register Data: The data for register access is written in Register Data. The length of Register Data will depends on the parameter length of command.

Example of Register Access Packet (e.g. write to the ILI9486)

	0	1	2	3	4	5	6	7
1	Packet Length					**(0x16)**		
2						(0x00)		
3	Packet Type					(0x92)		
4						(0x00)		
5	bClient ID					(0x00)		
6						(0x00)		
7	Read/Write Info.					(0x01)		
8						(0x00)		
9	Register Address					(index ID[7:0])		
10						(index ID[15:8])		
11						**(0x00) → Main Panel (ILI9486)**		
12						(0x00)		
13	Parameter CRC							
14								
15	Register Data List **(Various Length)**					1st Parameter		
16						0x00		
17						0x00		
18						0x00		
19						2nd Parameter		
20						0x00		
21						0x00		
22						0x00		
23	Parameter CRC							
24								

Note: The parameters colored in gray are not supported by the ILI9486.

Register Access Packet Restrictions

The ILI9486's internal RAM is accessible via Video Stream Packet. RAM access data is not included in Register Access Packet.

Link Shutdown Packet

This packet is used to bring Link to the Hibernation state.

	0	1	2	3	4	5	6	7
1	Packet Length							
2	(0X0014)							
3	Packet Type							
4	(0x0045)							
5	Parameter CRC							
6								
7	All Zeros (Type-I: 16 bytes)							
22								

Note: The parameters colored in gray are not supported by the ILI9486.

Filler Packet

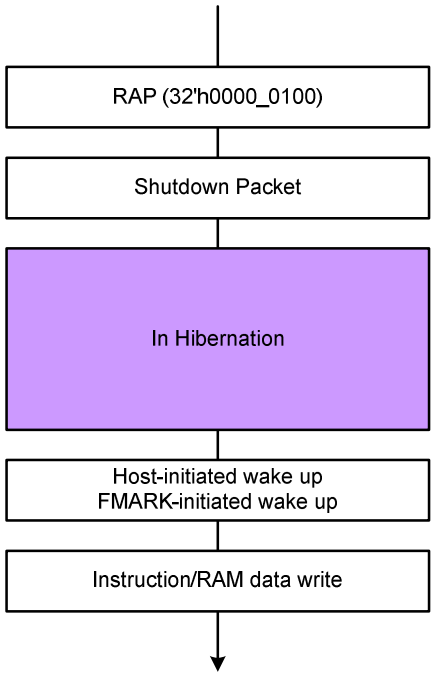
	0	1	2	3	4	5	6	7
1	Packet Length							
2								
3	Packet Type							
4	(0x0000)							
	Filler bytes (all zeros) (Packet Length: 4 bytes)							
	CRC							

Hibernation Setting

The ILI9486's Client MDDI supports Hibernation setting. There are two ways to cancel the Hibernation setting, which can be selected according to the condition of use.

Hibernation Cancellation	
Host-initiated wake up	In power-saving mode such as standby
TE-initiated wake up	Save power consumption in transferring moving picture data Host-initiated wake up triggered by the output from TE.

The Hibernation setting and cancellation sequence must be compatible with the VESA-MDDI specifications.



Host-Initiated Wake up from Hibernation

The host initialed wake up is described below without contention from the client trying to wake up at the same time. The following sequence of events is illustrated in the figures below!

A. The host sends a Link Shutdown Packet to inform the client that the link will transition to the low power hibernation state.

B. Following the CRC of the Link Shutdown Packet the host toggles MDDI_Stb for 64 cycles to allow processing in the client to finish before it stops MDDI_Stb from toggling which stops the recovered clock in the client device. During the interval the host initially sets MDDI_Data0 to a logic zero level, and then disables the MDDI_Data0 output in the range of 16 to 48 MDDI_Stb cycles (including output disable propagation delays) after the CRC. It may be desirable for the client to place its high-speed receivers for MDDI_Data0 and MDDI_Stb into a low power state any time after 48 MDDI_Stb cycles after the CRC and before point C.

C. The host enters the low power hibernation state by disabling the MDDI_Data0 and MDDI_Stb drivers and by placing the host controller into a low power hibernation state. It is also allowable for MDDI_Stb to be driven to a logic zero level or to continue toggling during hibernation. The client is also in the low power hibernation

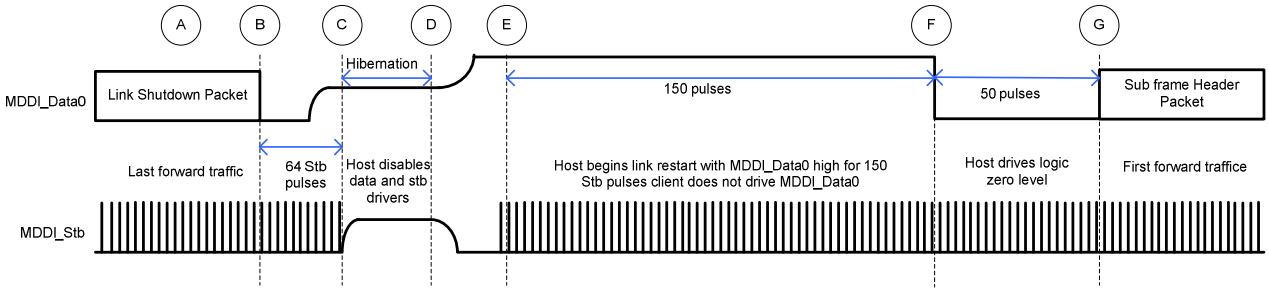
state.

D. After a while, the host begins the line restart sequence by enabling the MDDI_Data0 and MDDI_Stb driver outputs. The host drivers MDDI_Data0 to a logic one level and MDDI_Stb to a logic zero level for at least 200nsec after MDDI_Data0 reaches a valid logic one level and MDDI_Stb reaches a valid logic zero level before driving pulses on MDDI_Stb. This gives the client sufficient time to prepare to receive high speed pulses on MDDI_Stb. The client first detects the wake up pulse using a low power differential receiver having a +125mV input offset voltage.

E. The host drivers are fully enabled and MDDI_Data0 is being driven to a logic one level. The host begins to toggle MDDI_Stb in a manner consistent with having a logic zero level on MDDI_Data0 for a duration of 150 MDDI_Stb cycles.

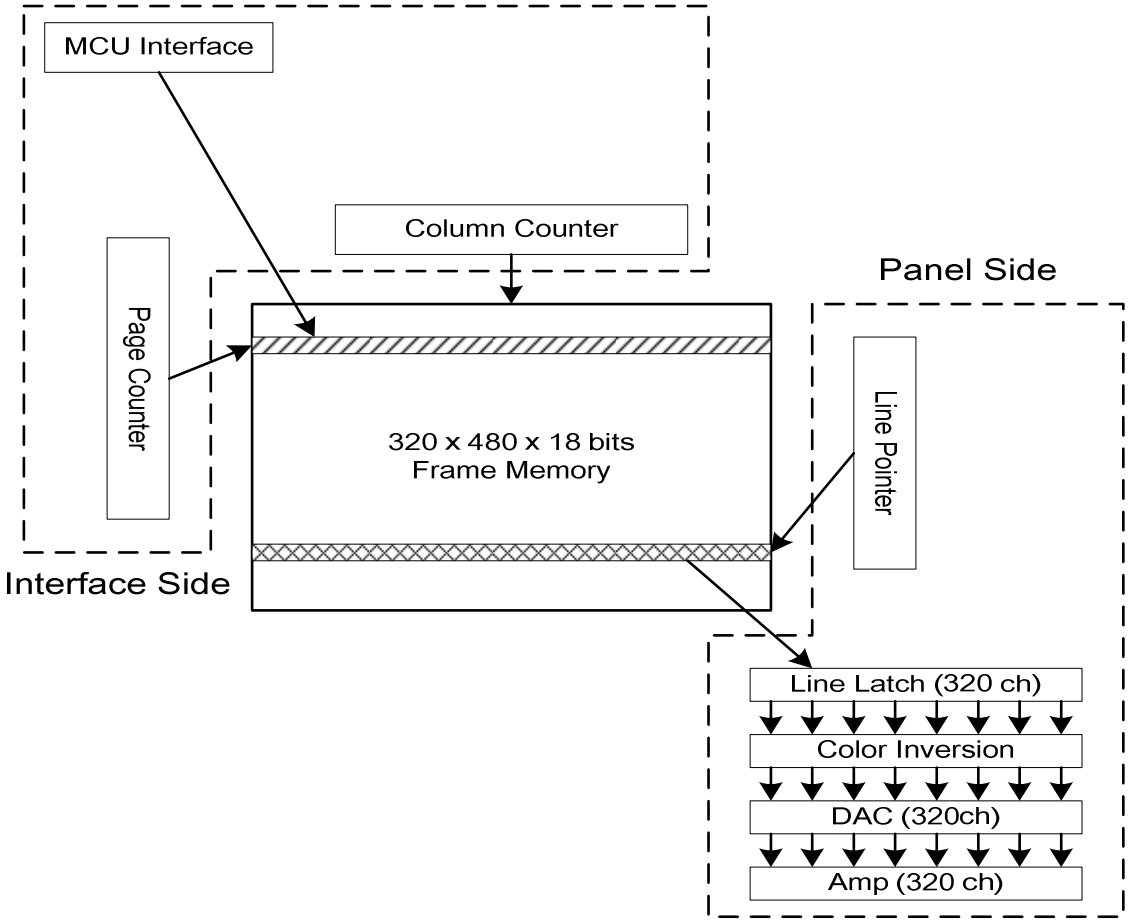
F. The host drives MDDI_Data0 to a logic zero level for 50 MDDI_Stb cycles. The client begins to look for the Sub frame Header Packet after MDDI_Data0 is at a logic zero level for 40 MDDI_Stb cycles.

G. The host begins to transmit data on the forward link by sending a Sub-frame Header packet. Beginning at point G the MDDI host generates MDDI_Stb based on the logic level on MDDI_Data0 so that proper data-strobe encoding commences form point G.



7.6. Display Data RAM (DDRAM)

The ILI9486 has an integrated 320x480x18-bit graphic type static RAM. This 345,600-byte memory allows storing a 320xRGBx480 image with an 18-bit resolution (262K-color). There will be no abnormal visible effect on the display when there is a simultaneous Panel Read and Interface Read or Write to the same location of the Frame Memory.

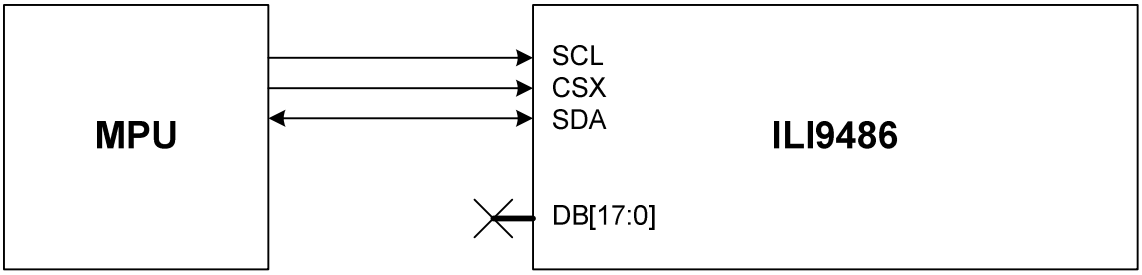


7.7. Display Data Format

ILI9486 supplies 18-/16-/9-/8-bit parallel MCU interface with 8080-series and 3-/4-line serial interface and 16-/18-bit parallel RGB interface. The parallel MCU interface and serial interface mode can be selected by external pins IM [2:0].

7.7.1. 3-line Serial Interface

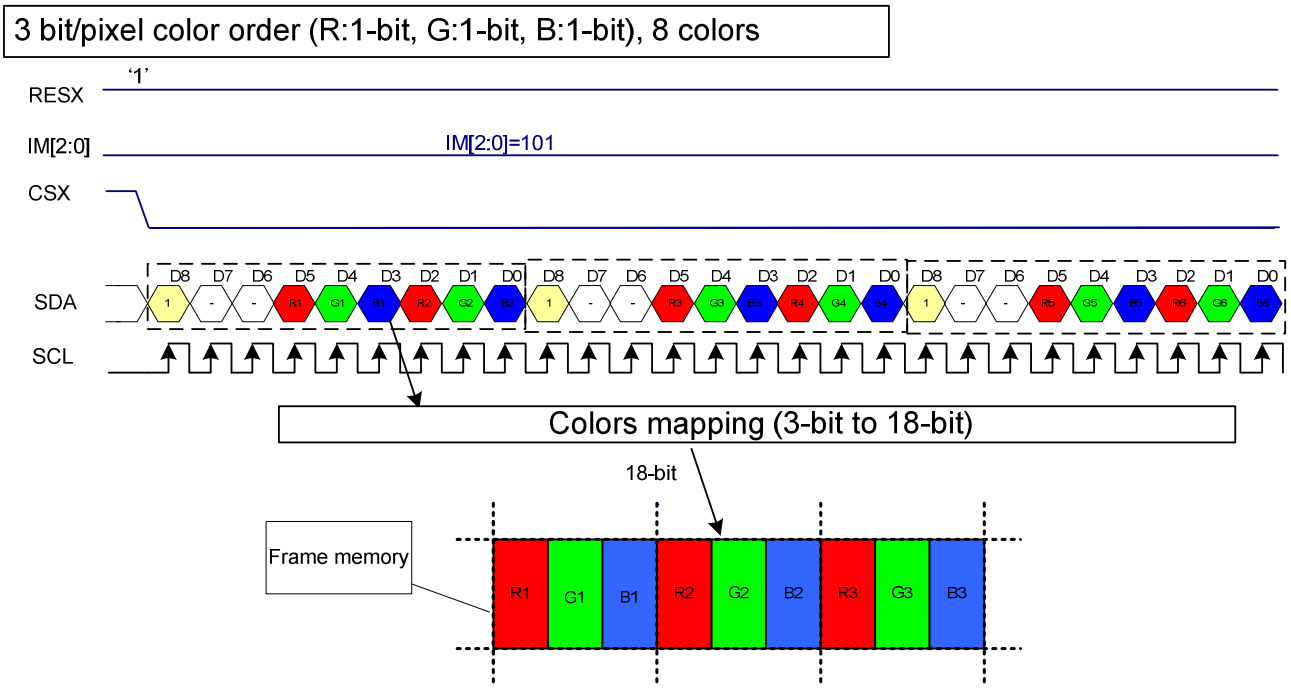
The 3-line/9-bit serial bus interface of ILI9486 can be used by setting external pin as IM [2:0] to "101". The figure in the following is the example of interface with 8080 microcomputer system interface.



In 3-line serial interface, different display data formats are available for two color depths supported by the LCM listed below.

-8 colors, RGB 1, 1, 1 -bits input

-262k colors, RGB 6, 6, 6 -bits input.



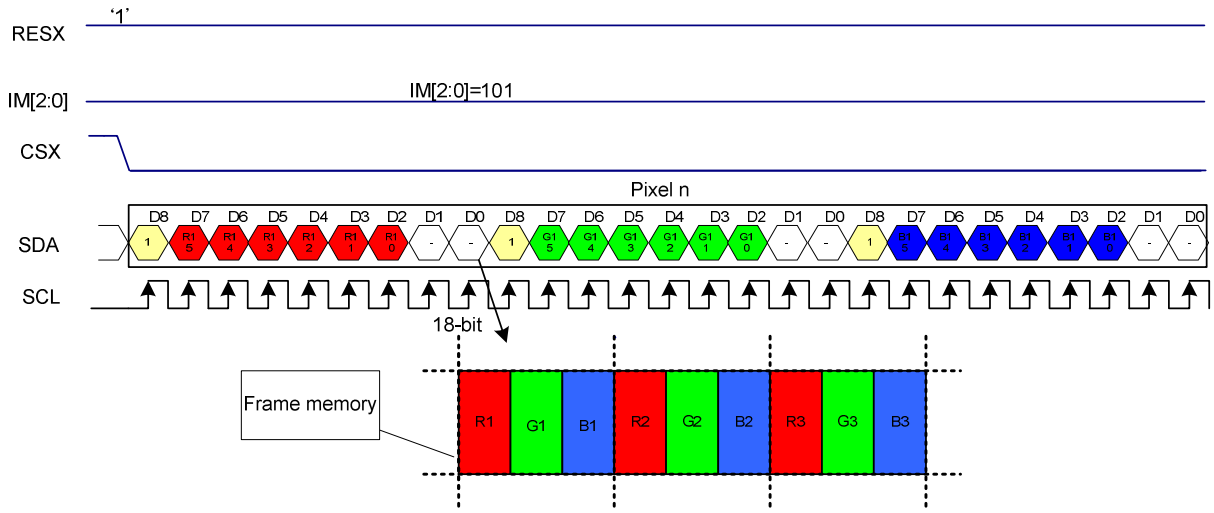
Note 1: The pixel data with 16-bit color depth information.

Note 2: The most significant bits are: Rx4, Gx5 and Bx4.

Note 3: The least significant bits are: Rx0, Gx0 and Bx0.

Note 4: '-'= Don't care – Leave these pins to Open.

18 bit/pixel color order (R:6-bit, G:6-bit, B:6-bit), 262,144 colors



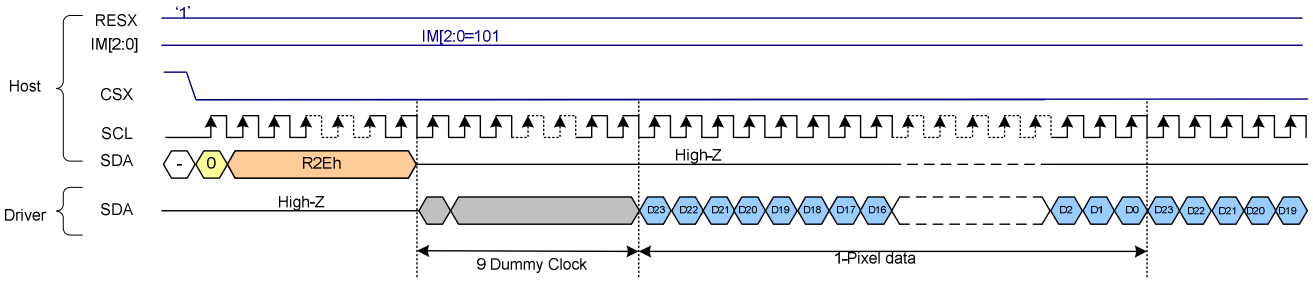
Note 1: The pixel data with 18-bit color depth information.

Note 2: The most significant bits are: Rx5, Gx5 and Bx5.

Note 3: The least significant bits are : Rx0, Gx0 and Bx0.

Note 4: '-'= Don't care - Leave these pins to Open.

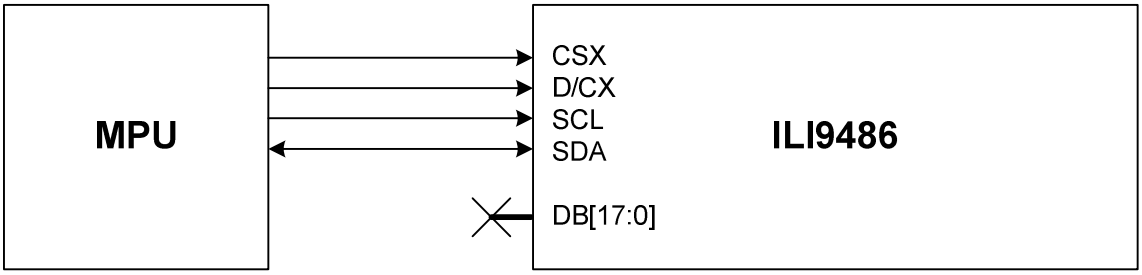
Read data through 3-line SPI mode



Note 1: '-'= Don't care – Leave these pins to Open.

7.7.2. 4-line Serial Interface

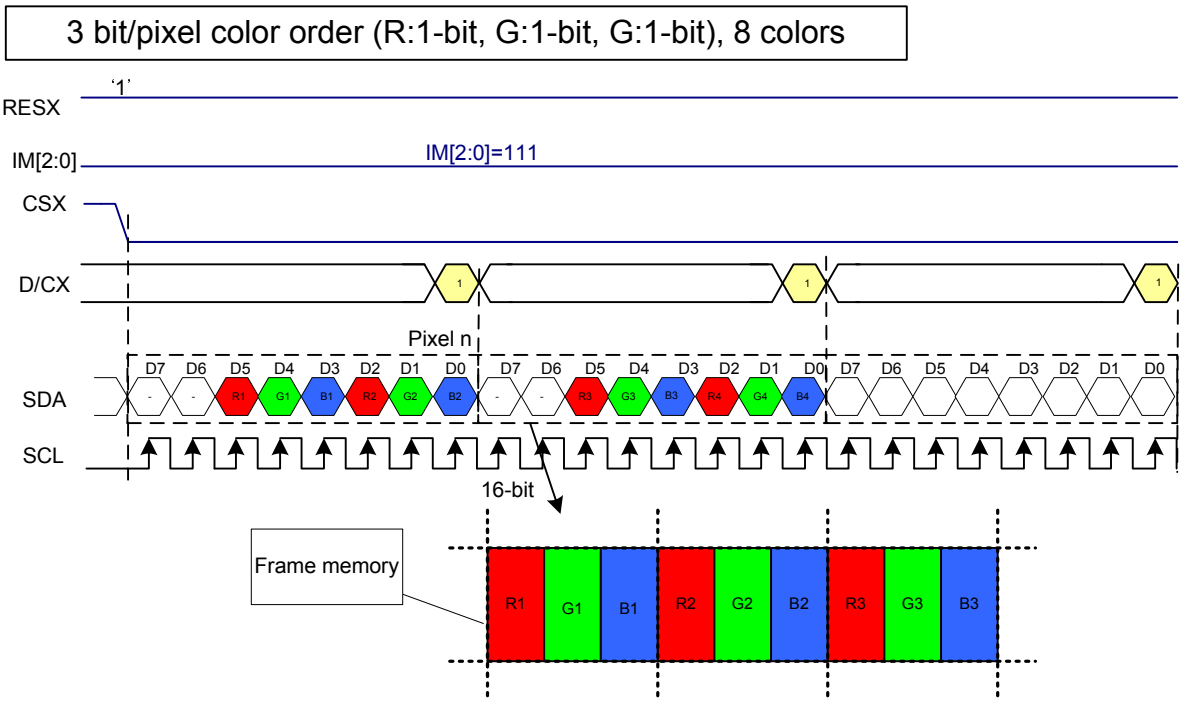
The 4-line/8-bit serial bus interface of ILI9486 can be used by setting external pin as IM [2:0] to “111”. The figure in the following is the example of interface with 8080 microcomputer system interface.



In 4-line serial interface, different display data formats are available for two color depths supported by the LCM listed below.

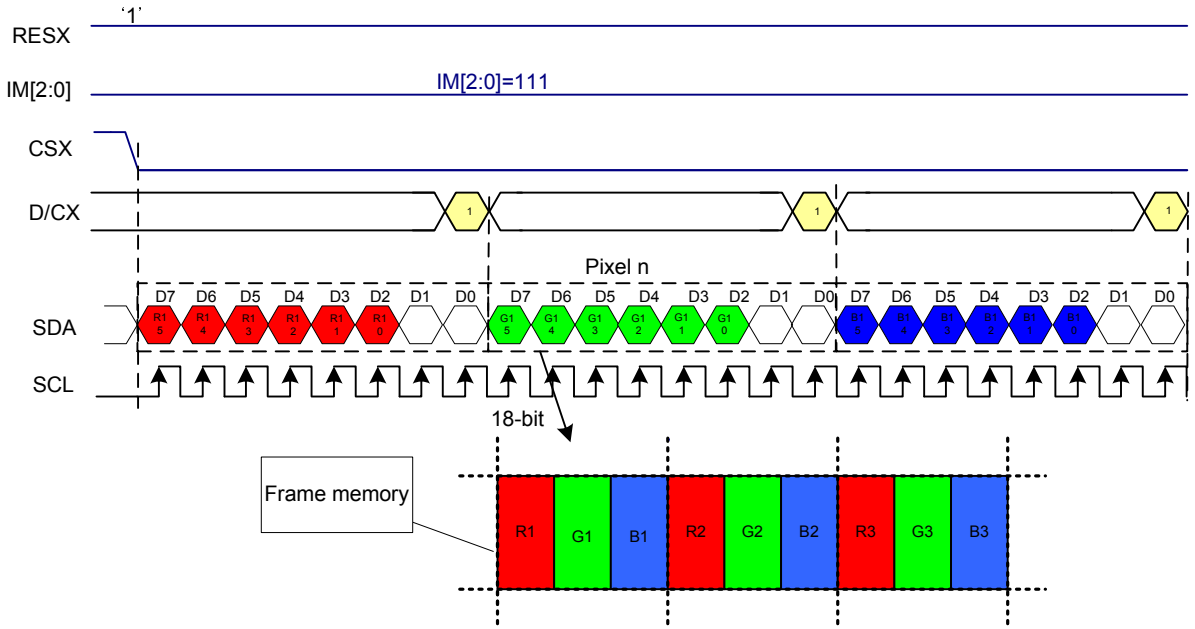
-8 colors, RGB 1, 1, 1 -bits input.

-262k colors, RGB 6, 6, 6 -bits input.



Note : ‘-‘= Don’t care – Leave these pins to Open.

18 bit/pixel color order (R:6-bit, G:6-bit, B:6-bit) , 262,144 colors



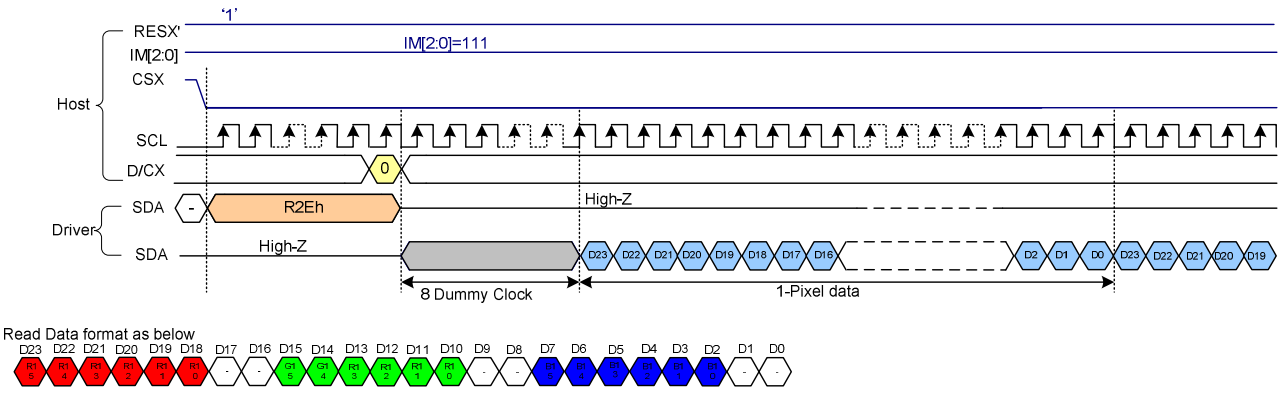
Note 1: The pixel data with 18-bit color depth information.

Note 2: The most significant bits are: Rx5, Gx5 and Bx5.

Note 3: The least significant bits are: Rx0, Gx0 and Bx0.

Note 4: '-'= Don't care – Leave these pins to Open.

Read data through 4-line SPI mode

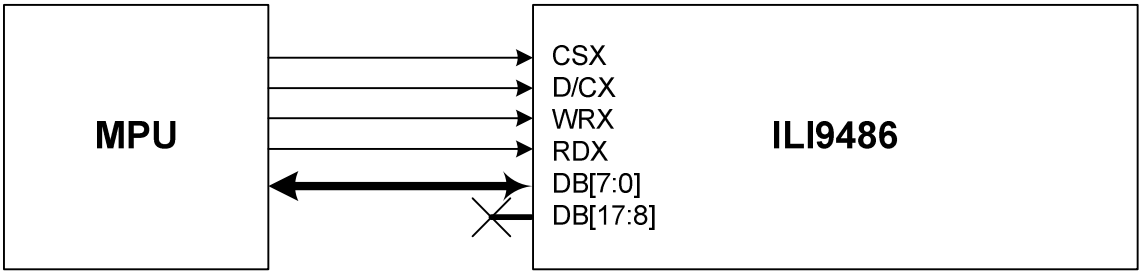


Note 1: '-'= Don't care – Leave these pins to Open.

7.7.3. 8-bit Parallel MCU Interface

The 8080-system 8-bit parallel bus interface of ILI9486 can be used by setting external pin as IM [2:0] to “011”.

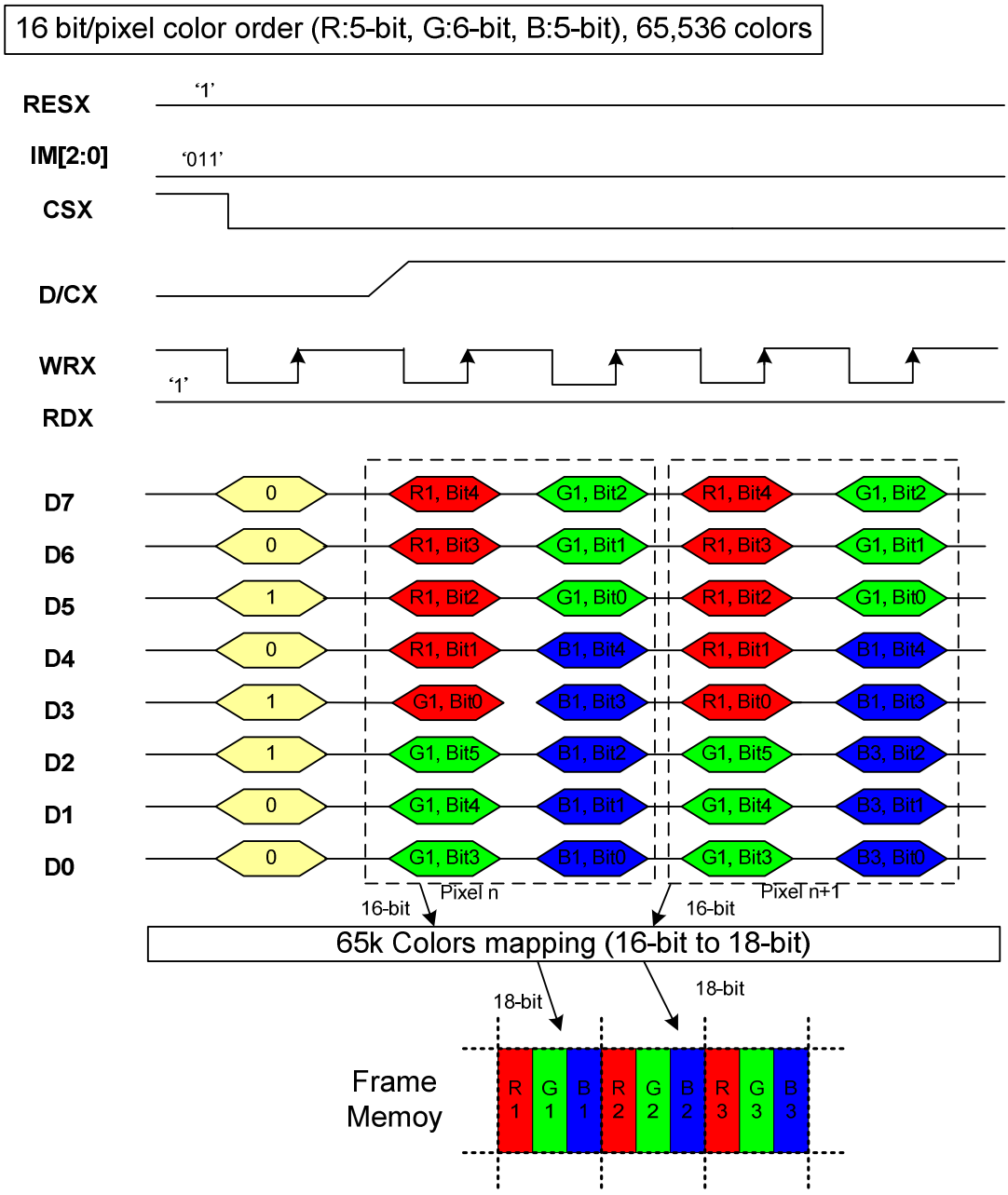
The figure in the following is the example of interface with 8080 microcomputer system interface.



Different display data formats are available for two color depths supported by listed below.

- 65K-Colors, RGB 5, 6, 5 -bits input data.
- 262K-Colors, RGB 6, 6, 6 -bits input data.

7.7.3.1. 8-bit Data Bus for 16-bit/pixel (RGB 5-6-5 bits input), 65K-color

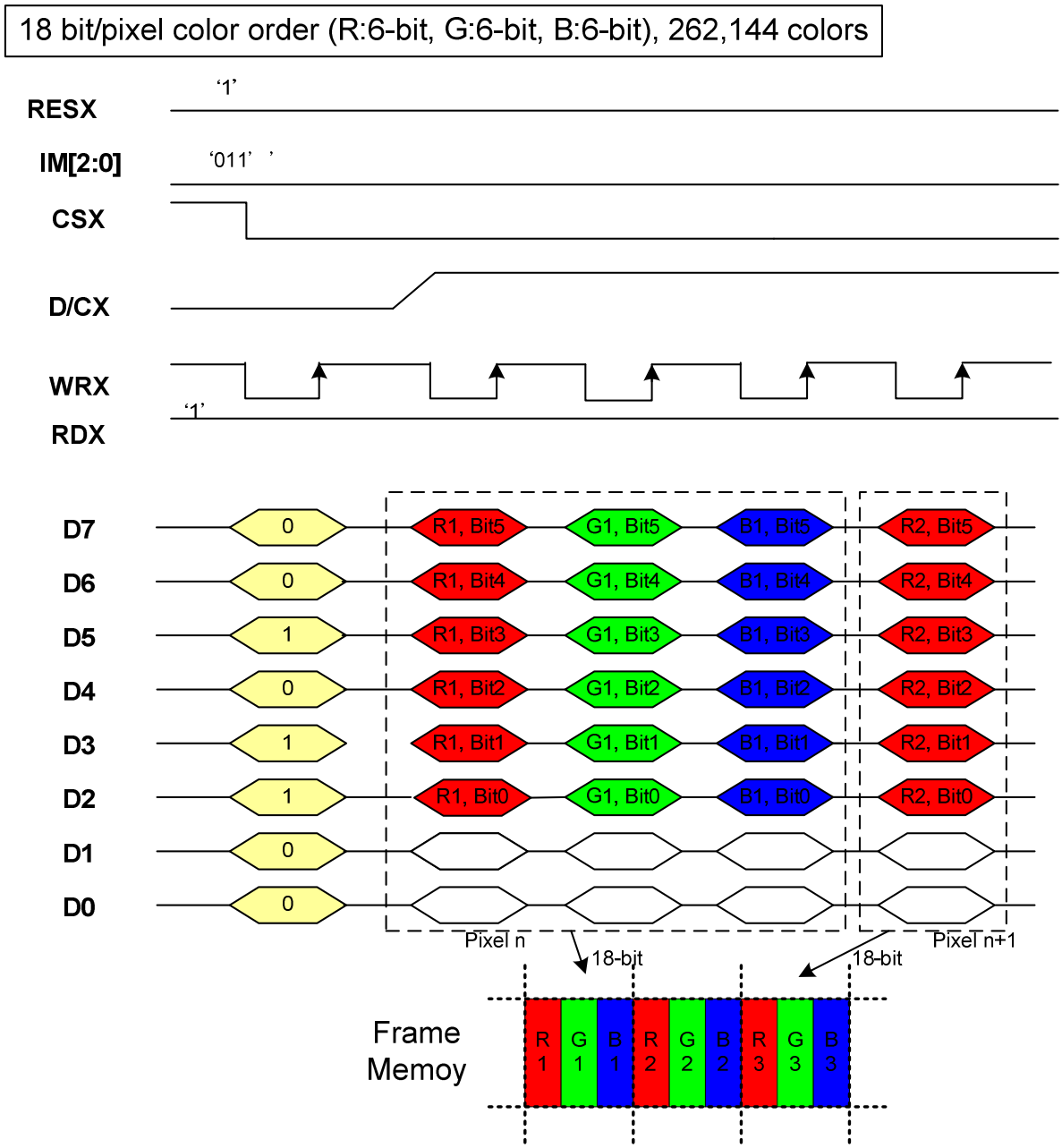


Note 1: The data order is as follows, MSB=D7, LSB=D0 and picture data is MSB=Bit 5, LSB=Bit 0 for Green data and MSB=Bit 4, LSB=Bit0 for Red and Blue data.

Note 2: 2-times transfer is used to transmit 1 pixel data with the 16-bits color depth information.

Note 3: '-'= Don't care – Leave these pins to Open.

7.7.3.2. 8-bit Data Bus for 18-bit/pixel (RGB 6-6-6 bits input), 262K-color



Note 1: The data order is as follows, MSB=D7, LSB=D0 and picture data is MSB=Bit 5, LSB=Bit 0 for Green, Red and Blue data.

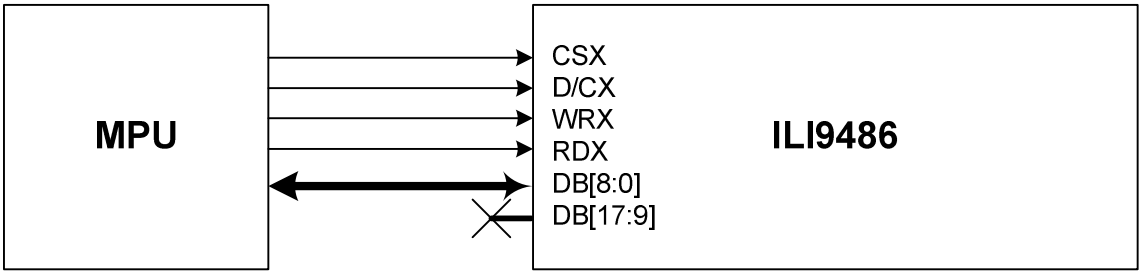
Note 2: 3-times transfer is used to transmit 1 pixel data with the 18-bits color depth information.

Note 3: '-'= Don't care – Leave these pins to Open.

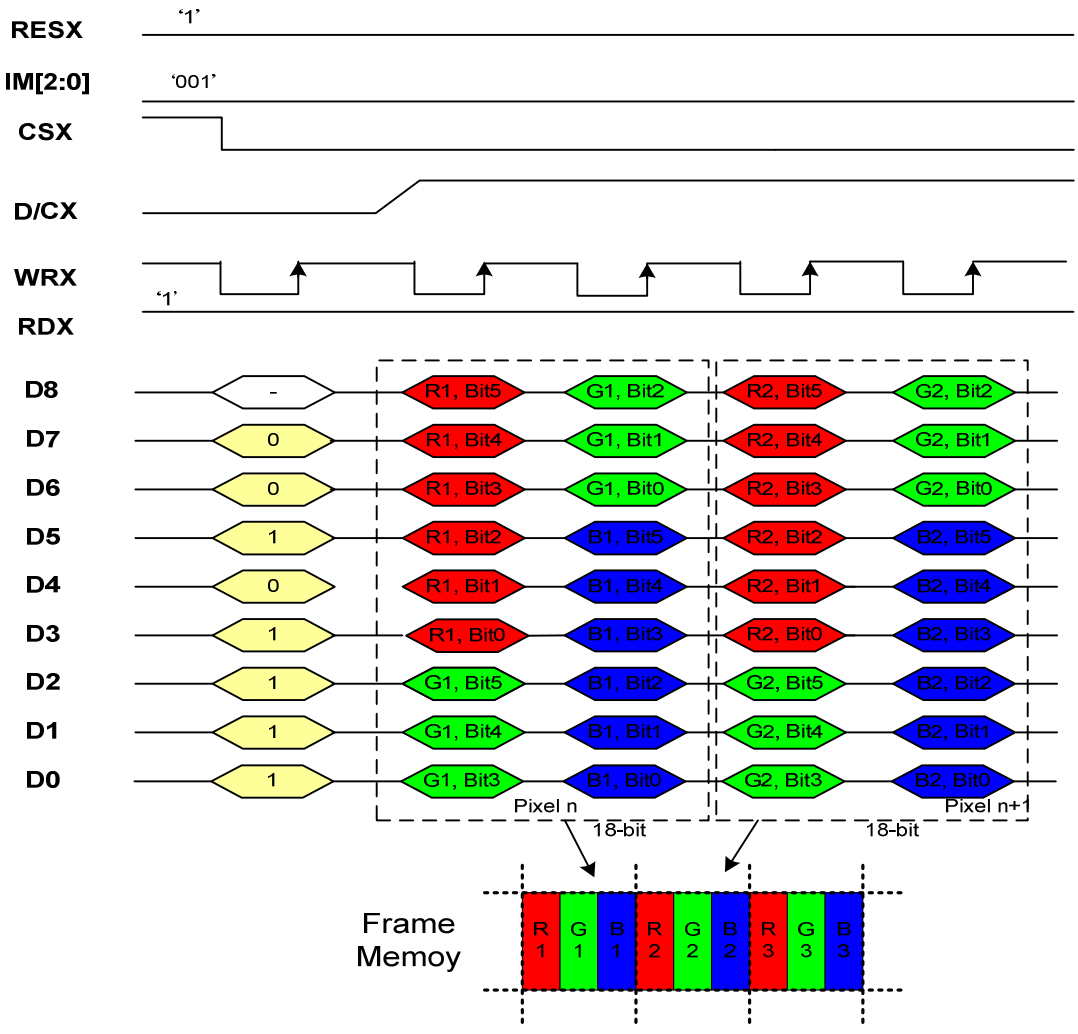
7.7.4. 9-bit Parallel MCU Interface

The 8080-system 9-bit parallel bus interface of ILI9486 can be used by setting external pin as IM [2:0] to “001”.

The figure in the following is the example of interface with 8080 microcomputer system interface.



18 bit/pixel color order (R:6-bit, G:6-bit, B:6-bit), 262,144 colors



Note 1: The data order is as follows, MSB=D8, LSB=D0 and picture data is MSB=Bit 5, LSB=Bit 0 for Green, Red and Blue data.

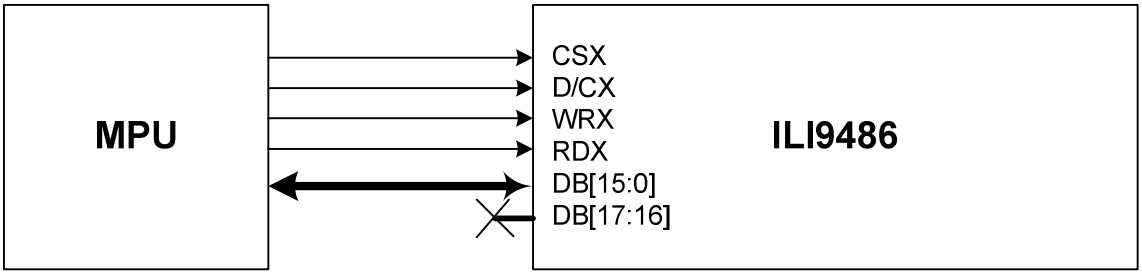
Note 2: 2-times transfer is used to transmit 1 pixel data with the 18-bits color depth information.

Note 3: '-'= Don't care – Leave these pins to Open.

7.7.5. 16-bit Parallel MCU Interface

The 8080-system 16-bit parallel bus interface of ILI9486 can be used by setting external pin as IM [2:0] to “010”.

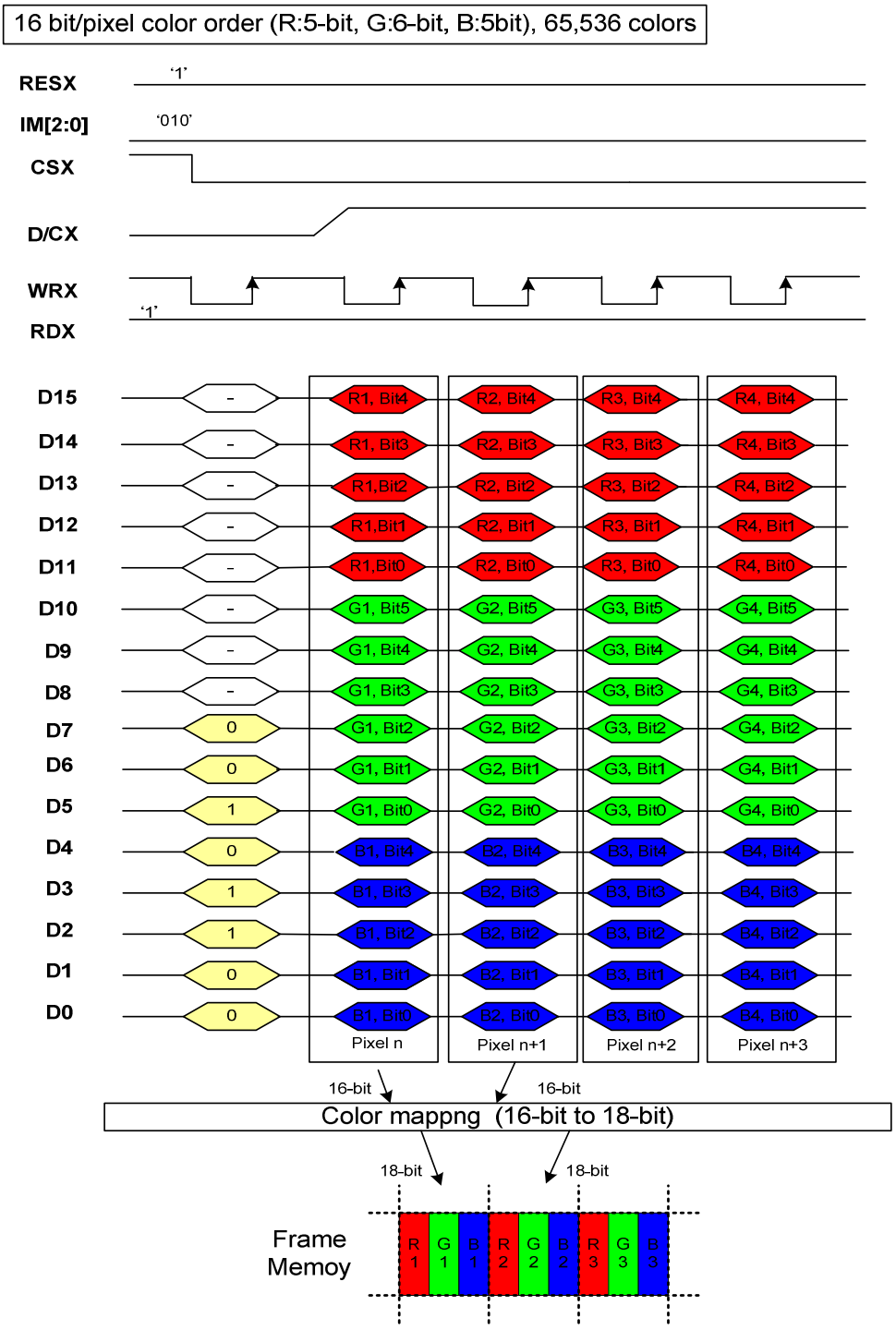
The figure in the following is the example of interface with 8080 microcomputer system interface.



Different display data formats are available for two colors depth supported by listed below.

- 65K-Colors, RGB 5, 6, 5 -bits input data.
- 262K-Colors, RGB 6, 6, 6 -bits input data.

7.7.5.1. 16-bit Data Bus for 16-bit/pixel (RGB 5-6-5 bits input), 65K-color

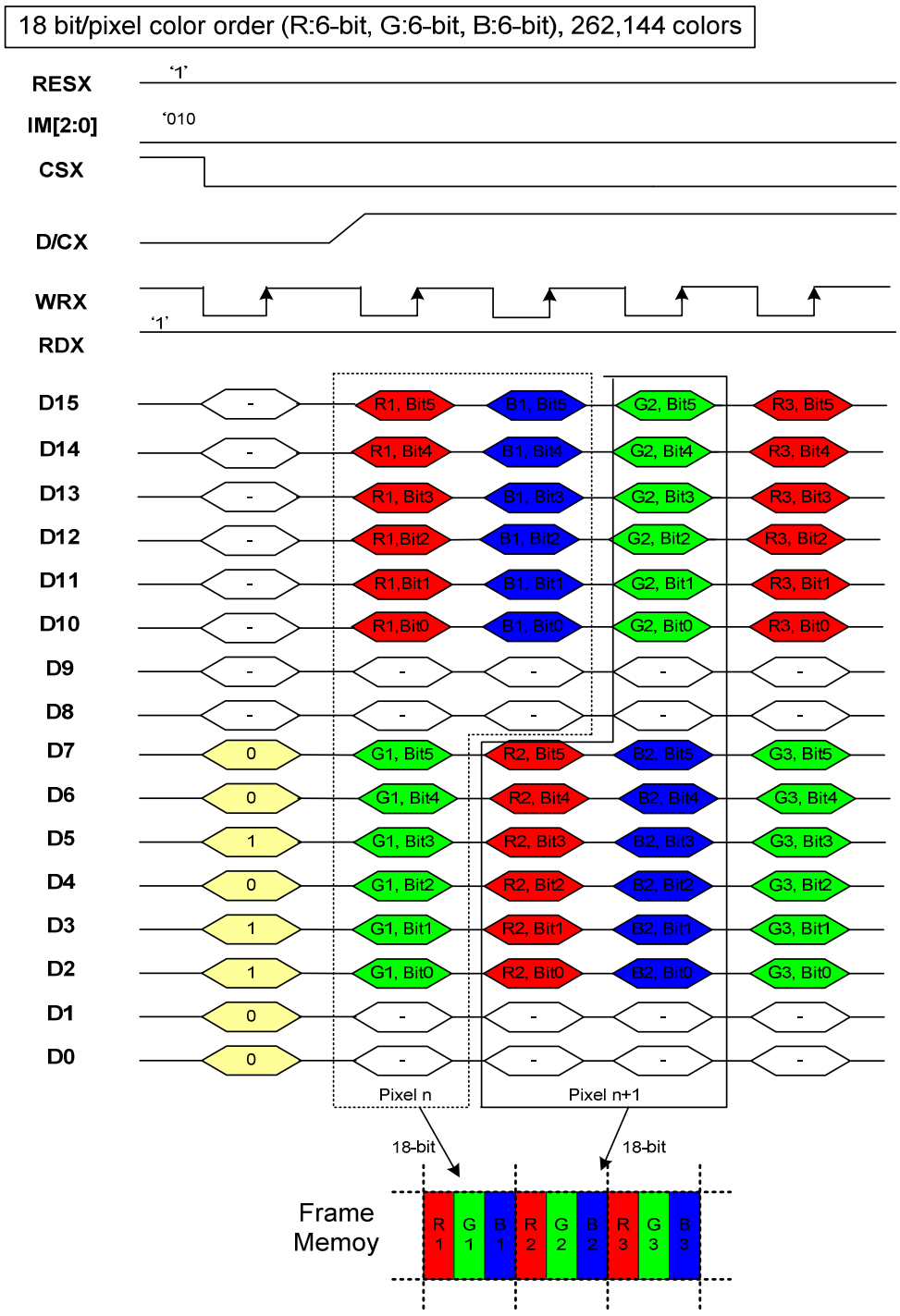


Note 1: The data order is as follows, MSB=D15, LSB=D0 and picture data is MSB=Bit 5, LSB=Bit 0 for Green data and MSB=Bit 4, LSB=Bit0 for Red and Blue data.

Note 2: 1-times transfer is used to transmit 1 pixel data with the 16-bits color depth information.

Note 3: '-'= Don't care – Leave these pins to Open.

7.7.5.2. 16-bit Data Bus for 18-bit/pixel (RGB 6-6-6 bits input), 262K-color



Note 1: The data order is as follows, MSB=D15, LSB=D0 and picture data is MSB=Bit 5, LSB=Bit 0 for Green, Red and Blue data.

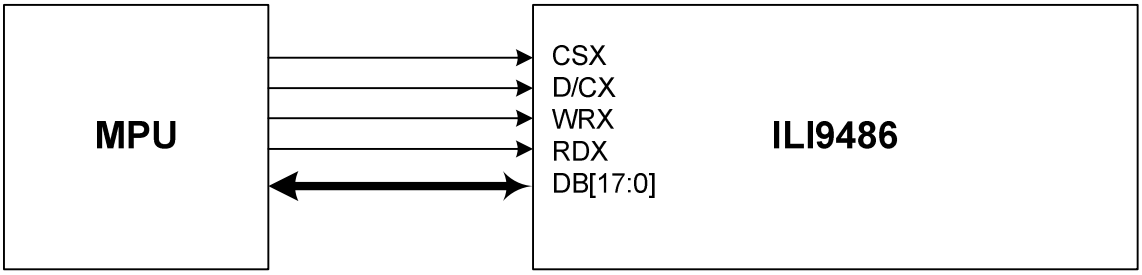
Note 2: 2-times transfer is used to transmit 1 pixel data with the 18-bits color depth information.

Note 3: '-'= Don't care – Leave these pins to Open.

7.7.6. 18-bit Parallel MCU Interface

The 8080-system 18-bit parallel bus interface of ILI9486 can be used by setting external pin as IM [2:0] to “000”.

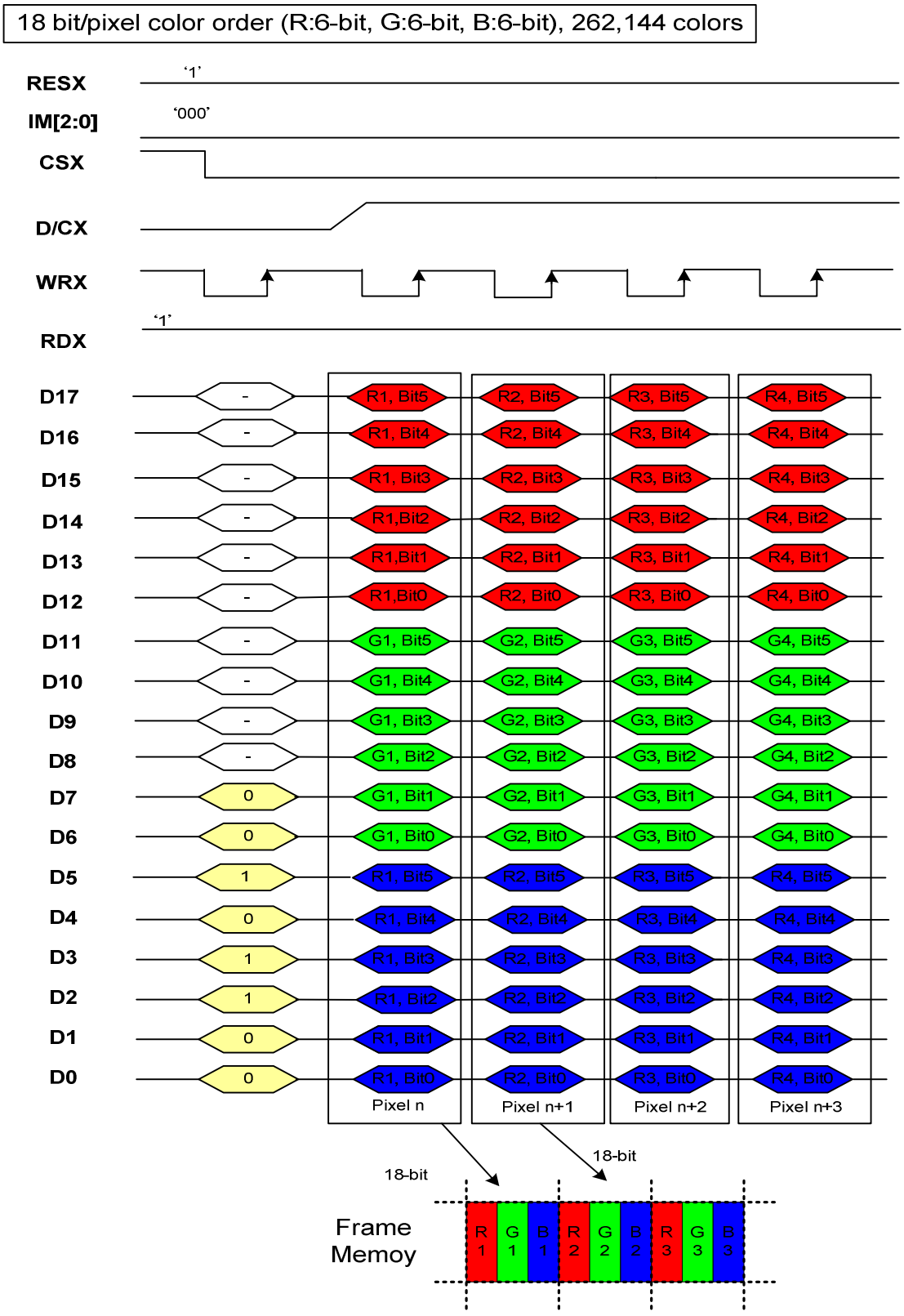
The figure in the following is the example of interface with 8080 microcomputer system interface.



Different display data formats are available for one color depth only supported by listed below.

- 262K-Colors, RGB 6, 6, 6 -bits input data.

7.7.6.1. 18-bit Data Bus for 18-bit/pixel (RGB 6-6-6 bits input), 262K-color



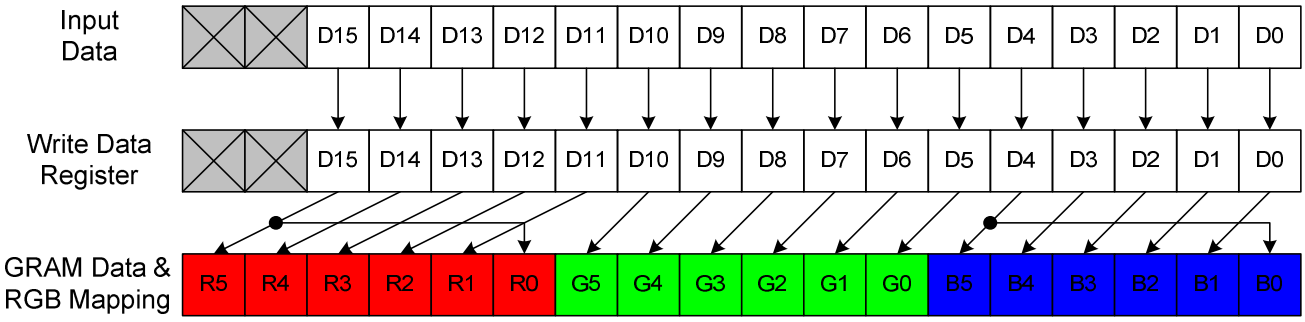
Note 1: The data order is as follows, MSB=D17, LSB=D0 and picture data is MSB=Bit 5, LSB=Bit 0 for Green and MSB=Bit4, LSB=Bit0 for Red and Blue data.

Note 2: 1-times transfer is used to transmit 1 pixel data with the 16-bits color depth information.

Note 3: '-'= Don't care – Leave these pins to Open.

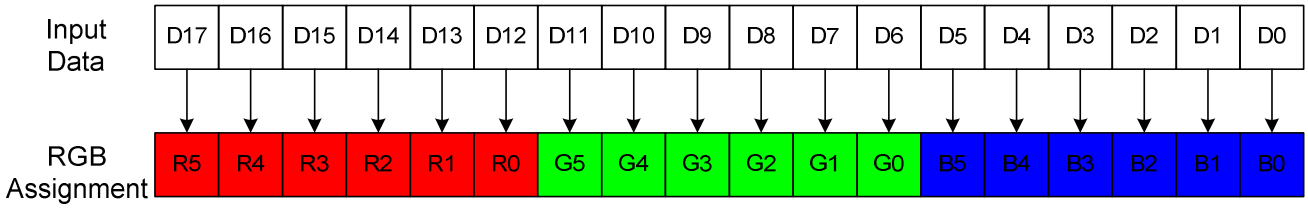
7.7.7. 16-bit Parallel RGB Interface

The 16-bit RGB interface is selected by setting the DPI[2:0] bits to “101”. The display operation is synchronized with VSYNC, HSYNC and DOTCLK signals. The display data are transferred to the internal GRAM in synchronization with the display operation via 16-bit RGB data bus (D[15:0]). Both D17 and D16 pins must be left to OPEN for ensure normally operation. Registers can be set by the system interface.



7.7.8. 18-bit Parallel RGB Interface

The 18-bit RGB interface is selected by setting the DPI[2:0] bits to “110”. The display operation is synchronized with VSYNC, HSYNC and DOTCLK signals. The display data are transferred to the internal GRAM in synchronization with the display operation via 18-bit RGB data bus (DB[17:0]) according to the data enable signal (ENABLE). Registers can be set by the system interface.

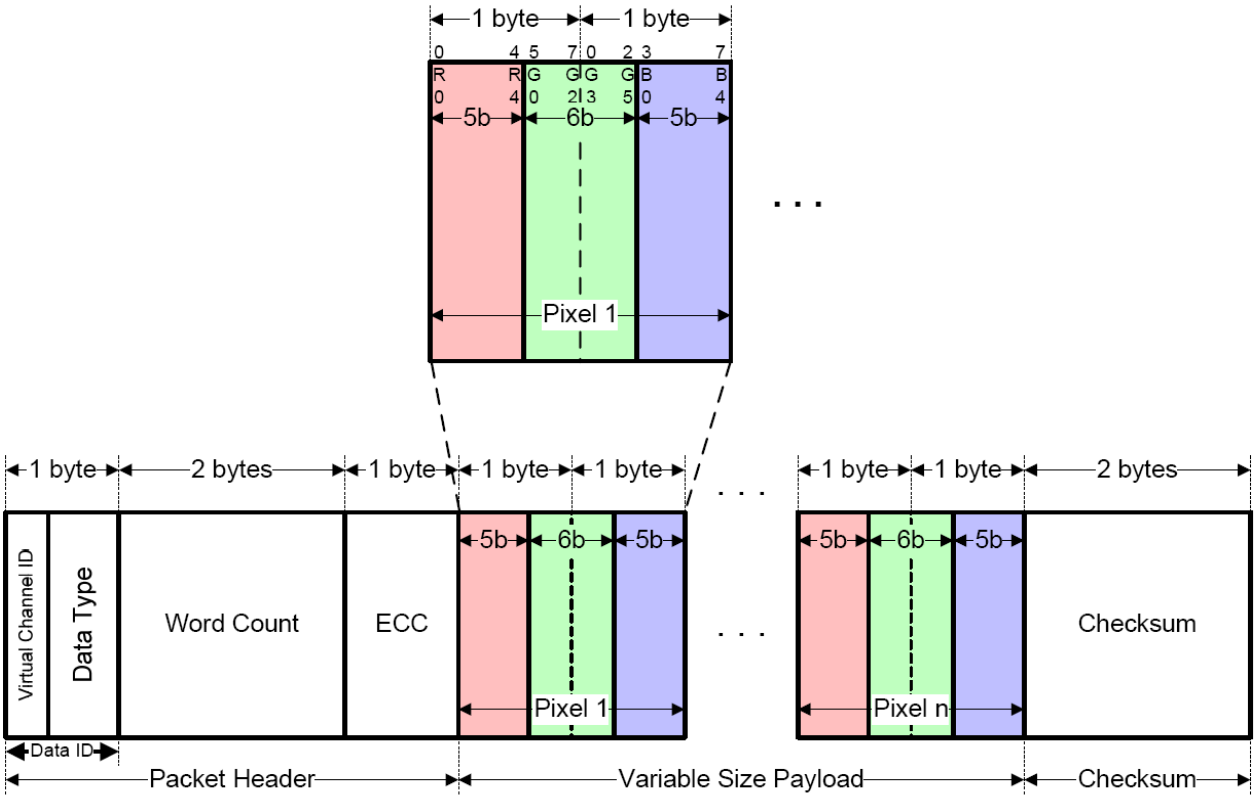


7.7.9. MIPI - DSI

Packed Pixel Stream 16-Bit Format is a Long packet used to transmit image data formatted as 16-bit pixels to a Video Mode display module. The packet consists of the DI byte, a two-byte WC, an ECC byte, a payload of length WC bytes and a two-byte checksum. Pixel format is five bits red, six bits green, five bits blue, in that order. Note that the “Green” component is split across two bytes. Within a color component, the LSB is sent first, the MSB last.

With this format, pixel boundaries align with byte boundaries every two bytes. The total line width (displayed plus non-displayed pixels) should be a multiple of two bytes.

Normally, ILI9486 has no frame buffer of its own, so all image data shall be supplied by the host processor at a sufficiently high rate to avoid flicker or other visible artifacts.

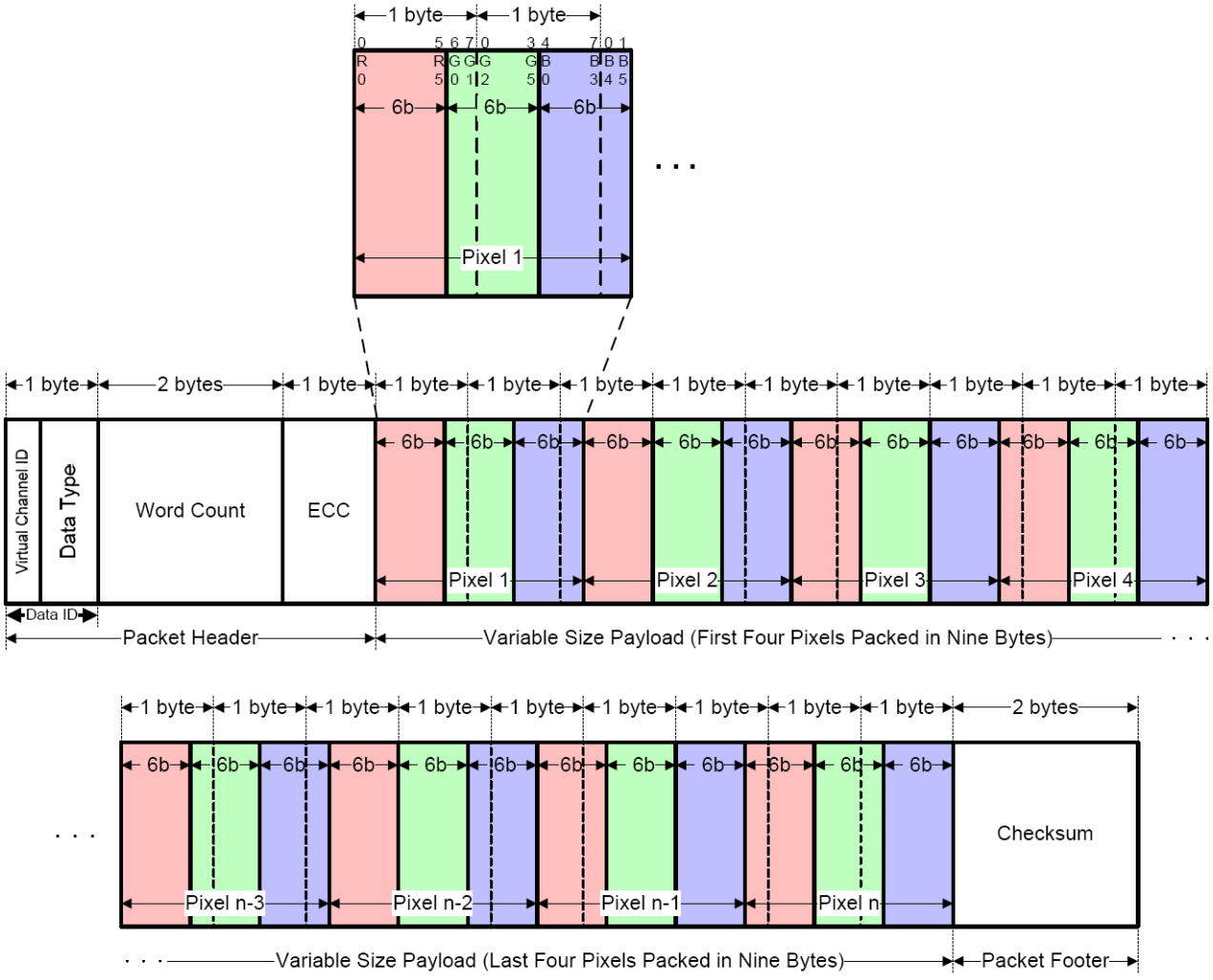


7.7.10. MIPI – 18-bit per Pixel, Long packet, Data Type = 01 1110 (1Eh)

Packed Pixel Stream 18-Bit Format (Packed) is a Long packet. It is used to transmit RGB image data formatted as pixels to a Video Mode display module that displays 18-bit pixels The packet consists of the DI byte, a two-byte WC, an ECC byte, a payload of length WC bytes and a two-byte Checksum. Pixel format is red (6 bits), green (6 bits) and blue (6 bits), in that order. Within a color component, the LSB is sent first, the MSB last.

Note that pixel boundaries only align with byte boundaries every four pixels (nine bytes). Preferably, display modules employing this format have a horizontal extent (width in pixels) evenly divisible by four, so no partial bytes remain at the end of the display line data. If the active (displayed) horizontal width is not a multiple of four pixels, the transmitter shall send additional fill pixels at the end of the display line to make the transmitted width a multiple of four pixels. The receiving peripheral shall not display the fill pixels when refreshing the display device. For example, if a display device has an active display width of 399 pixels, the transmitter should send 400 pixels in one or more packets. The receiver should display the first 399 pixels and discard the last pixel of the transmission.

With this format, the total line width (displayed plus non-displayed pixels) should be a multiple of four 1246 pixels (nine bytes).

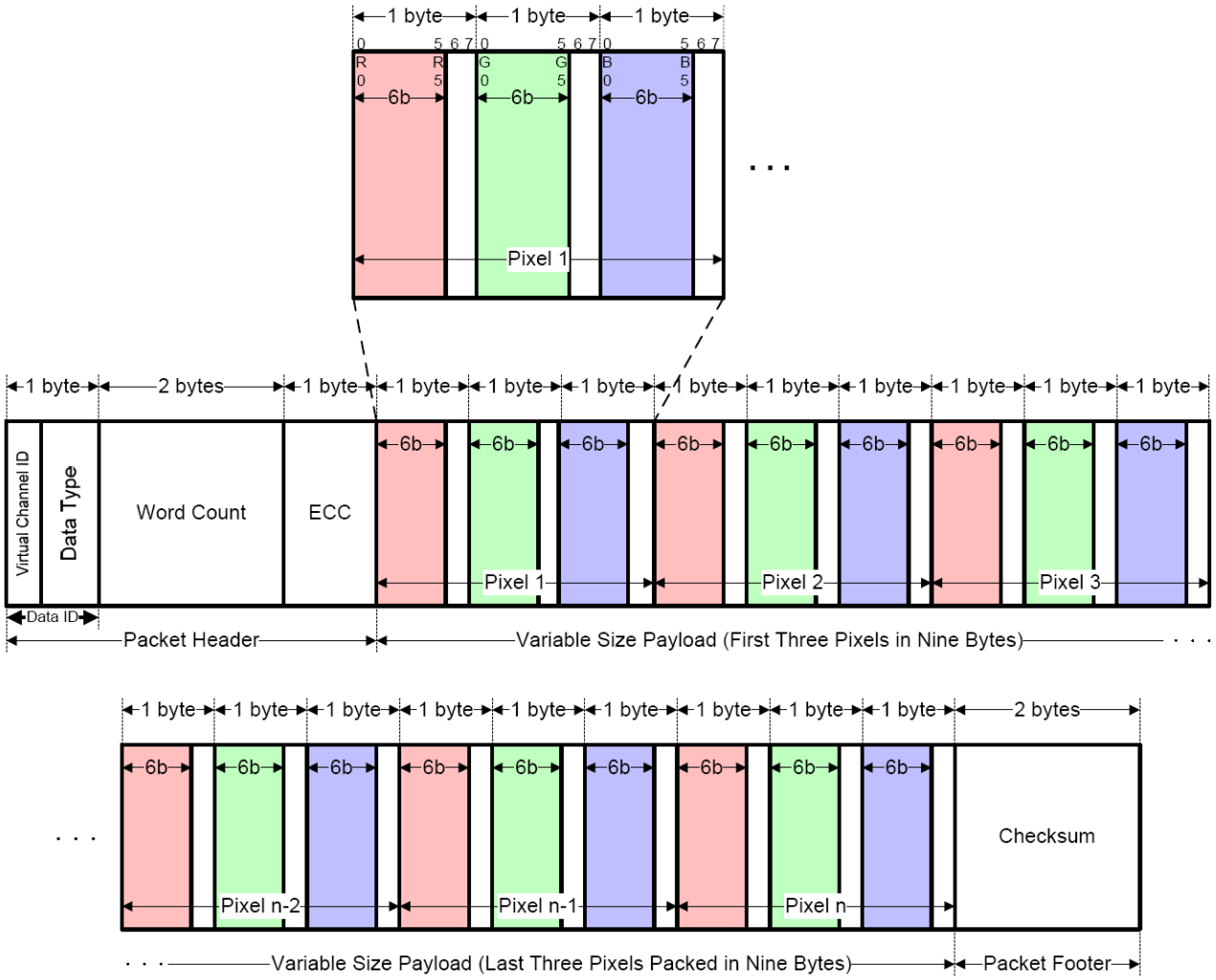


7.7.11. MIPI – 18-bit per Pixel, Long packet, Data Type = 10 1110 (2Eh)

In the 18-bit Pixel Loosely Packed format, each R, G, or B color component is six bits but is shifted to the upper bits of the byte, such that the valid pixel bits occupy bits [7:2] of each byte. Bits [1:0] of each payload byte representing active pixels are ignored. As a result, each pixel requires three bytes as it is transmitted across the Link. This requires more bandwidth than the “packed” format, but requires less shifting and multiplexing logic in the packing and unpacking functions on each end of the Link.

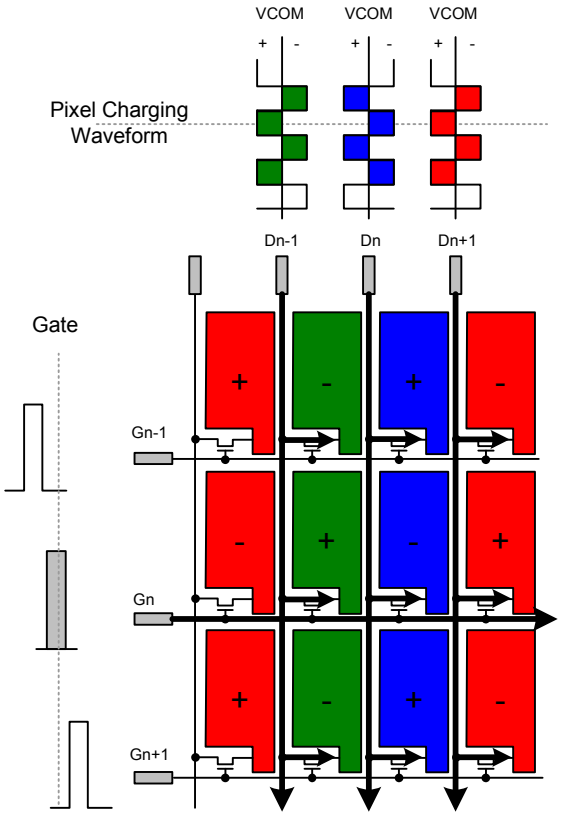
This format is used to transmit RGB image data formatted as pixels to a Video Mode display module that displays 18-bit pixels. The packet consists of the DI byte, a two-byte WC, an ECC byte, a payload of length WC bytes and a two-byte Checksum. The pixel format is red (6 bits), green (6 bits) and blue (6 bits) in that order. Within a color component, the LSB is sent first, the MSB last.

With this format, pixel boundaries align with byte boundaries every three bytes. The total line width (displayed plus non-displayed pixels) should be a multiple of three bytes.

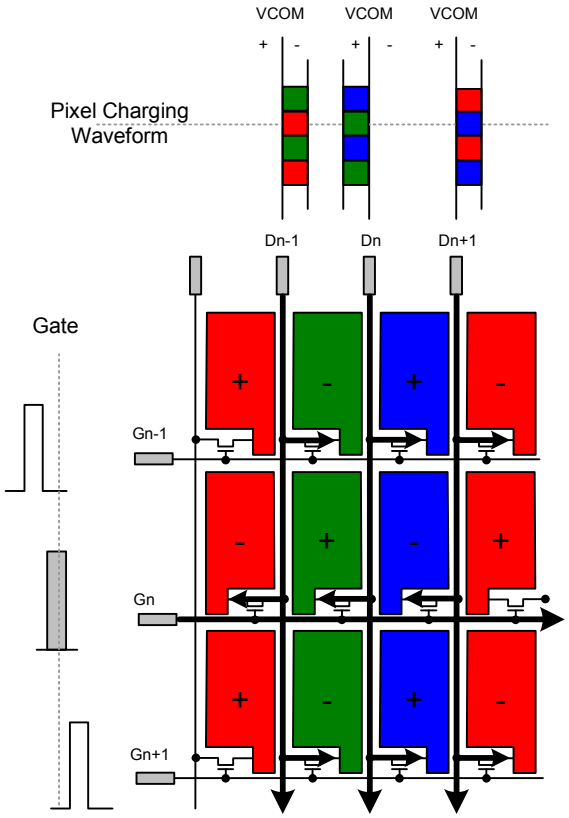


7.8. Z-inversion

The ILI9486 supports Z-inversion for reduce power consumption. The Zigzag can decrease the switching frequency, relative to the magnitude of the display power consumption, and the switching level. This method will have a addendum data line after the last data line.



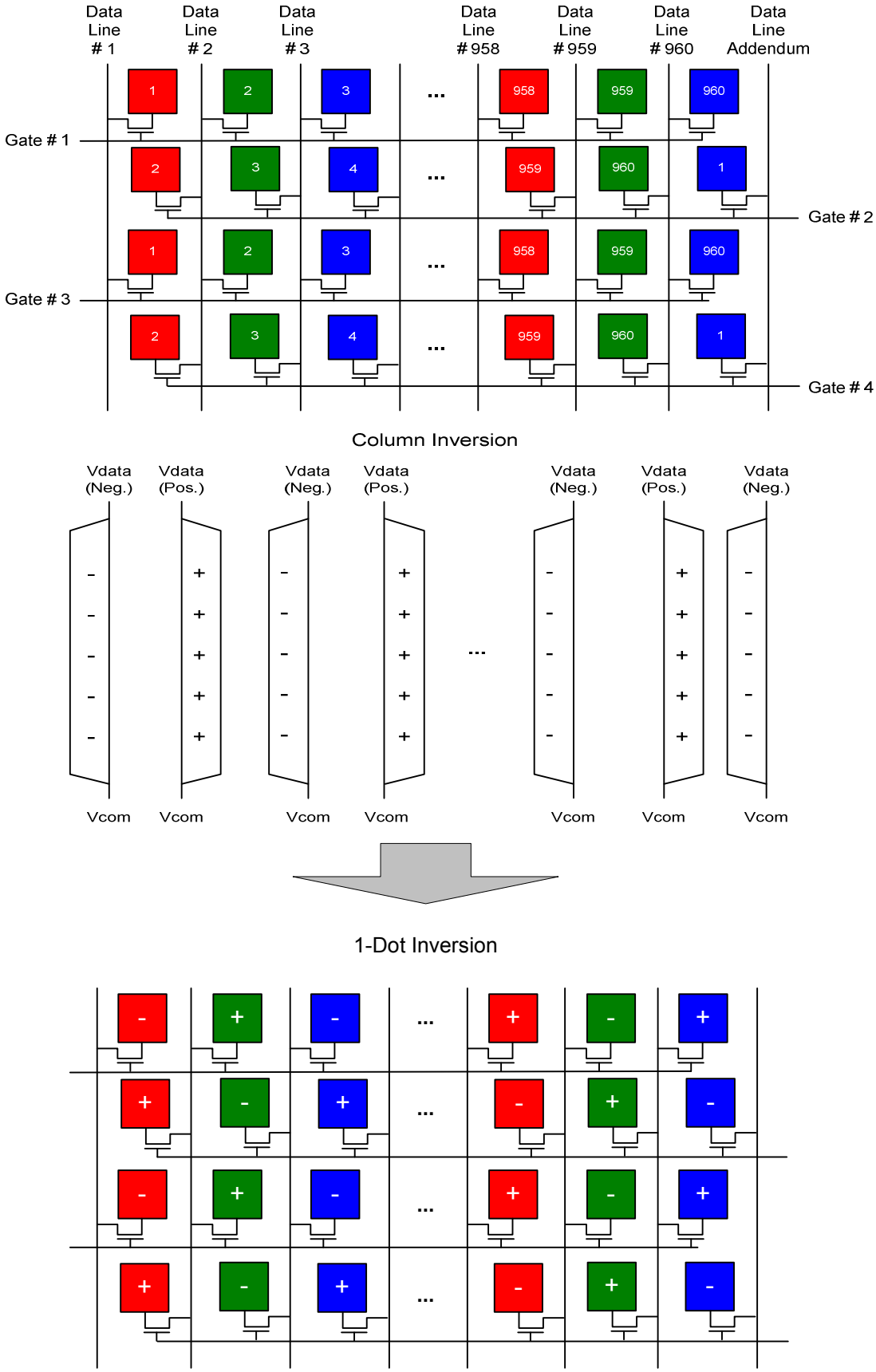
1-Dot Inversion Driving



Vertical Bi-Color driving

7.8.1 Z-inversion concept

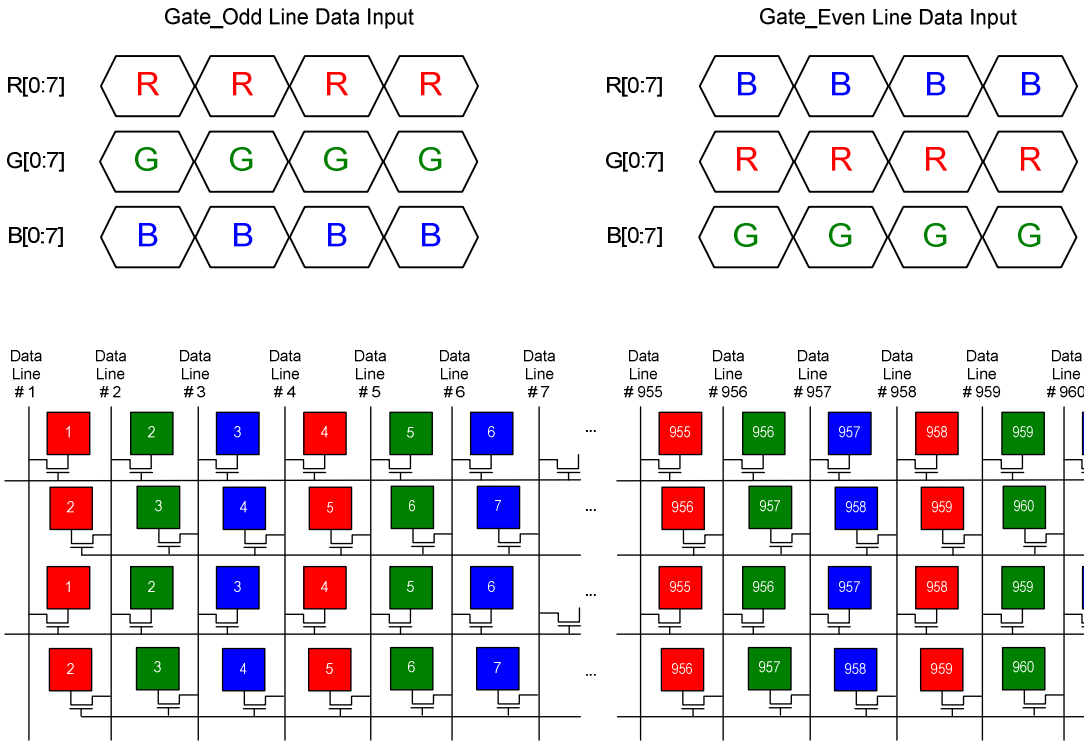
The Zigzag method uses the same polarity of data line of the column inversion to show out the 1-dot inversion.



7.8.2 Z-inversion Odd/Even Gate data input method

Gate_Odd line : using the normally data input mode and put on the R, G, B date to sub-pixel R, G, B respectively.

Gate_Even line : put on the G, B, R data to sub-pixel R, G, B respectively.



7.8.3 Z-inversion data input method

The driving panel display method is that added the one sub pixel at the Gate_Even shift the data output.

Red

	Data # 1	Data # 2	Data # 3	Data # 4	Data # 5	Data # 6	...	Data # 955	Data # 956	Data # 957	Data # 958	Data # 959	Data # 960	Data Option
Gate_Odd	R	G	B	R	G	B		R	G	B	R	G	B	
Gate_Even	R	G	B	R	G	B		R	G	B	R	G	B	
Gate_Odd	R	G	B	R	G	B		R	G	B	R	G	B	
Gate_Even	R	G	B	R	G	B		R	G	B	R	G	B	

Green

	Data # 1	Data # 2	Data # 3	Data # 4	Data # 5	Data # 6	...	Data # 955	Data # 956	Data # 957	Data # 958	Data # 959	Data # 960	Data Option
Gate_Odd	R	G	B	R	G	B		R	G	B	R	G	B	
Gate_Even	R	G	B	R	G	B		R	G	B	R	G	B	
Gate_Odd	R	G	B	R	G	B		R	G	B	R	G	B	
Gate_Even	R	G	B	R	G	B		R	G	B	R	G	B	

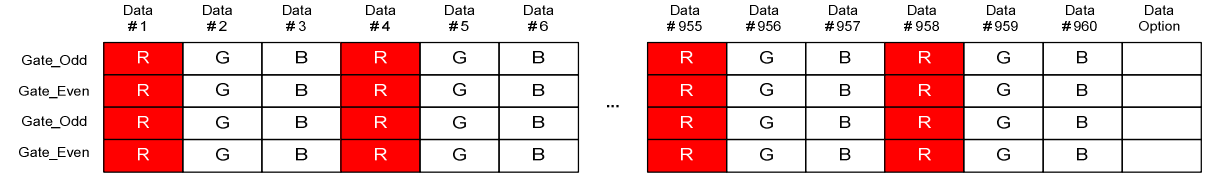
Blue

	Data # 1	Data # 2	Data # 3	Data # 4	Data # 5	Data # 6	...	Data # 955	Data # 956	Data # 957	Data # 958	Data # 959	Data # 960	Data Option
Gate_Odd	R	G	B	R	G	B		R	G	B	R	G	B	
Gate_Even	R	G	B	R	G	B		R	G	B	R	G	B	
Gate_Odd	R	G	B	R	G	B		R	G	B	R	G	B	
Gate_Even	R	G	B	R	G	B		R	G	B	R	G	B	

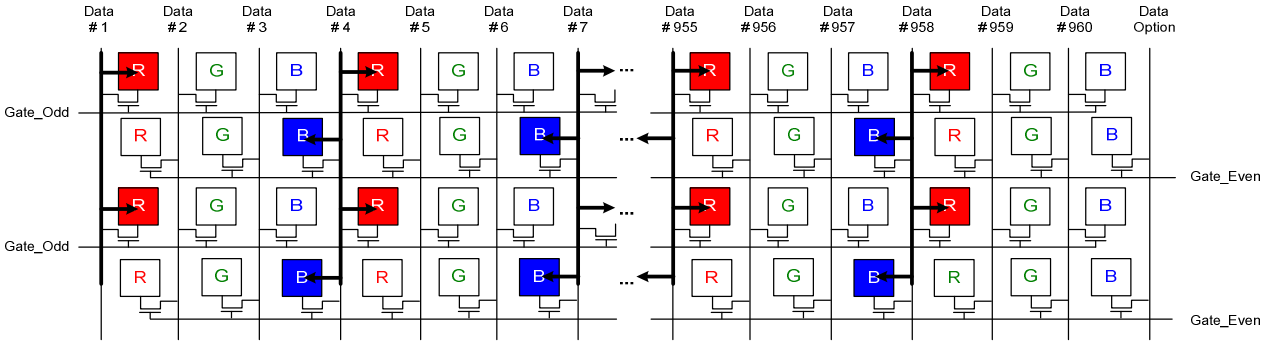
7.8.3.1 Z-inversion RED Data display

The below figure is normally panel driving method for Red data input. For driving Red pattern, the Red and Blue sub pixel will light up line by line when the data signal input.

Input Data Signal

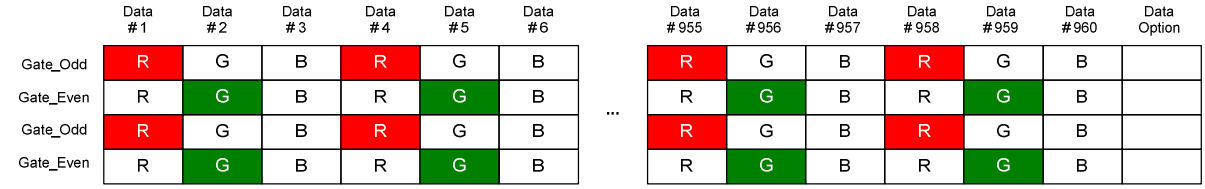


Panel Driving

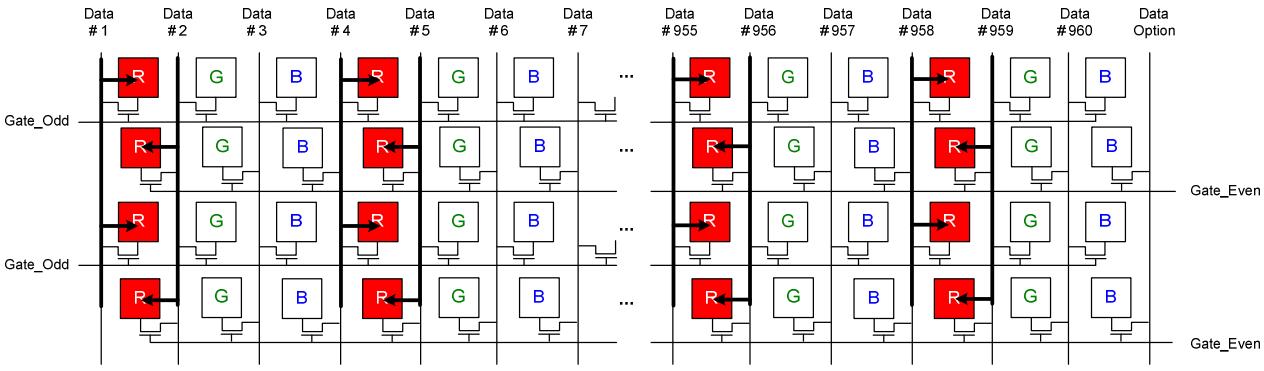


The below figure is Z-inversion panel driving method. The panel will be drive by the Red data input of the Gate_Odd and the Green data input of the Gate_Even.

Input Data Signal



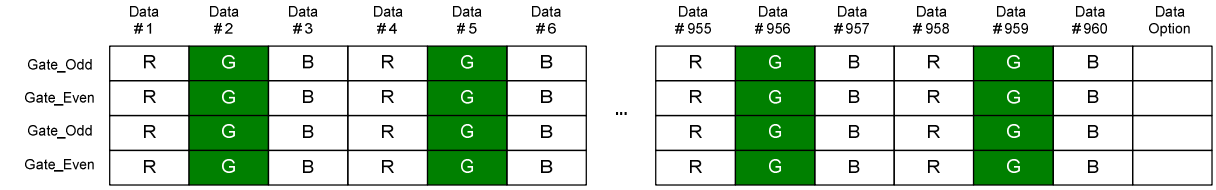
Panel Driving



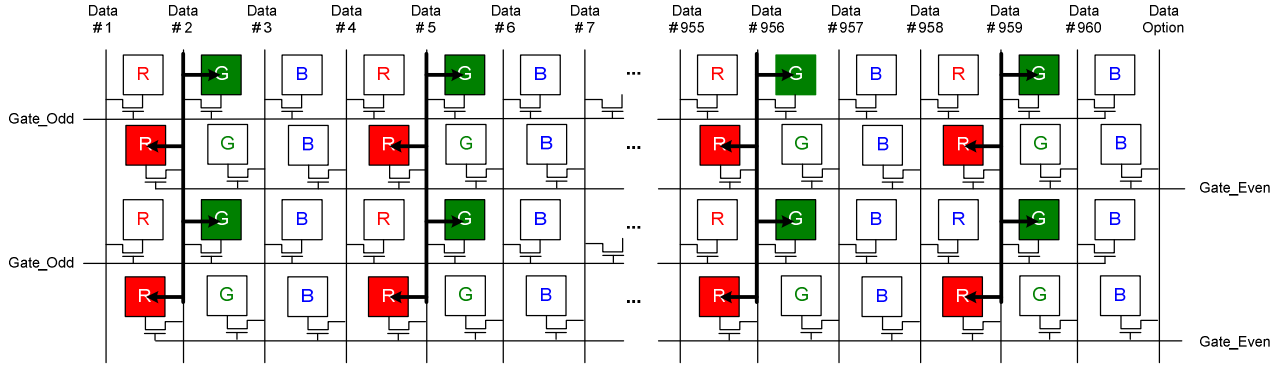
7.8.3.2 Z-inversion GREEN Data display

The below figure is normally panel driving method for Green data input. For driving Green pattern, the Green and Red sub pixel will light up line by line when the data signal input.

Input Data Signal

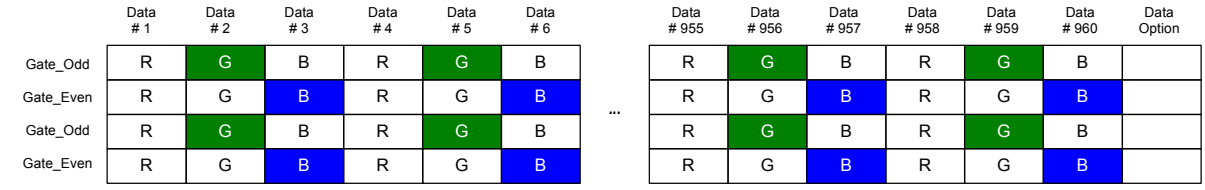


Panel Driving

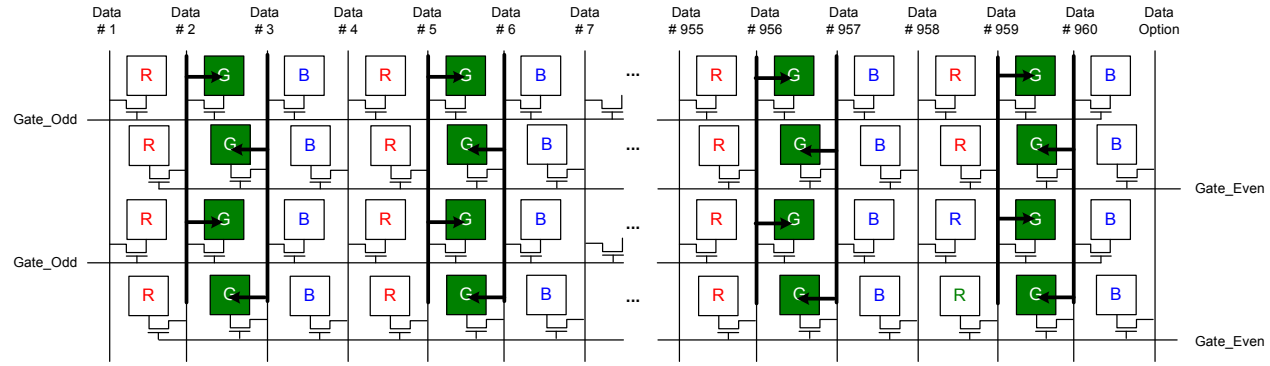


The below figure is Z-inversion panel driving method. The panel will be drive by the Green data input of the Gate_Odd and the Blue data input of the Gate_Even.

Input Data Signal



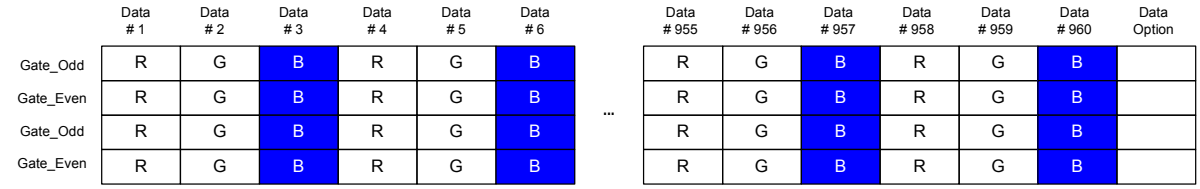
Panel Driving



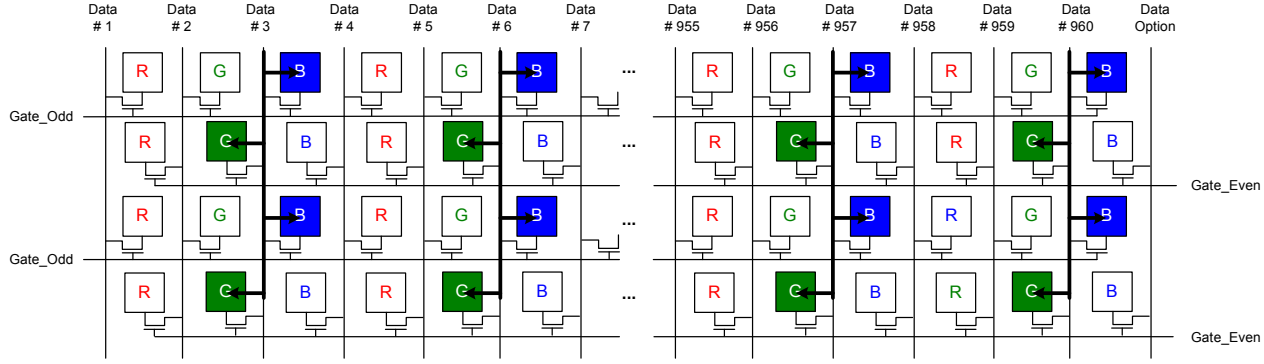
7.8.3.3 Z-inversion BLUE Data display

The below figure is normally panel driving method for Blue data input. For driving Blue pattern, the Blue and Green sub pixel will light up line by line when the data signal input.

Input Data Signal

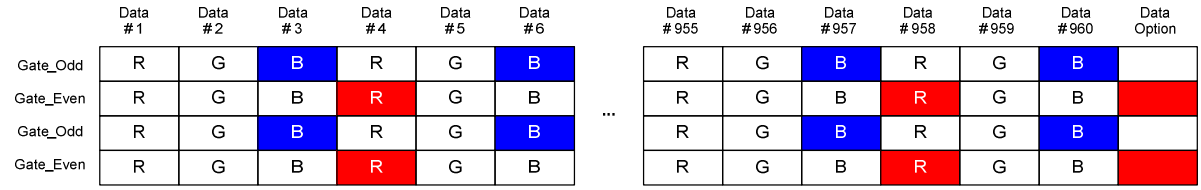


Panel Driving

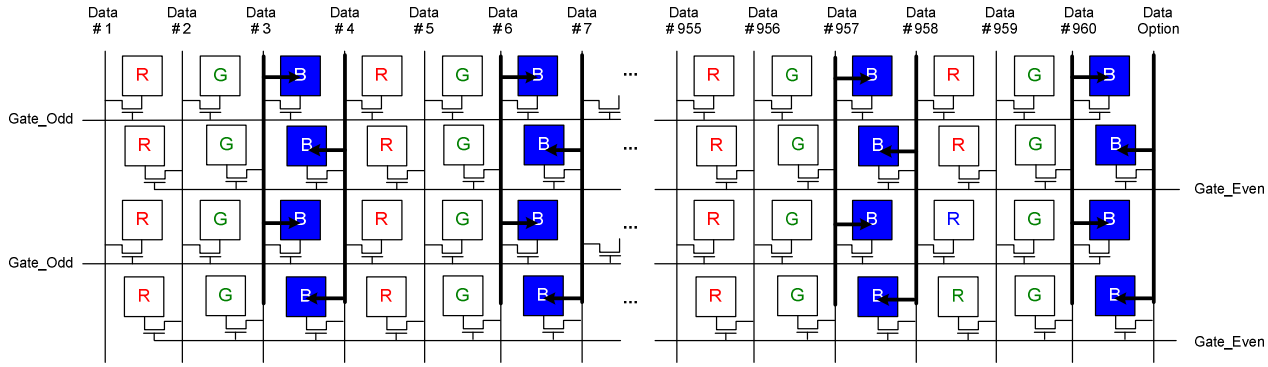


The below figure is Z-inversion panel driving method. The panel will be drive by the Blue data input of the Gate_Odd and the Red data input of the Gate_Even.

Input Data Signal



Panel Driving



8. Command

8.1. Command List

Regular Command Set													
Command Function	D/CX	RDX	WRX	D[15:8]	D7	D6	D5	D4	D3	D2	D1	D0	Hex
NOP	0	1	↑	XXXXXXXX	0	0	0	0	0	0	0	0	00h
Soft Reset	0	1	↑	XXXXXXXX	0	0	0	0	0	0	0	1	01h
Read display identification information	0	1	↑	XXXXXXXX	0	0	0	0	0	1	0	0	04h
	1	↑	1	XXXXXXXX	X	X	X	X	X	X	X	X	XX
	1	↑	1	XXXXXXXX	ID1 [7:0]								XX
	1	↑	1	XXXXXXXX	ID2 [7:0]								XX
	1	↑	1	XXXXXXXX	ID3 [7:0]								XX
Read Number of the Errors on DSI	0	↑	1	XXXXXXXX	0	0	0	0	0	1	0	1	05h
	1	↑	1	XXXXXXXX	X	X	X	X	X	X	X	X	XX
	1	↑	1	XXXXXXXX	P[7:0]								XX
Read Display Status	0	↑	1	XXXXXXXX	0	0	0	0	1	0	0	1	09h
	1	↑	1	XXXXXXXX	X	X	X	X	X	X	X	X	XX
	1	↑	1	XXXXXXXX	D[31:24]								XX
	1	↑	1	XXXXXXXX	D[23:16]								XX
	1	↑	1	XXXXXXXX	D[15:8]								XX
	1	↑	1	XXXXXXXX	D[7:0]								XX
Read Display Power Mode	0	↑	1	XXXXXXXX	0	0	0	0	1	0	1	0	0Ah
	1	↑	1	XXXXXXXX	X	X	X	X	X	X	X	X	XX
	1	↑	1	XXXXXXXX	D[7:2]						0	0	XX
Read Display MADCTL	0	↑	1	XXXXXXXX	0	0	0	0	1	0	1	1	0Bh
	1	↑	1	XXXXXXXX	X	X	X	X	X	X	X	X	XX
	1	↑	1	XXXXXXXX	D[7:2]						0	0	XX
Read Pixel Format	0	↑	1	XXXXXXXX	0	0	0	0	1	1	0	0	0Ch
	1	↑	1	XXXXXXXX	X	X	X	X	X	X	X	X	XX
	1	↑	1	XXXXXXXX	DPI[3:0]				0	DBI[2:0]			XX
Read Display Image Mode	0	↑	1	XXXXXXXX	0	0	0	0	1	1	0	1	0Dh
	1	↑	1	XXXXXXXX	X	X	X	X	X	X	X	X	XX
	1	↑	1	XXXXXXXX	D[7:0]								XX
Read Display signal Mode	0	↑	1	XXXXXXXX	0	0	0	0	1	1	1	0	0Eh
	1	↑	1	XXXXXXXX	X	X	X	X	X	X	X	X	XX
	1	↑	1	XXXXXXXX	D7	D6	D5	D4	D3	D2	D1	D0	XX
Read Display Self-Diagnostic Result	0	↑	1	XXXXXXXX	0	0	0	0	1	1	1	1	0Fh
	1	↑	1	XXXXXXXX	X	X	X	X	X	X	X	X	XX
	1	↑	1	XXXXXXXX	D7	D6	0	0	0	0	0	D0	XX
Sleep IN	0	1	↑	XXXXXXXX	0	0	0	1	0	0	0	0	10h
Sleep OUT	0	1	↑	XXXXXXXX	0	0	0	1	0	0	0	1	11h
Partial Mode ON	0	1	↑	XXXXXXXX	0	0	0	1	0	0	1	0	12h
Normal Display Mode ON	0	1	↑	XXXXXXXX	0	0	0	1	0	0	1	1	13h
Display Inversion OFF	0	1	↑	XXXXXXXX	0	0	1	0	0	0	0	0	20h
Display Inversion ON	0	1	↑	XXXXXXXX	0	0	1	0	0	0	0	1	21h
Display OFF	0	1	↑	XXXXXXXX	0	0	1	0	1	0	0	0	28h
Display ON	0	1	↑	XXXXXXXX	0	0	1	0	1	0	0	1	29h
Column Address Set	0	1	↑	XXXXXXXX	0	0	1	0	1	0	1	0	2Ah
	1	1	↑	XXXXXXXX	SC[15:8]								XX
	1	1	↑	XXXXXXXX	SC[7:0]								XX
	1	1	↑	XXXXXXXX	EC[15:8]								XX
	1	1	↑	XXXXXXXX	EC[7:0]								XX
Page Address Set	0	1	↑	XXXXXXXX	0	0	1	0	1	0	1	1	2Bh
	1	1	↑	XXXXXXXX	SP[15:8]								XX
	1	1	↑	XXXXXXXX	SP[7:0]								XX
	1	1	↑	XXXXXXXX	EP[15:8]								XX
	1	1	↑	XXXXXXXX	EP[7:0]								XX
Memory Write	0	1	↑	XXXXXXXX	0	0	1	0	1	1	0	0	2Ch
	1	1	↑	D1[15:0]									XX
	1	1	↑	Dx[15:0]									XX
	1	1	↑	Dn[15:0]									XX
Memory Read	0	↑	1	XXXXXXXX	0	0	1	0	1	1	1	0	2Eh
	1	↑	1	XXXXXXXX	X	X	X	X	X	X	X	X	XX

	1	↑	1	D1[15:0]									XX
	1	↑	1	Dx[15:0]									XX
	1	↑	1	Dn[15:0]									XX
	1	↑	1	XXXXXXXX	Pn[7:0]								XX
Partial Area	0	1	↑	XXXXXXXX	0	0	1	1	0	0	0	0	30h
	1	1	↑	XXXXXXXX	SR[15:8]								XX
	1	1	↑	XXXXXXXX	SR[7:0]								XX
	1	1	↑	XXXXXXXX	ER[15:8]								XX
	1	1	↑	XXXXXXXX	ER[7:0]								XX
Vertical Scrolling Definition	0	1	↑	XXXXXXXX	0	0	1	1	0	0	1	1	33h
	1	1	↑	XXXXXXXX	TFA[15:8]								XX
	1	1	↑	XXXXXXXX	TFA[7:0]								XX
	1	1	↑	XXXXXXXX	VSA[15:8]								XX
	1	1	↑	XXXXXXXX	VSA[7:0]								XX
	1	1	↑	XXXXXXXX	BFA[15:8]								XX
	1	1	↑	XXXXXXXX	BFA[7:0]								XX
Tearing Effect Line OFF	0	1	↑	XXXXXXXX	0	0	1	1	0	1	0	0	34h
Tearing Effect Line ON	0	1	↑	XXXXXXXX	0	0	1	1	0	1	0	1	35h
Memory Access Control	0	1	↑	XXXXXXXX	0	0	1	1	0	1	1	0	36h
	1	1	↑	XXXXXXXX	MY	MX	MV	ML	BGR	MH	X	X	XX
Vertical Scrolling Start Address	0	1	↑	XXXXXXXX	0	0	1	1	0	1	1	1	37h
	1	1	↑	XXXXXXXX	VSP[15:8]								XX
	1	1	↑	XXXXXXXX	VSP[7:0]								XX
Idle Mode OFF	0	1	↑	XXXXXXXX	0	0	1	1	1	0	0	0	38h
Idle Mode ON	0	1	↑	XXXXXXXX	0	0	1	1	1	0	0	1	39h
Interface Pixel Format	0	1	↑	XXXXXXXX	0	0	1	1	1	0	1	0	3Ah
	1	1	↑	XXXXXXXX	0	DPI[6:4]			0	DBI[2:0]			XX
Memory Write Continue	0	1	↑	XXXXXXXX	0	0	1	1	1	1	0	0	3Ch
	1	1	↑	D1[15:0]									XX
	1	1	↑	Dx[15:0]									XX
	1	1	↑	Dn[15:0]									XX
Memory Read Continue	0	↑	1	XXXXXXXX	0	0	1	1	1	1	1	0	3Eh
	1	↑	1	XXXXXXXX	X	X	X	X	X	X	X	X	XX
	1	↑	1	D1[15:0]									XX
	1	↑	1	Dx[15:0]									XX
	1	↑	1	Dn[15:0]									XX
Write Tear Scan line	0	1	↑	XXXXXXXX	0	1	0	0	0	1	0	0	44h
	1	1	↑	XXXXXXXX	N[15:8]								XX
	1	1	↑	XXXXXXXX	N[7:0]								XX
Read Tear Scan Line	0	↑	1	XXXXXXXX	0	1	0	0	0	1	0	1	45h
	1	↑	1	XXXXXXXX	X	X	X	X	X	X	X	X	XX
	1	↑	1	XXXXXXXX	N[15:8]								XX
	1	↑	1	XXXXXXXX	N[7:0]								XX
Write Display Brightness value	0	1	↑	XXXXXXXX	0	1	0	1	0	0	0	1	51h
	1	1	↑	XXXXXXXX	DBV[7:0]								XX
Read Display Brightness Value	0	1	↑	XXXXXXXX	0	1	0	1	1	0	1	0	52h
	1	↑	1	XXXXXXXX	X	X	X	X	X	X	X	X	XX
	1	↑	1	XXXXXXXX	DBV[7:0]								XX
Write CTRL Display value	0	1	↑	XXXXXXXX	0	1	0	1	0	0	1	1	53h
	1	1	↑	XXXXXXXX	0	0	BCTRL	0	DD	BL	0	0	XX
Read CTRL Display value	0	1	↑	XXXXXXXX	0	1	0	1	0	1	0	0	54h
	1	↑	1	XXXXXXXX	X	X	X	X	X	X	X	X	XX
	1	↑	1	XXXXXXXX	0	0	BCTRL	0	DD	BL	0	0	XX
Write Content Adaptive Brightness Control value	0	1	↑	XXXXXXXX	0	1	0	1	0	1	0	1	55h
	1	1	↑	XXXXXXXX	0	0	0	0	0	0	C[1:0]		XX
Read Content Adaptive Brightness Control value	0	1	↑	XXXXXXXX	0	1	0	1	0	1	1	0	56h
	1	↑	1	XXXXXXXX	X	X	X	X	X	X	X	X	XX
	1	↑	1	XXXXXXXX	0	0	0	0	0	0	C[1:0]		XX
Write CABC Minimum Brightness	0	1	↑	XXXXXXXX	0	1	0	1	1	1	1	0	5Eh
	1	1	↑	XXXXXXXX	CMB[7:0]								XX
Read CABC Minimum Brightness	0	1	↑	XXXXXXXX	0	1	0	1	1	1	1	1	5Fh
	1	↑	1	XXXXXXXX	X	X	X	X	X	X	X	X	XX
	1	↑	1	XXXXXXXX	CMB[7:0]								XX
Read First Checksum	0	1	↑	XXXXXXXX	1	0	1	0	1	0	1	0	AAh
	1	↑	1	XXXXXXXX	X	X	X	X	X	X	X	X	XX

	1	↑	1	XXXXXXXX	FCS[7:0]								XX
Read Continue Checksum	0	1	↑	XXXXXXXX	1	0	1	0	1	1	1	1	AFh
	1	↑	1	XXXXXXXX	X	X	X	X	X	X	X	X	XX
	1	↑	1	XXXXXXXX	CCS[7:0]								XX
Read ID1	0	1	↑	XXXXXXXX	1	1	0	1	1	0	1	0	DAh
	1	↑	1	XXXXXXXX	X	X	X	X	X	X	X	X	XX
	1	↑	1	XXXXXXXX	ID1[7:0]								XX
Read ID2	0	1	↑	XXXXXXXX	1	0	1	0	1	0	1	1	DBh
	1	↑	1	XXXXXXXX	X	X	X	X	X	X	X	X	XX
	1	↑	1	XXXXXXXX	ID2[7:0]								XX
Read ID3	0	1	↑	XXXXXXXX	1	0	1	0	1	1	0	0	DCh
	1	↑	1	XXXXXXXX	X	X	X	X	X	X	X	X	XX
	1	↑	1	XXXXXXXX	ID3[7:0]								XX

Extended Command Set													
Command Function	D/CX	RDX	WRX	D[15:8]	D7	D6	D5	D4	D3	D2	D1	D0	Hex
Interface Mode Control	0	1	↑	XXXXXXXX	1	0	1	1	0	0	0	0	B0h
	1	1	↑	XXXXXXXX	SDA_EN	0	0	0	VSPL	HSPL	DPL	EPL	XX
Frame Rate Control（In Normal Mode/Full Colors）	0	1	↑	XXXXXXXX	1	0	1	1	0	0	0	1	B1h
	1	1	↑	XXXXXXXX	FRS[3:0]				0	0	DIVA[1:0]		XX
	1	1	↑	XXXXXXXX	0	0	0	RTNA[4:0]					XX
Frame Rate Control（In Idle Mode/8 colors）	0	1	↑	XXXXXXXX	1	0	1	1	0	0	1	0	B2h
	1	1	↑	XXXXXXXX	0	0	0	0	0	0	DIVB[1:0]		XX
	1	1	↑	XXXXXXXX	0	0	0	RTNB[4:0]					XX
Frame Rate Control（In Partial Mode/Full colors）	0	1	↑	XXXXXXXX	1	0	1	1	0	0	1	1	B3h
	1	1	↑	XXXXXXXX	0	0	0	0	0	0	DIVC[1:0]		XX
	1	1	↑	XXXXXXXX	0	0	0	RTN[4:0]					XX
Display Inversion Control	0	1	↑	XXXXXXXX	1	0	1	1	0	1	0	0	B4h
	1	1	↑	XXXXXXXX	0	0	0	ZINV	0	0	DINV[1:0]		XX
Blanking Porch Control	0	1	↑	XXXXXXXX	1	0	1	1	0	1	0	1	B5h
	1	1	↑	XXXXXXXX	VFP[7:0]								XX
	1	1	↑	XXXXXXXX	VBP[7:0]								XX
	1	1	↑	XXXXXXXX	0	0	0	HFP[4:0]					XX
	1	1	↑	XXXXXXXX	HBP[7:0]								XX
Display Function Control	0	1	↑	XXXXXXXX	1	0	1	1	0	1	1	0	B6h
	1	1	↑	XXXXXXXX	BYPASS	0	RM	DM	PTG[1:0]		PT[1:0]		XX
	1	1	↑	XXXXXXXX	0	GS	SS	SM	ISC[3:0]				XX
	1	1	↑	XXXXXXXX	0	0	NL[5:0]						XX
Entry Mode Set	0	1	↑	XXXXXXXX	1	0	1	1	0	1	1	1	B7h
	1	1	↑	XXXXXXXX	EPF[1:0]		0	0	DSTB	GON	DTE	GAS	XX
Power Control 1	0	1	↑	XXXXXXXX	1	1	0	0	0	0	0	0	C0h
	1	1	↑	XXXXXXXX	0	0	0	VRH1[4:0]					XX
	1	1	↑	XXXXXXXX	0	0	0	VRH2[4:0]					XX
Power Control 2	0	1	↑	XXXXXXXX	1	1	0	0	0	0	0	1	C1h
	1	1	↑	XXXXXXXX	0	SAP[2:0]			BT[2:0]				XX
	1	1	↑	XXXXXXXX	0	0	0	0	0	VC[2:0]			XX
Power Control 3	0	1	↑	XXXXXXXX	1	1	0	0	0	0	1	0	C2h
	1	1	↑	XXXXXXXX	0	DCA1[2:0]			0	DCA0[2:0]			XX
Power Control 4	0	1	↑	XXXXXXXX	1	1	0	0	0	0	1	1	C3h
	1	1	↑	XXXXXXXX	0	DCB1[2:0]			0	DCB0[2:0]			XX
Power Control 5	0	1	↑	XXXXXXXX	1	1	0	0	0	1	0	0	C4h
	1	1	↑	XXXXXXXX	0	DCC2[2:0]			0	DCC0[2:0]			XX
VCOM Control 1	0	↑	↓	XXXXXXXX	1	1	0	0	0	1	0	1	C5h
	1	1	↑	XXXXXXXX	0	0	0	0	0	0	0	nVM	XX
	1	1	↑	XXXXXXXX	VCM_REG[7:0]								XX
	1	1	↑	XXXXXXXX	VCM_REG_EN	0	0	0	0	0	0	0	XX
	1	↑	↓	XXXXXXXX	VCM_OUT[7:0]								XX
CABC Control 1	0	1	↑	XXXXXXXX	1	1	0	0	0	1	1	0	C6h

	1	1	↑	XXXXXXXX	SCD_VLINE[7:0]									XX
	1	1	↑	XXXXXXXX	0	0	0	0	0	SCD_VLINE[10:8]				XX
CABC Control 2	0	1	↑	XXXXXXXX	1	1	0	0	1	0	0	0		C8h
	1	1	↑	XXXXXXXX	0	0	0	0	0	LEDONR	LEDONPOL	PWMPOL		XX
	1	1	↑	XXXXXXXX	PWM_DIV[7:0]									XX
CABC Control 3	0	1	↑	XXXXXXXX	1	1	0	0	1	0	0	1		C9h
	1	1	↑	XXXXXXXX	THRES_MOV[3:0]				THRES_STILL[3:0]					XX
CABC Control 4	0	1	↑	XXXXXXXX	1	1	0	0	1	0	1	0		CAh
	1	1	↑	XXXXXXXX	0	0	0	0	THRES_UI[3:0]					XX
CABC Control 5	0	1	↑	XXXXXXXX	1	1	0	0	1	0	1	1		CBh
	1	1	↑	XXXXXXXX	DTH_MOV[3:0]				DTH_STILL[3:0]					XX
CABC Control 6	0	1	↑	XXXXXXXX	1	1	0	0	1	1	0	0		CCh
	1	1	↑	XXXXXXXX	0	0	0	0	DTH_UI[3:0]					XX
CABC Control 7	0	1	↑	XXXXXXXX	1	1	0	0	1	1	0	1		CDh
	1	1	↑	XXXXXXXX	0	DIM_MOV[2:0]			0	DIM_STILL[2:0]				XX
CABC Control 8	0	1	↑	XXXXXXXX	1	1	0	0	1	1	1	0		CEh
	1	1	↑	XXXXXXXX	DIM_MIN[3:0]				0	DIM_UI[2:0]				XX
CABC Control 9	0	1	↑	XXXXXXXX										CFh
	1	1	↑	XXXXXXXX	PWM_DIV[7:0]									XX
NV Memory Write	0	1	↑	XXXXXXXX	1	1	0	1	0	0	0	0		D0h
	1	1	↑	XXXXXXXX	0	0	0	PGM_ADR[4:0]						XX
	1	1	↑	XXXXXXXX	PGM_DATA[7:0]									XX
NV Memory Protection Key	0	1	↑	XXXXXXXX	1	1	0	1	0	0	0	1		D1h
	1	1	↑	XXXXXXXX	KEY[23:16]									XX
	0	↑	1	XXXXXXXX	KEY[15:8]									XX
	1	↑	1	XXXXXXXX	KEY[7:0]									XX
NV Memory Status Read	1	↑	1	XXXXXXXX	1	1	0	1	0	0	1	0		D2h
	1	↑	1	XXXXXXXX	X	X	X	X	X	X	X	X		XX
	0	1	↑	XXXXXXXX	ID2_CNT[3:0]				ID1_CNT[3:0]					XX
	1	1	↑	XXXXXXXX	VMF_CNT[3:0]				ID3_CNT[3:0]					XX
	1	1	↑	XXXXXXXX	BUSY	0	0	0	0	0	0	MDDI_V12		XX
	1	1	↑	XXXXXXXX	OTP_DATA[7:0]									XX
Read ID4	0	↑	1	XXXXXXXX	1	1	0	1	0	0	1	1		D3h
	1	↑	1	XXXXXXXX	X	X	X	X	X	X	X	X		XX
	1	↑	1	XXXXXXXX	ID41[7:0]									XX
	1	↑	1	XXXXXXXX	ID42[7:0]									XX
	1	↑	1	XXXXXXXX	ID43[7:0]									XX
PGAMCTRL（Positive Gamma Control）	0	1	↑	XXXXXXXX	1	1	1	0	0	0	0	0		E0h
	1	1	↑	XXXXXXXX	0	0	0	0	VP0[3:0]					XX
	1	1	↑	XXXXXXXX	0	0	VP1[5:0]							XX
	1	1	↑	XXXXXXXX	0	0	VP2[5:0]							XX
	1	1	↑	XXXXXXXX	0	0	0	0	VP4[3:0]					XX
	1	1	↑	XXXXXXXX	0	0	0	VP6[4:0]						XX
	1	1	↑	XXXXXXXX	0	0	0	0	VP13[3:0]					XX
	1	1	↑	XXXXXXXX	0	VP20[6:0]								XX
	1	1	↑	XXXXXXXX	VP36[3:0]				VP27[3:0]					XX
	1	1	↑	XXXXXXXX	0	VP43[6:0]								XX
	1	1	↑	XXXXXXXX	0	0	0	0	VP50[3:0]					XX
	1	1	↑	XXXXXXXX	0	0	0	VP57[4:0]						XX
	1	1	↑	XXXXXXXX	0	0	0	0	VP59[3:0]					XX
	1	1	↑	XXXXXXXX	0	0	VP61[5:0]							XX
	1	1	↑	XXXXXXXX	0	0	VP62[5:0]							XX
	1	1	↑	XXXXXXXX	0	0	0	0	VP63[3:0]					XX
NGAMCTRL（Negative Gamma Control）	0	1	↑	XXXXXXXX	1	1	1	0	0	0	0	1		E1h
	1	1	↑	XXXXXXXX	0	0	0	0	VN0[3:0]					XX
	1	1	↑	XXXXXXXX	0	0	VN1[5:0]							XX
	1	1	↑	XXXXXXXX	0	0	VN2[5:0]							XX

	1	1	↑	XXXXXXXX	0		0	0	0	VN4[3:0]				XX
	1	1	↑	XXXXXXXX	0		0	0	VN6[4:0]					XX
	1	1	↑	XXXXXXXX	0		0	0		VN13[3:0]				XX
	1	1	↑	XXXXXXXX	0	VN20[6:0]								XX
	1	1	↑	XXXXXXXX	VN36[3:0]					VN27[3:0]				XX
	1	1	↑	XXXXXXXX	0	VN43[6:0]								XX
	1	1	↑	XXXXXXXX	0		0	0	0	VN50[3:0]				XX
	1	1	↑	XXXXXXXX	0		0	0	VN57[4:0]					XX
	1	1	↑	XXXXXXXX	0		0	0	0	VN59[3:0]				XX
	1	1	↑	XXXXXXXX	0		0	VN61[5:0]						XX
	1	1	↑	XXXXXXXX	0		0	VN62[5:0]						XX
	1	1	↑	XXXXXXXX	0		0	0	0	VN63[3:0]				XX
Digital Gamma Control 1	0	1	↑	XXXXXXXX	1		1	1	0	0	0	0	1	E2h
	1	1	↑	XXXXXXXX	RCA0[3:0]					BCA0[3:0]				XX
	1	1	↑	XXXXXXXX	RCAx[3:0]					BCAx[3:0]				XX
	1	1	↑	XXXXXXXX	RCA63[3:0]					BCA63[3:0]				XX
Digital Gamma Control 2	0	1	↑	XXXXXXXX	1		1	1	0	0	0	0	1	E3h
	1	1	↑	XXXXXXXX	RFA0[3:0]					BFA0[3:0]				XX
	1	1	↑	XXXXXXXX	RFAx[3:0]					BFAx[3:0]				XX
	1	1	↑	XXXXXXXX	RFA255[3:0]					BFA255[3:0]				XX
SPI Read Command Setting	0	1	↑	XXXXXXXX	1	1	1	1		1	0	1	1	FBh
	1	1	↑	XXXXXXXX	0	0	0	SPI_READ_EN		SPI_CNT[3:0]				XX

8.2. Command Description

8.2.1. NOP (00h)

00h	NOP (No Operation)												
	D/CX	RDX	WRX	D[15:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XXXXXXXX	0	0	0	0	0	0	0	0	00h
Parameter	No parameter												
Description	This command is an empty command; it does not have any effect on ILI9486. However it can be used to terminate Frame Memory Write or Read as described in RAMWR (Memory Write) and RAMRD (Memory Read) Commands. X = Don't care.												
Restriction	None												
Register Availability													

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	N/A
SW Reset	N/A
HW Reset	N/A

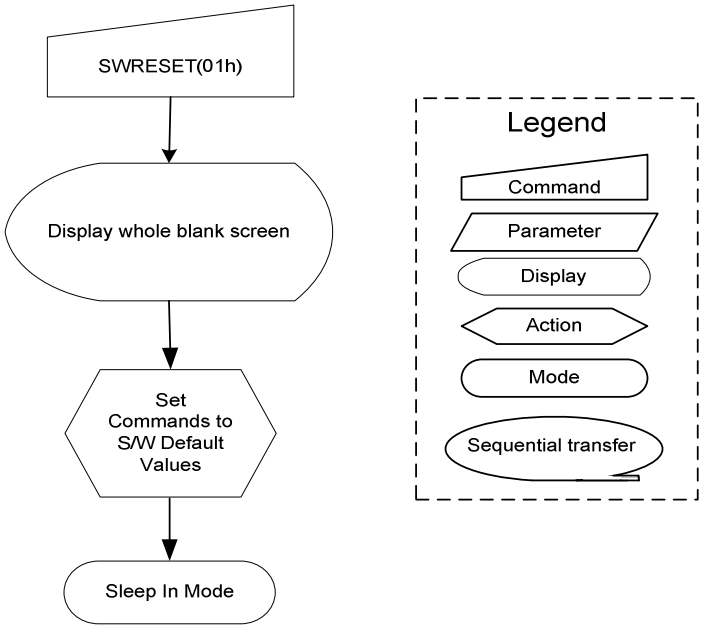
Flow Chart	None

8.2.2. Soft Reset (01h)

01h	SWRESET (Soft Reset)												
	D/CX	RDX	WRX	D[15:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XXXXXXXX	0	0	0	0	0	0	0	1	01h
Parameter	No parameter												
Description	When the Software Reset command is written, it causes software reset. It resets the commands and parameters to their S/W Reset default values. (See default tables in each command description.) The display is blank immediately Note: The Frame Memory contents is kept or not by this command. X = Don't care												
Restriction	It will be necessary to wait 5msec before sending new command following software reset. The display module loads all display supplier factory default values to the registers during this 5msec. If Software Reset is applied during Sleep Out mode, it will be necessary to wait 120msec before sending Sleep out command. Software Reset Command cannot be sent during Sleep Out sequence.												
Register Availability													
Default													
Flow Chart													

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Status	Default Value
Power On Sequence	N/A
SW Reset	N/A
HW Reset	N/A



8.2.3. Read display identification information (04h)

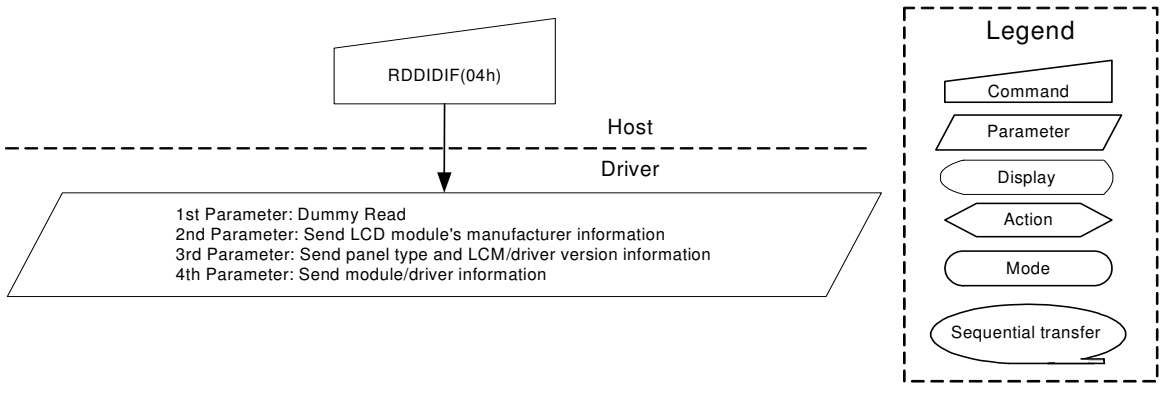
04h	RDDIDIF (Read Display Identification Information)												
	D/CX	RDX	WRX	D[17:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	0	0	0	1	0	0	04h
1st Parameter	1	↑	1	XX	X	X	X	X	X	X	X	X	X
2ndParameter	1	↑	1	XX	ID1 [7:0]								XX
3rd Parameter	1	↑	1	XX	ID2 [7:0]								XX
4th Parameter	1	↑	1	XX	ID3 [7:0]								XX
Description	This read byte returns 24 bits display identification information. The 1st parameter is dummy data. The 2nd parameter (ID1 [7:0]): LCD module's manufacturer ID. The 3rd parameter (ID2 [7:0]): LCD module/driver version ID. The 4th parameter (ID3 [7:0]): LCD module/driver ID.												
Restriction													
Register Availability													

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	See description
SW Reset	See description
HW Reset	See description

Flow Chart



8.2.4. Read Number of the Errors on DSI (05h)

05h	RDNUMED (Read Number of the Errors on DSI)												
	D/CX	RDX	WRX	D[15:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XXXXXXXX	0	0	0	0	0	1	0	1	05h
1st Parameter	1	↑	1	XXXXXXXX	X	X	X	X	X	X	X	X	XX
2nd Parameter	1	↑	1	XXXXXXXX	P[7:0]								XX
Description	The second parameter is telling a number of the errors on DSI. The more detailed description of the bits is below. P [6..0] bits are telling a number of the errors. P [7] is set to '1' if there is overflow with P[6..0] bits. P [7...0] bits are set to '0's (as well as RDDSM(0Eh)'s D0 is set '0' at the same time) after there is sent the second parameter information (= The read function is completed). This function is always returning P [7...0] = 00h if the parallel MCU interface is selected. X = can be '0' or '1'												
Restriction	ILI9486 is sending 2nd parameter value on the data lines if the MCU wants to read more than one parameter (= more than 2 RDX cycle) on parallel MCU interface. Only 2nd parameter is sent on DSI (The 1st parameter is not sent).												

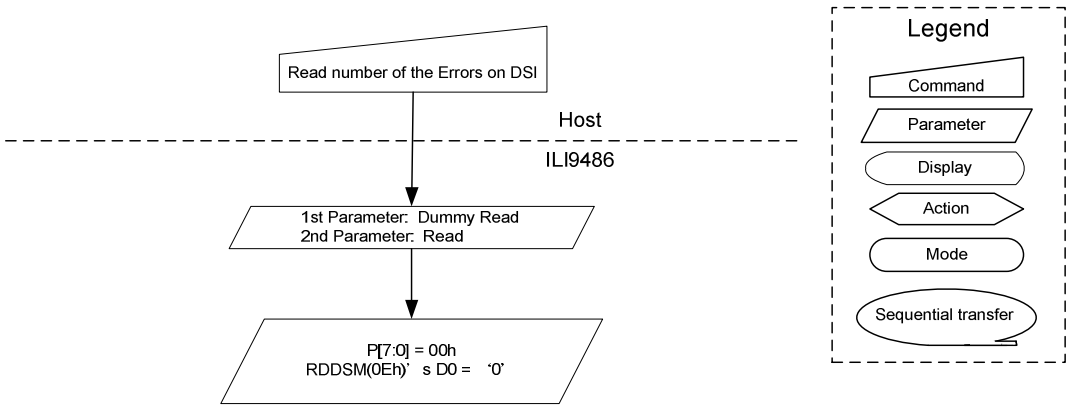
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	08_{HEX}
SW Reset	08_{HEX}
HW Reset	08_{HEX}

Flow Chart



8.2.5. Read Display Status (09h)

09h	RDDST (Read Display Status)												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	0	0	1	0	0	1	09h
1st Parameter	1	↑	1	XX	X	X	X	X	X	X	X	X	XX
2ndParameter	1	↑	1	XX	D [31:25]							0	XX
3rdParameter	1	↑	1	XX	0	D [22:20]			D [19:16]				XX
4thParameter	1	↑	1	XX	D15	0	D13	0	0	D [10:8]			XX
5thParameter	1	↑	1	XX	D [7:5]			0	0	0	0	0	XX

Description

This command indicates the current status of the display as described in the table below:

Bit	Description	Value	Status
D31	Booster voltage status	0	Booster OFF
		1	Booster ON
D30	Row address order	0	Top to Bottom (When MADCTL B7='0')
		1	Bottom to Top (When MADCTL B7='1')
D29	Column address order	0	Left to Right (When MADCTL B6='0').
		1	Right to Left (When MADCTL B6='1').
D28	Row/column exchange	0	Normal Mode (When MADCTL B5='0').
		1	Reverse Mode (When MADCTL B5='1').
D27	Vertical refresh	0	LCD Refresh Top to Bottom (When MADCTL B4='0')
		1	LCD Refresh Bottom to Top (When MADCTL B4='1').
D26	RGB/BGR order	0	RGB (When MADCTL B3='0')
		1	BGR (When MADCTL B3='1')
D25	Horizontal refresh order	0	LCD Refresh Left to Right (When MADCTL B2='0')
		1	LCD Refresh Right to Left (When MADCTL B2='1')
D24	Not used	0	---
D23	Not used	0	---
D22	Interface color pixel format definition	011	12-bit/pixel
D21		101	16-bit/pixel
D20		110	18-bit/pixel
D19	Idle mode ON/OFF	0	Idle Mode OFF
		1	Idle Mode ON
D18	Partial mode ON/OFF	0	Partial Mode OFF
		1	Partial Mode ON.
D17	Sleep IN/OUT	0	Sleep IN Mode
		1	Sleep OUT Mode.
D16	Display normal mode ON/OFF	0	Display Normal Mode OFF.
		1	Display Normal Mode ON.
D15	Vertical scrolling status	0	Vertical Scroll OFF
		1	Vertical Scroll ON
D14	Not used	0	---
D13	Inversion status	0	Inversion OFF
		1	Inversion ON
D12	All pixel ON	0	Not defined
D11	All pixel OFF	0	Not defined
D10	Display ON/OFF	0	Display is OFF
		1	Display is ON
D9	Tearing effect line ON/OFF	0	Tearing Effect Line OFF
		1	Tearing Effect ON
D[8:6]	Gamma curve selection	000	GC0
		001	GC1
		010	GC2
		011	GC3
		other	Not defined

	D5	Tearing effect line mode	0	Mode 1, V-Blanking only
			1	Mode 2, both H-Blanking and V-Blanking.
	D4	Not used	0	---
	D3	Not used	0	---
	D2	Not used	0	---
	D1	Not used	0	---
	D0	Not used	0	---

X = Don't care

Restriction

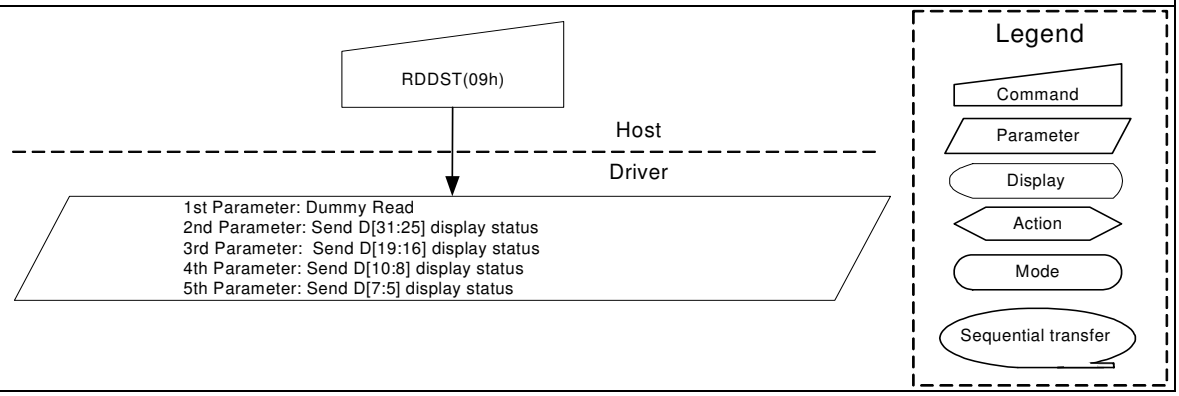
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	32'h00610000h
SW Reset	32'h00610000h
HW Reset	32'h00610000h

Flow Chart



8.2.6. Read Display Power Mode (0Ah)

0Ah	RDDPM (Read Display Power Mode)												
	D/CX	RDX	WRX	D[15:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XXXXXXXX	0	0	0	0	1	0	1	0	0Ah
1st Parameter	1	↑	1	XXXXXXXX	X	X	X	X	X	X	X	X	XX
2nd Parameter	1	↑	1	XXXXXXXX	D[7:2]						0	0	XX

Description

This command indicates the current status of the display as described in the table below:

Bit	Description	Comment
D7	Booster Voltage Status	
D6	Idle Mode On/Off	
D5	Partial Mode On/Off	
D4	Sleep In/Out	
D3	Display Normal Mode On/Off	
D2	Display On/Off	
D1	Not Defined	Set to '0'
D0	Not Defined	Set to '0'

Bit D7 – Booster Voltage Status

'0' = Booster Off or has a fault.

'1' = Booster On and working OK.

Bit D6 - Idle Mode On/Off

'0' = Idle Mode Off.

'1' = Idle Mode On.

Bit D5 – Partial Mode On/Off

'0' = Partial Mode Off.

'1' = Partial Mode On.

Bit D4 – Sleep In/Out

'0' = Sleep In Mode.

'1' = Sleep Out Mode.

Bit D3 – Display Normal Mode On/Off

'0' = Display Normal Mode Off.

'1' = Display Normal Mode On.

Bit D2 – Display On/Off

'0' = Display is Off.

'1' = Display is On.

Bit D1 – Not Defined

'This bit is not applicable for this project, so it is set to '0'

Bit D0 – Not Defined

'This bit is not applicable for this project, so it is set to '0'

X = Don't care

<table>
<tr><td>Restriction</td><td>ILI9486 is sending 2nd parameter value on the data lines if the MCU wants to read more than one parameter (= more than 2 RDX cycle) on parallel MCU interface.
Only 2nd parameter is sent on DSI (The 1st parameter is not sent).</td></tr>
<tr><td>Register Availability</td><td>
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
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</td></tr>
<tr><td>Default</td><td>
<table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td>08_{HEX}</td></tr>
<tr><td>SW Reset</td><td>08_{HEX}</td></tr>
<tr><td>HW Reset</td><td>08_{HEX}</td></tr>
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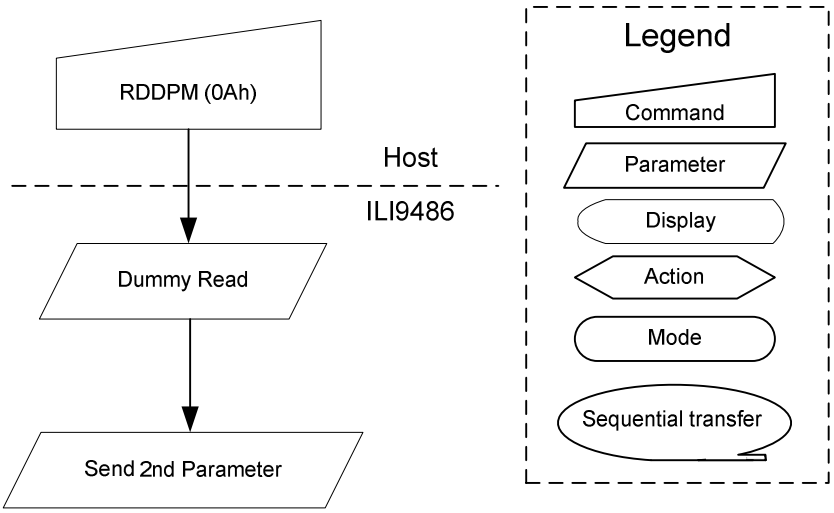
</td></tr>
<tr><td>Flow Chart</td><td> 
</td></tr>
</table>

8.2.7. Read Display MADCTL (0Bh)

0Bh	RDDMADCTL (Read Display MADCTL)												
	D/CX	RDX	WRX	D[15:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XXXXXXXX	0	0	0	0	1	0	1	1	0Bh
1st Parameter	1	↑	1	XXXXXXXX	X	X	X	X	X	X	X	X	XX
2nd Parameter	1	↑	1	XXXXXXXX	D[7:2]						0	0	XX

Description

This command indicates the current status of the display as described in the table below:

Bit	Description	Comment
D7	Page Address Order	
D6	Column Address Order	
D5	Page/Column Order	
D4	Line Address Order	
D3	RGB/BGR Order	
D2	Display Data Latch Data Order	
D1	Reserved	Set to '0'
D0	Reserved	Set to '0'

- Bit D7 – Page Address Order
  '0' = Top to Bottom
  '1' = Bottom to Top
- Bit D6 – Column Address Order
  '0' = Left to Right
  '1' = Right to Left
- Bit D5 - Page/Column Order
  '0' = Normal Mode
  '1' = Reverse Mode
  Note: For Bits D7 to D5, also refer to Section 9.3 MCU to memory write/read direction.
- Bit D4 – Line Address Order
  '0' = LCD Refresh Top to Bottom
  '1' = LCD Refresh Bottom to Top
- Bit D3 – RGB/BGR Order
  '0' = RGB
  '1' = BGR
- Bit D2 – Display Data Latch Data Order
  '0' = LCD Refresh Left to Right
  '1' = LCD Refresh Right to Left

Restriction

ILI9486 is sending 2nd parameter value on the data lines if the MCU wants to read more than one parameter (= more than 2 RDX cycle) on parallel MCU interface.

Only 2nd parameter is sent on DSI (The 1st parameter is not sent).

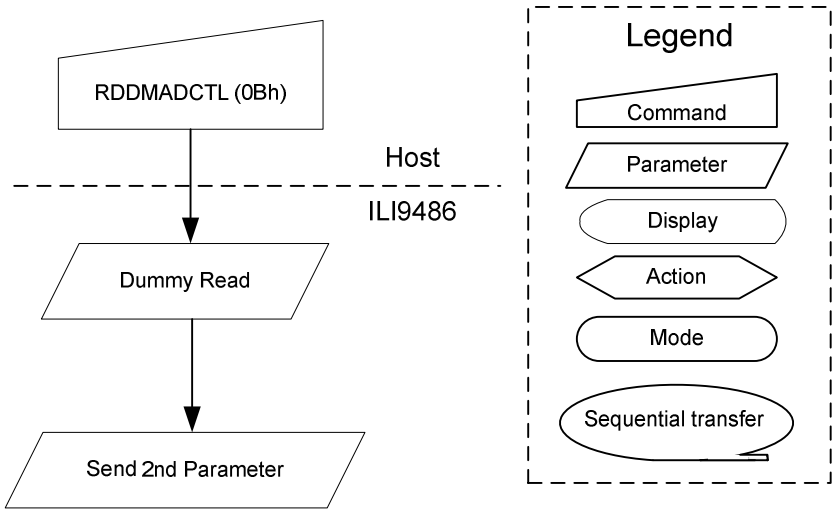
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00_{HEX}
SW Reset	**No Change**
HW Reset	00_{HEX}

Flow Chart



8.2.8. Read Display Pixel Format (0Ch)

0Ch	RDDCOLMOD (Read Display COLMOD)												
	D/CX	RDX	WRX	D[15:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XXXXXXXX	0	0	0	0	1	1	0	0	0Ch
1st Parameter	1	↑	1	XXXXXXXX	X	X	X	X	X	X	X	X	XX
2nd Parameter	1	↑	1	XXXXXXXX	DPI[3:0]				0	DBI[2:0]			XX

Description

This command indicates the current status of the display as described in the table below:

DPI[3:0]				RGB Interface Format
0	0	0	0	Reserved
0	0	0	1	Reserved
0	0	1	0	Reserved
0	0	1	1	Reserved
0	1	0	0	Reserved
0	1	0	1	16 bits / pixel
0	1	1	0	18 bits / pixel
0	1	1	1	Reserved

DBI[2:0]			CPU Interface Format
0	0	0	Reserved
0	0	1	Reserved
0	1	0	Reserved
0	1	1	Reserved
1	0	0	Reserved
1	0	1	16 bits / pixel
1	1	0	18 bits / pixel
1	1	1	Reserved

Restriction

ILI9486 is sending 2nd parameter value on the data lines if the MCU wants to read more than one parameter (= more than 2 RDX cycle) on parallel MCU interface.

Only 2nd parameter is sent on DSI (The 1st parameter is not sent).

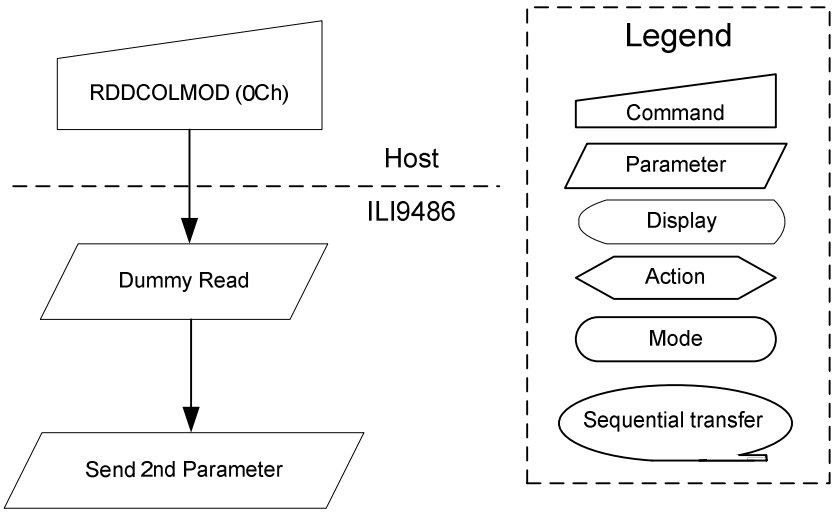
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	06_{HEX}
SW Reset	**No Change**
HW Reset	06_{HEX}

Flow Chart



8.2.9. Read Display Image Mode (0Dh)

0Dh	RDDIM (Read Display Image Mode)												
	D/CX	RDX	WRX	D[15:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XXXXXXXX	0	0	0	0	1	1	0	1	0Dh
1st Parameter	1	↑	1	XXXXXXXX	X	X	X	X	X	X	X	X	XX
2nd Parameter	1	↑	1	XXXXXXXX	D[7:0]								XX

Description

ILI9486 returns the Display Image Mode status.

Bit	Description
D7	Vertical Scrolling Status
D6	Reserved
D5	Inversion On/Off
D4	Reserved
D3	Reserved
D2	Gamma Curve Selection
D1	Gamma Curve Selection
D0	Gamma Curve Selection

This command indicates the current status of the display as described in the table below:

- Bit D7 – Vertical Scrolling On/Off

  '0' = Vertical Scrolling is Off.

  '1' = Vertical Scrolling is On.

- Bit D6 – Reserved
- Bit D5 – Inversion On/Off

  '0' = Inversion is Off.

  '1' = Inversion is On.

- Bit D4 – Reserved
- Bit D3 – Reserved
- Bits D2, D1, D0 – Gamma Curve Selection

  These bits are not applicable for this project, so they are set to '000', only support Gamma 2.2.

Restriction

ILI9486 is sending 2nd parameter value on the data lines if the MCU wants to read more than one parameter (= more than 2 RDX cycle) on parallel MCU interface.

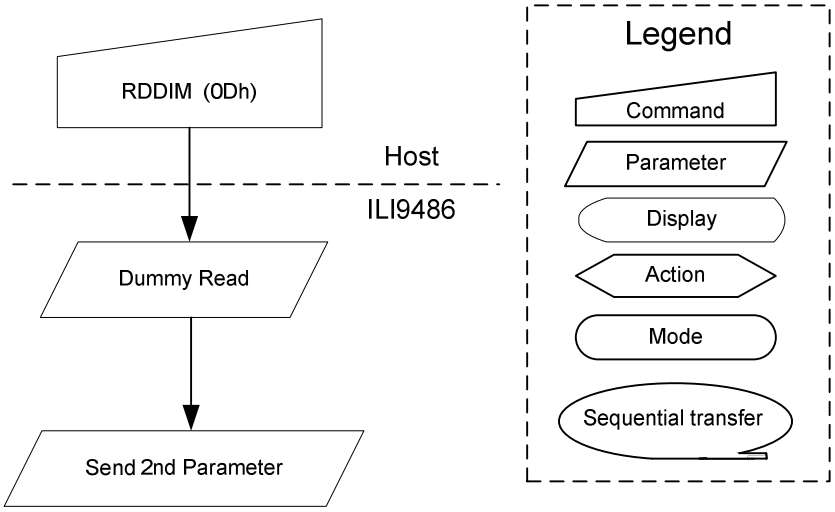
Only 2nd parameter is sent on DSI (The 1st parameter is not sent).

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00_{HEX}
SW Reset	00_{HEX}
HW Reset	00_{HEX}

Flow Chart	

8.2.10. Read Display Signal Mode (0Eh)

0Eh	RDDSM (Read Display Signal Mode)												
	D/CX	RDX	WRX	D[15:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XXXXXXXX	0	0	0	0	1	1	1	0	0Eh
1st Parameter	1	↑	1	XXXXXXXX	X	X	X	X	X	X	X	X	XX
2nd Parameter	1	↑	1	XXXXXXXX	D7	D6	D5	D4	D3	D2	D1	D0	XX

Description

This command indicates the current status of the display as described in the table below:

Bit	Value	Function
D7	0	Tearing Effect Line OFF
	1	Tearing Effect Line ON
D6	0	Tearing Effect Line Mode 1
	1	Tearing Effect Line Mode 2
D5	0	Horizontal Sync (RGB interface) OFF
	1	Horizontal Sync (RGB interface) ON
D4	0	Vertical Sync (RGB interface) OFF
	1	Vertical Sync (RGB interface) ON
D3	0	Pixel Clock (DOTCLK, RGB interface) OFF
	1	Pixel Clock (DOTCLK, RGB interface) ON
D2	0	Data Enable (DE, RGB interface) OFF
	1	Data Enable (DE, RGB interface) ON
D1	0	Reserved
	1	Reserved
D0	0	No Error on DSI
	1	Error on DSI

Restriction

ILI9486 is sending 2nd parameter value on the data lines if the MCU wants to read more than one parameter (= more than 2 RDX cycle) on parallel MCU interface.

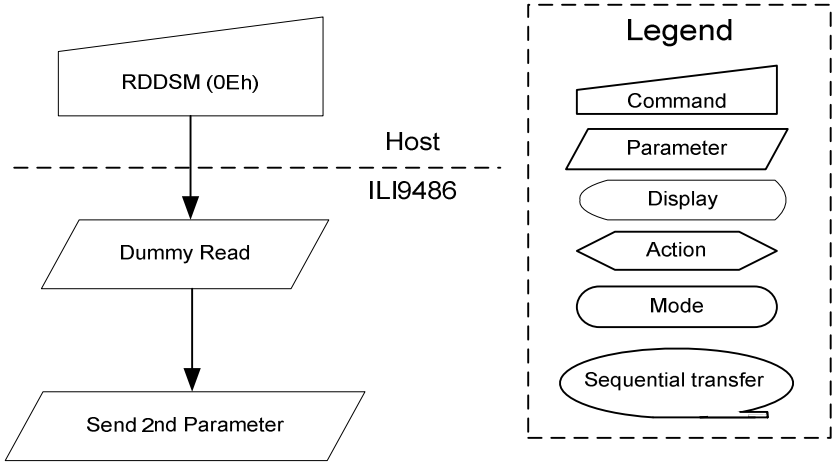
Only 2nd parameter is sent on DSI (The 1st parameter is not sent).

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00_{HEX}
SW Reset	00_{HEX}
HW Reset	00_{HEX}

Flow Chart	

8.2.11. Read Display Self-Diagnostic Result (0Fh)

0Fh	RDDSDR (Read Display Self-Diagnostic Result)												
	D/CX	RDX	WRX	D[15:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XXXXXXXX	0	0	0	0	1	1	1	1	0Fh
1st Parameter	1	↑	1	XXXXXXXX	X	X	X	X	X	X	X	X	XX
2nd Parameter	1	↑	1	XXXXXXXX	D7	D6	0	0	0	0	0	D0	XX

Description

This command indicates the status of the display self-diagnostic results after Sleep Out -command as described in the table below:

Bit	Description	Action
D7	Register Loading Detection	Invert the D7 bit if register values loading work properly.
D6	Functionality Detection	Invert the D6 bit if the display is functionality
D5	Not Used	'0'
D4	Not Used	'0'
D3	Not Used	'0'
D2	Not Used	'0'
D1	Not Used	'0'
D0	Checksums Comparison	'0' = Checksums are same '1' = Checksums are not same

Restriction

It will be necessary to wait 300ms after there is the last write access on User area registers before there can read Bit D0 value.

ILI9486 is sending 2nd parameter value on the data lines if the MCU wants to read more than one parameter (= more than 2 RDX cycle) on parallel MCU interface.

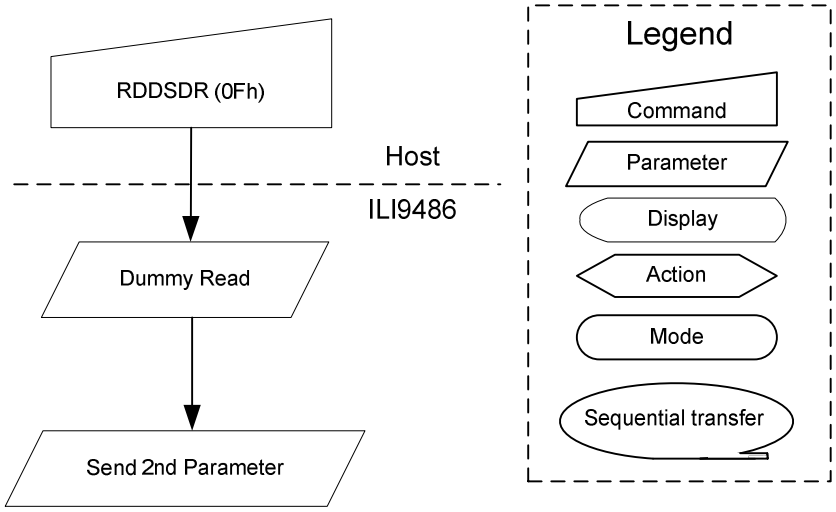
Only 2nd parameter is sent on DSI (The 1st parameter is not sent).

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00_{HEX}
SW Reset	00_{HEX}
HW Reset	00_{HEX}

Flow Chart	

8.2.12. Sleep IN (10h)

10h	SLPIN (Sleep IN)												
	D/CX	RDX	WRX	D[15:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XXXXXXXX	0	0	0	1	0	0	0	0	10h
Parameter	No parameter												
Description	This command causes ILI9486 to enter the minimum power consumption mode. In this mode e.g. the DC/DC converter is stopped, Internal oscillator is stopped, and panel scanning is stopped. Out → Blank → STOP MCU interface and memory are still working and the memory keeps its contents. Dimming function does not work when there is changing mode from Sleep OUT to Sleep IN. X = Don't care												
Restriction	This command has no effect when module is already in sleep in mode. Sleep In Mode can only be left by the Sleep Out Command (11h). It will be necessary to wait 5msec before sending next command; this is to allow time for the supply voltages and clock circuits to stabilize. It will be necessary to wait 120msec after sending Sleep Out command (when in Sleep In Mode) before Sleep In command can be sent.												

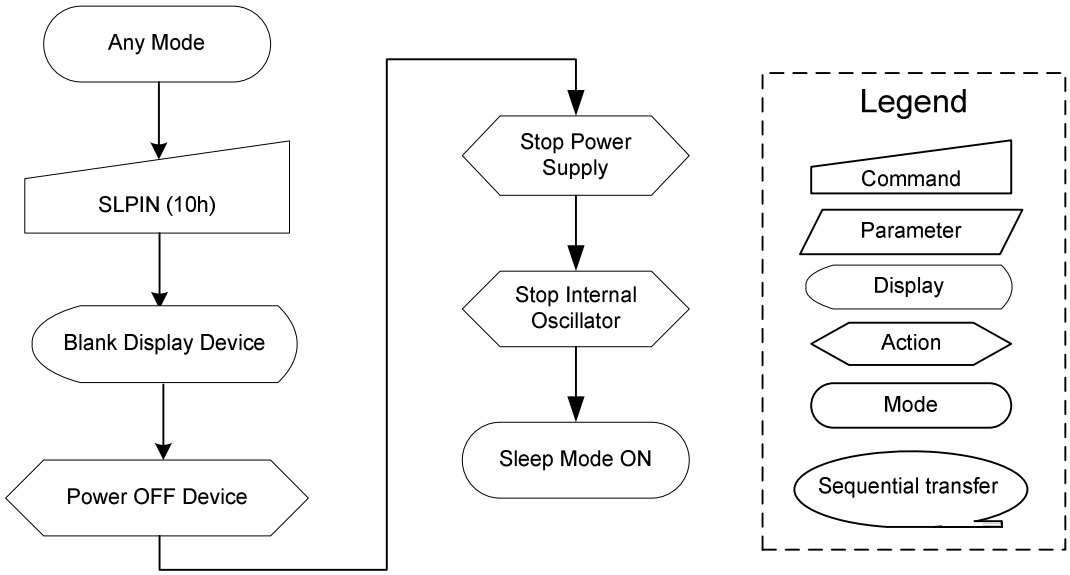
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Sleep IN Mode
SW Reset	Sleep IN Mode
HW Reset	Sleep IN Mode

Flow Chart



8.2.13. Sleep OUT (11h)

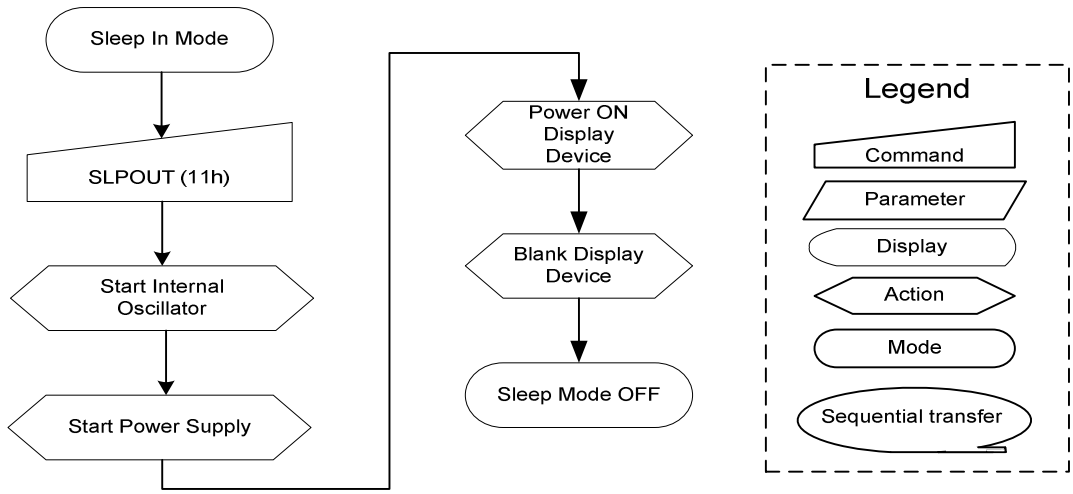
11h	SLPOUT (Sleep OUT)												
	D/CX	RDX	WRX	D[15:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XXXXXXXX	0	0	0	1	0	0	0	1	11h
Parameter	No parameter												
Description	This command turns off sleep mode. In this mode e.g. the DC/DC converter is enabled, Internal oscillator is started, and panel scanning is started.  X = Don't care												
Restriction	Sleep Out Mode can only be left by the Sleep In Command (10h). It will be necessary to wait 5msec before sending next command; this is to allow time for the supply voltages and clock circuits to stabilize. ILI9486 loads all display supplier's factory default values to the registers during this 5msec and there cannot be any abnormal visual effect on the display image if factory default and register values are same when this load is done and when ILI9486 is already Sleep Out –mode. ILI9486 is doing self-diagnostic functions during this 5msec. It will be necessary to wait 120msec after sending Sleep In command (when in Sleep Out mode) before Sleep Out command can be sent.												
Register Availability													

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Sleep IN Mode
SW Reset	Sleep IN Mode
HW Reset	Sleep IN Mode

Flow Chart



8.2.14. Partial Mode ON (12h)

12h	PTLON (Partial Mode ON)												
	D/CX	RDX	WRX	D[15:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XXXXXXXX	0	0	0	1	0	0	1	0	12h
Parameter	No parameter												
Description	This command turns on partial mode The partial mode window is described by the Partial Area command (30H). To leave Partial mode, the Normal Display Mode On command (13H) should be written.												
Restriction	This command has no effect when Partial Display Mode is already active.												
Register Availability													

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Sleep IN Mode
SW Reset	Sleep IN Mode
HW Reset	Sleep IN Mode

Flow Chart	See Partial Area (30h)

8.2.15. Normal Display Mode ON (13h)

13h	NORON (Normal Display Mode ON)												
	D/CX	RDX	WRX	D[15:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XXXXXXXX	0	0	0	1	0	0	1	1	13h
Parameter	No parameter												
Description	This command returns the display to normal mode. Normal display mode on means Partial mode off and Scroll mode off. X = Don't care												
Restriction	This command has no effect when Normal Display mode is active.												
Register Availability													

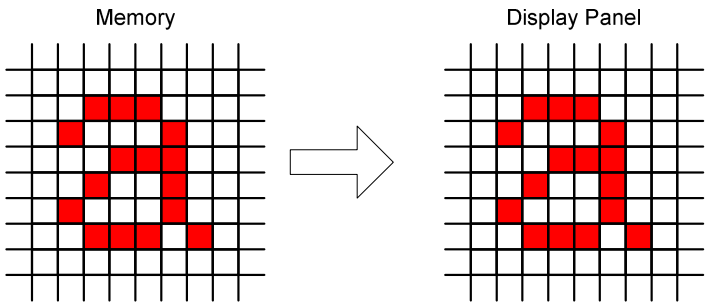
Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Normal Display Mode On
SW Reset	Normal Display Mode On
HW Reset	Normal Display Mode On

Flow Chart	See Partial Area Descriptions for details of when to use this command.

8.2.16. Display Inversion OFF (20h)

20h	INVOFF (Display Inversion OFF)												
	D/CX	RDX	WRX	D[15:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XXXXXXXX	0	0	1	0	0	0	0	0	20h
Parameter	No parameter												
Description	This command is used to recover from display inversion mode. Output from the Frame Memory is enabled. This command makes no change of the content of frame memory. This command doesn't change any other status.  X = Don't care												
Restriction	This command has no effect when ILI9486 is already in Inversion off mode.												

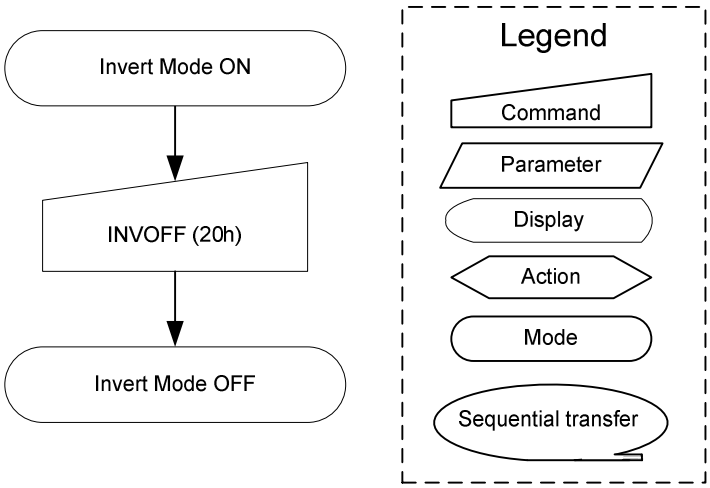
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

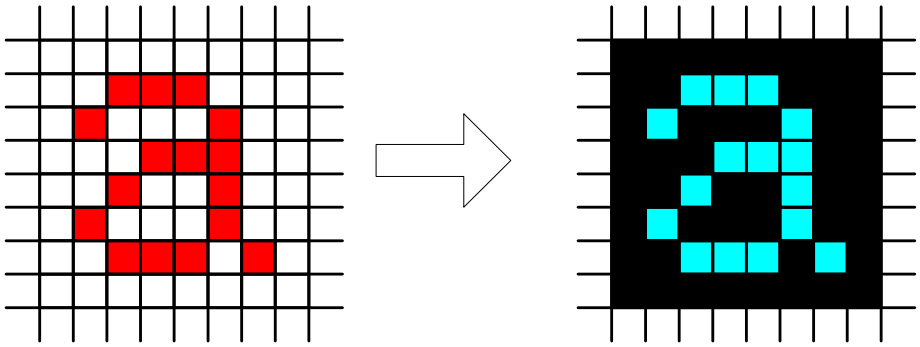
Default

Status	Default Value
Power On Sequence	Display Inversion OFF
SW Reset	Display Inversion OFF
HW Reset	Display Inversion OFF

Flow Chart



8.2.17. Display Inversion ON (21h)

21h	INVON (Display Inversion ON)												
	D/CX	RDX	WRX	D[15:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XXXXXXXX	0	0	1	0	0	0	0	1	21h
Parameter	No parameter												
Description	This command is used to enter into display inversion mode. This command makes no change of the content of frame memory. Every bit is inverted from the frame memory to the display. This command doesn't change any other status. To exit Display inversion mode, the Display inversion OFF command (20h) should be written.  X = Don't care												
Restriction	This command has no effect when ILI9486 is already in Inversion on mode.												

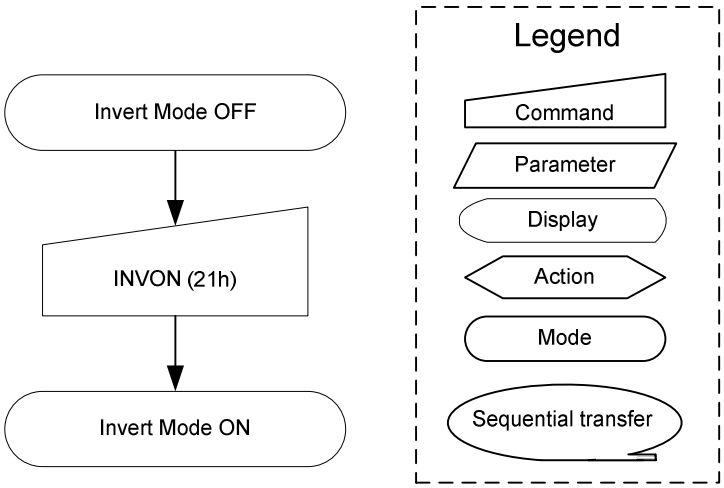
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

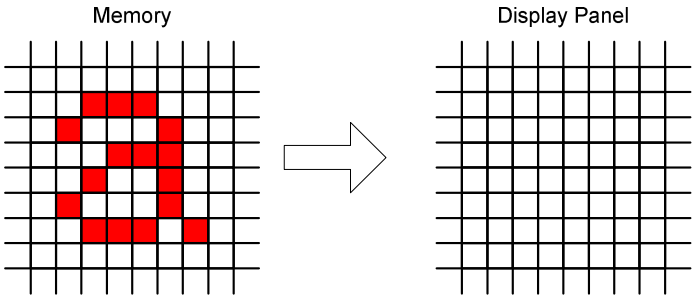
Default

Status	Default Value
Power On Sequence	Display Inversion OFF
SW Reset	Display Inversion OFF
HW Reset	Display Inversion OFF

Flow Chart



8.2.18. Display OFF (28h)

28h	DISOFF (Display OFF)												
	D/CX	RDX	WRX	D[15:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XXXXXXXX	0	0	1	0	1	0	0	0	28h
Parameter	No parameter												
Description	This command causes ILI9486 to stop displaying the image data on the display device. The frame memory contents remain unchanged. No status bits are changed.  X = Don't care												
Restriction	This command has no effect when ILI9486 is already in Display off mode.												

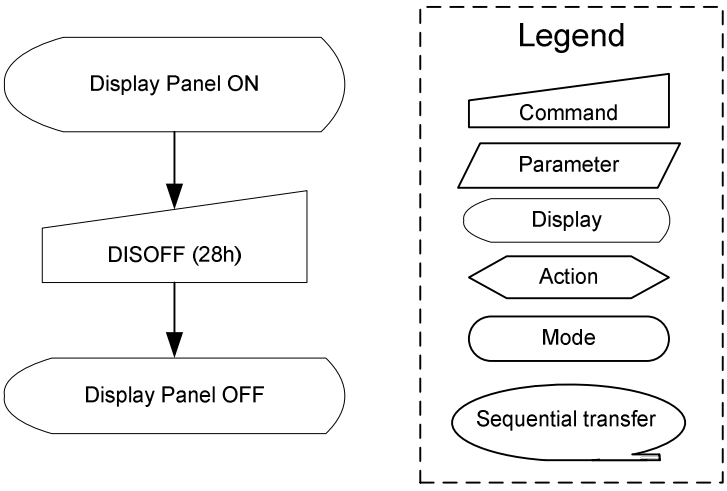
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Display OFF
SW Reset	Display OFF
HW Reset	Display OFF

Flow Chart

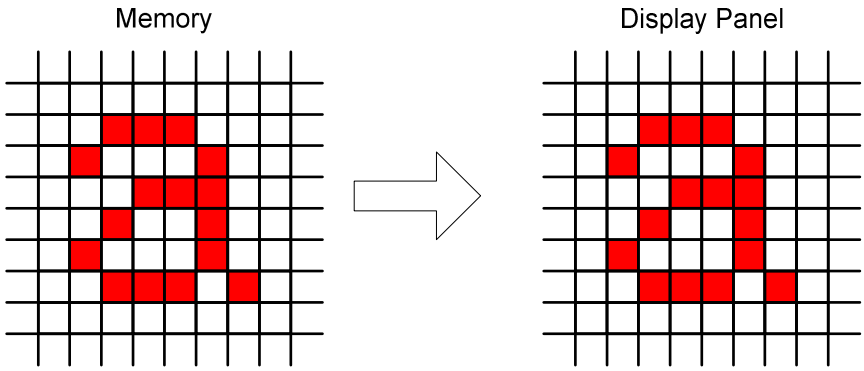


8.2.19. Display ON (29h)

29h	DISON (Display ON)												
	D/CX	RDX	WRX	D[15:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XXXXXXXX	0	0	1	0	1	0	0	1	29h
Parameter	No parameter												

Description

This command causes ILI9486 to start displaying the image data on the display device. The frame memory contents remain unchanged. No status bits are changed.



X = Don't care

Restriction

This command has no effect when ILI9486 is already in Display on mode.

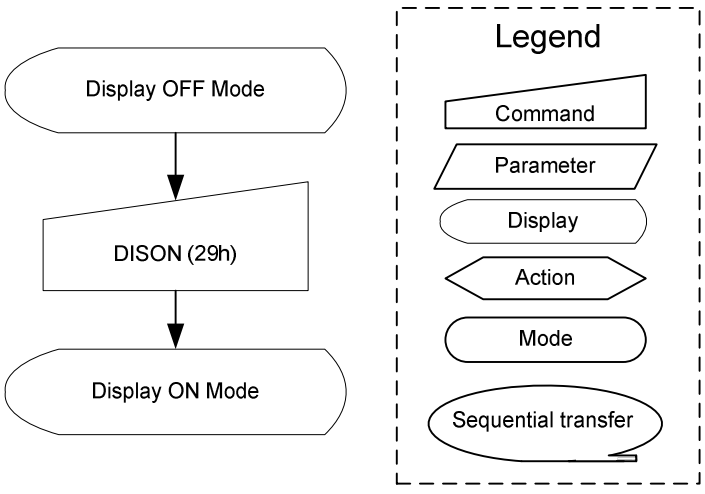
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Display OFF
SW Reset	Display OFF
HW Reset	Display OFF

Flow Chart

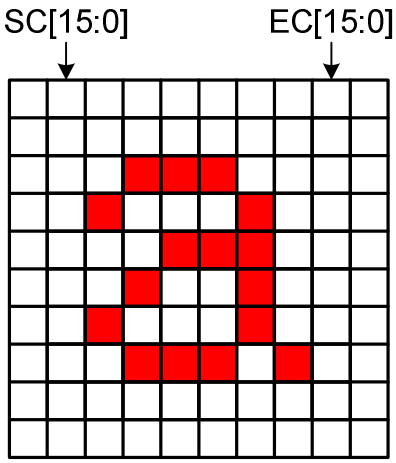


8.2.20. Column Address Set (2Ah)

2Ah	CASET (Column Address Set)												
	D/CX	RDX	WRX	D[15:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XXXXXXXX	0	0	1	0	1	0	1	0	2Ah
1st Parameter	1	1	↑	XXXXXXXX	SC[15:8]								XX
2nd Parameter	1	1	↑	XXXXXXXX	SC[7:0]								XX
3rd Parameter	1	1	↑	XXXXXXXX	EC[15:8]								XX
4th Parameter	1	1	↑	XXXXXXXX	EC[7:0]								XX

Description

This command is used to define area of frame memory where MCU can access. This command makes no change on the other driver status. The values of SC[15:0] and EC[15:0] are referred when RAMWR command comes. Each value represents one column line in the Frame Memory.



Restriction

SC[15:0] always must be equal to or less than EC[15:0].

Note 1: When SC[15:0] or EC[15:0] is greater than 013Fh (When MADCTL's B5 = 0) or 01DFh (When MADCTL's B5 = 1), data of out of range will be ignored

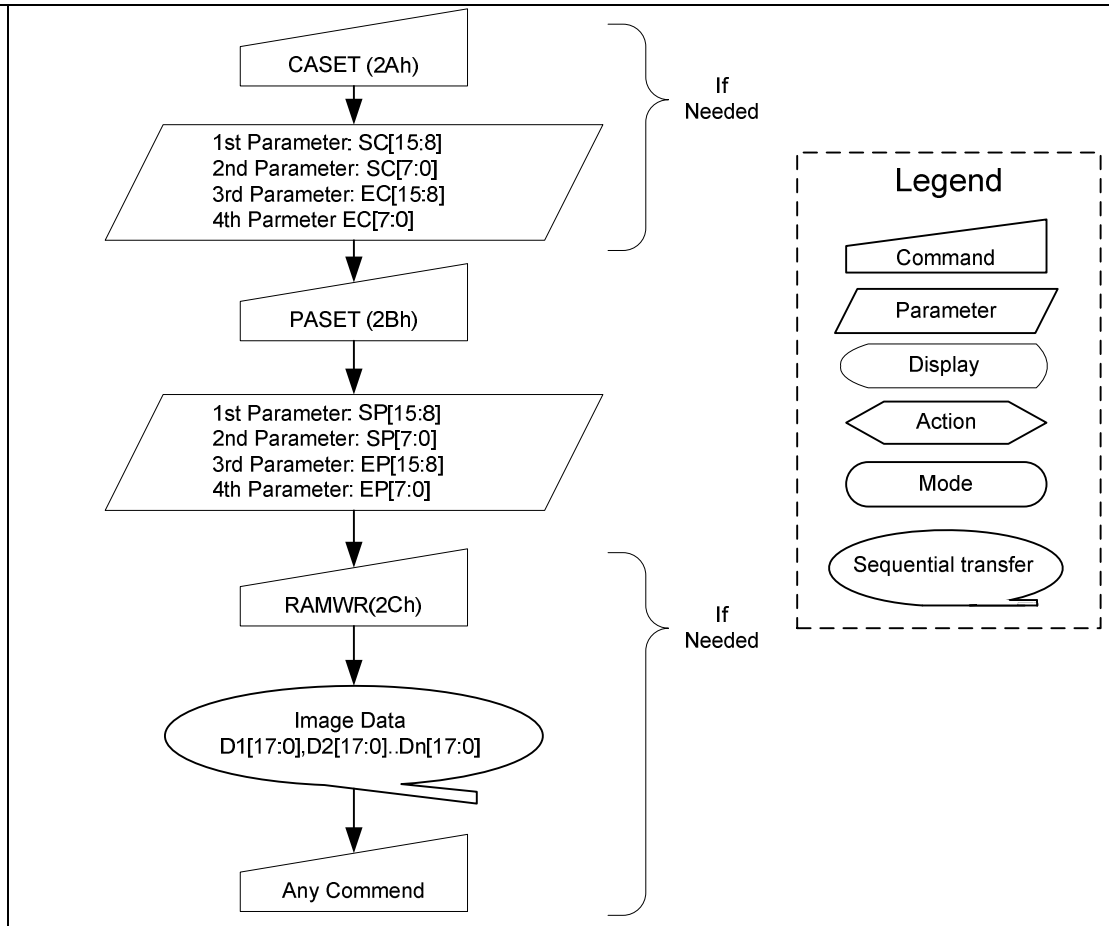
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value	
Power On Sequence	SC[15:0]=0000h	EC[15:0]=00EFh
SW Reset	SC[15:0]=0000h	If MADCTL's B5 = 0: EC[15:0]=013Fh If MADCTL's B5 = 1: EC[15:0]=01DFh
HW Reset	SC[15:0]=0000h	EC[15:0]=013Fh

Flow Chart

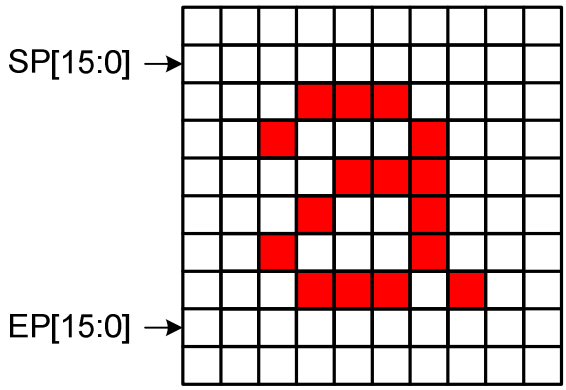


8.2.21. Page Address Set (2Bh)

2Bh	PASET (Page Address Set)												
	D/CX	RDX	WRX	D[15:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XXXXXXXX	0	0	1	0	1	0	1	1	2Bh
1st Parameter	1	1	↑	XXXXXXXX	SP[15:8]								XX
2nd Parameter	1	1	↑	XXXXXXXX	SP[7:0]								XX
3rd Parameter	1	1	↑	XXXXXXXX	EP[15:8]								XX
4th Parameter	1	1	↑	XXXXXXXX	EP[7:0]								XX

Description

This command is used to define area of frame memory where MCU can access. This command makes no change on the other driver status. The values of SP[15:0] and EP[15:0] are referred when RAMWR command comes. Each value represents one Page line in the Frame Memory.



X = don't care

Restriction

SP[15:0] always must be equal to or less than EP[15:0]

When SP[15:0] or EP[15:0] is greater than 01DFh (When MADCTL's B5 = 0) or 013Fh (When MADCTL's B5 = 1), data of out of range will be ignored.

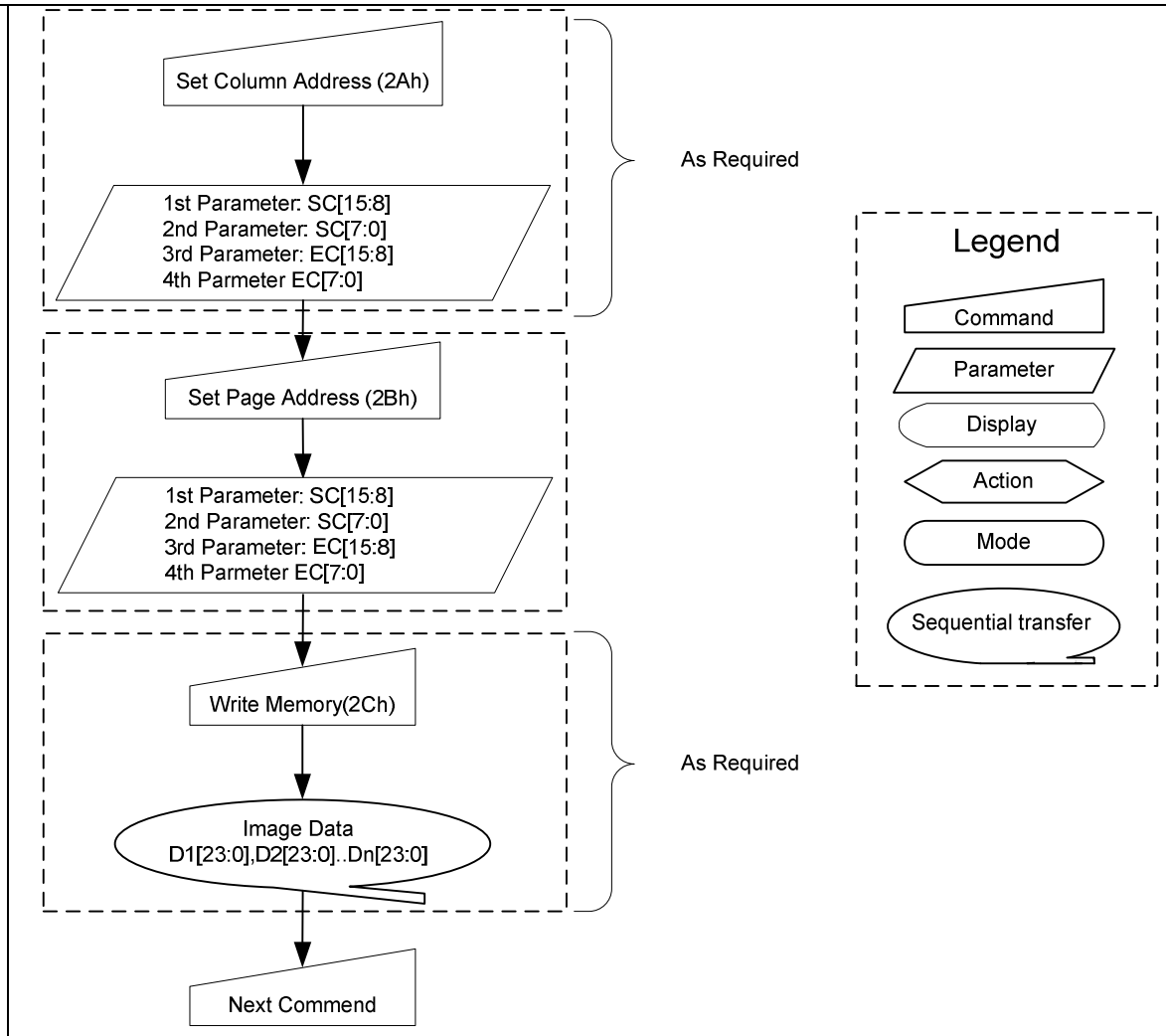
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value	
Power On Sequence	SP[15:0]=0000h	EP[15:0]=013Fh
SW Reset	SP[15:0]=0000h	If MADCTL's B5 = 0: EP[15:0]=01DFh If MADCTL's B5 = 1: EP[15:0]=013Fh
HW Reset	SP[15:0]=0000h	EP[15:0]=01EFh

Flow Chart



8.2.22. Memory Write (2Ch)

2Ch	RAMWR (Memory Write)												
	D/CX	RDX	WRX	D[15:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XXXXXXXX	0	0	1	0	1	1	0	0	2Ch
1st Parameter	1	1	↑	D1[15:0]									XX
:	1	1	↑	Dx[15:0]									XX
Nth Parameter	1	1	↑	Dn[15:0]									XX

Description

This command transfers image data from the host processor to ILI9486's frame memory starting at the pixel location specified by preceding Column Address Set (2Ah) and Page Address Set (2Bh) commands.

If Memory Access Control (36h) B5 = 0:

The column and page registers are reset to the Start Column (SC) and Start Page (SP), respectively. Pixel Data 1 is stored in frame memory at (SC, SP). The column register is then incremented and pixels are written to the frame memory until the column register equals the End Column (EC) value. The column register is then reset to SC and the page register is incremented. Pixels are written to the frame memory until the page register equals the End Page (EP) value or the host processor sends another command. If the number of pixels exceeds (EC – SC + 1) * (EP – SP + 1) the extra pixels are ignored.

If Memory Access control (36h) B5 = 1:

The column and page registers are reset to the Start Column (SC) and Start Page (SP), respectively. Pixel Data 1 is stored in frame memory at (SC, SP). The page register is then incremented and pixels are written to the frame memory until the page register equals the End Page (EP) value. The page register is then reset to SP and the column register is incremented. Pixels are written to the frame memory until the column register equals the End column (EC) value or the host processor sends another command. If the number of pixels exceeds (EC – SC + 1) * (EP – SP + 1) the extra pixels are ignored.

Restriction

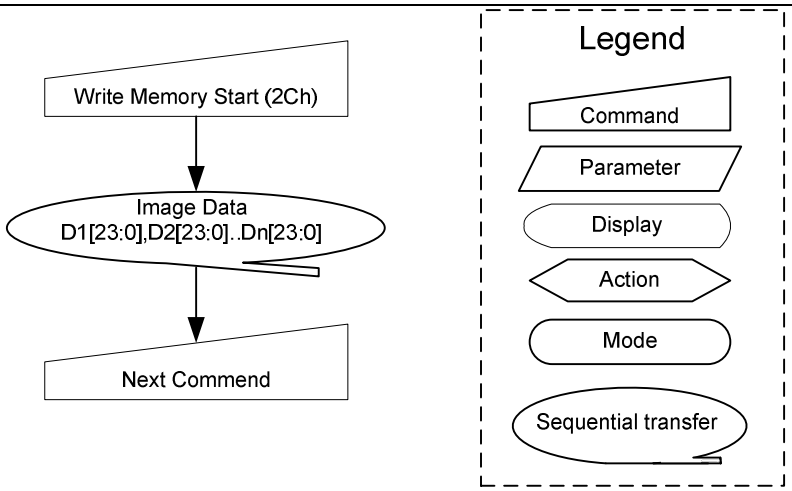
There is no restriction on length of parameters.

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Contents of memory is set randomly
SW Reset	Contents of memory is set randomly
HW Reset	Contents of memory is set randomly

Flow Chart	

8.2.23. Memory Read (2Eh)

2Eh	RAMRD (Memory Read)												
	D/CX	RDX	WRX	D[15:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XXXXXXXX	0	0	1	0	1	1	1	0	2Eh
1st Parameter	1	1	↑	XXXXXXXX	X	X	X	X	X	X	X	X	XX
2nd Parameter	1	1	↑	D1[15:0]									XX
:	1	1	↑	Dx[15:0]									XX
(N+1)th Parameter	1	1	↑	Dn[15:0]									XX

Description

This command transfers image data from ILI9486's frame memory to the host processor starting at the pixel location specified by preceding set_column_address and set_page_address commands.

If Memory Access control B5 = 0:

The column and page registers are reset to the Start Column (SC) and Start Page (SP), respectively. Pixels are read from frame memory at (SC, SP). The column register is then incremented and pixels read from the frame memory until the column register equals the End Column (EC) value. The column register is then reset to SC and the page register is incremented. Pixels are read from the frame memory until the page register equals the End Page (EP) value or the host processor sends another command.

If Memory Access Control B5 = 1:

The column and page registers are reset to the Start Column (SC) and Start Page (SP), respectively. Pixels are read from frame memory at (SC, SP). The page register is then incremented and pixels read from the frame memory until the page register equals the End Page (EP) value. The page register is then reset to SP and the column register is incremented. Pixels are read from the frame memory until the column register equals the End Column (EC) value or the host processor sends another command.

Restriction

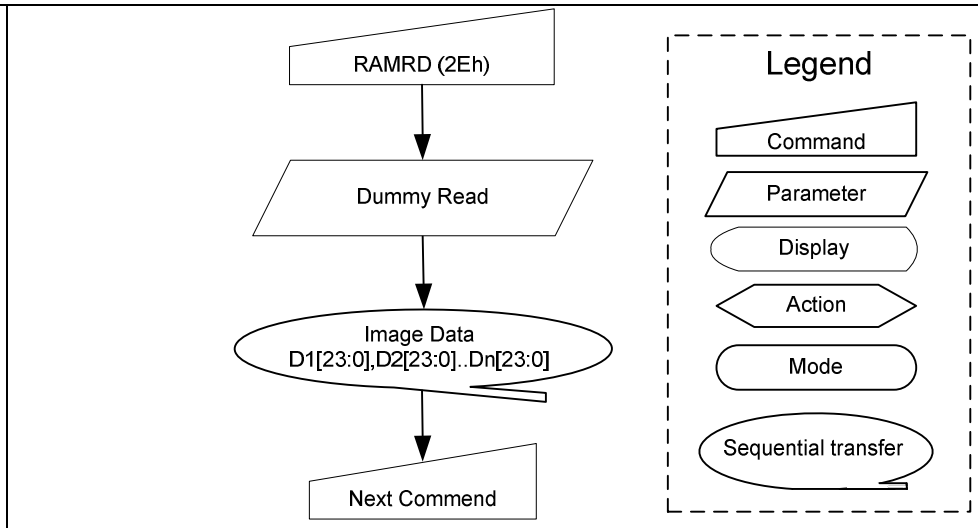
There is no restriction on length of parameters.

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Contents of memory is set randomly
SW Reset	Contents of memory is set randomly
HW Reset	Contents of memory is set randomly

Flow Chart	

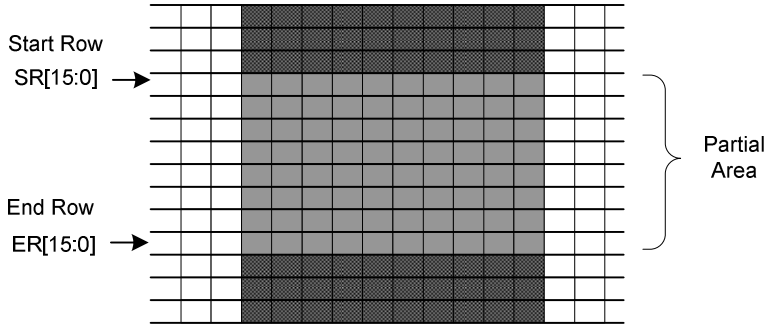
8.2.24. Partial Area (30h)

30h	PLTAR (Partial Area)												
	D/CX	RDX	WRX	D[15:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XXXXXXXX	0	0	1	1	0	0	0	0	30h
1st Parameter	1	1	↑	XXXXXXXX	SR[15:8]								XX
2nd Parameter	1	1	↑	XXXXXXXX	SR[7:0]								XX
3rd Parameter	1	1	↑	XXXXXXXX	ER[15:8]								XX
4th Parameter	1	1	↑	XXXXXXXX	ER[7:0]								XX

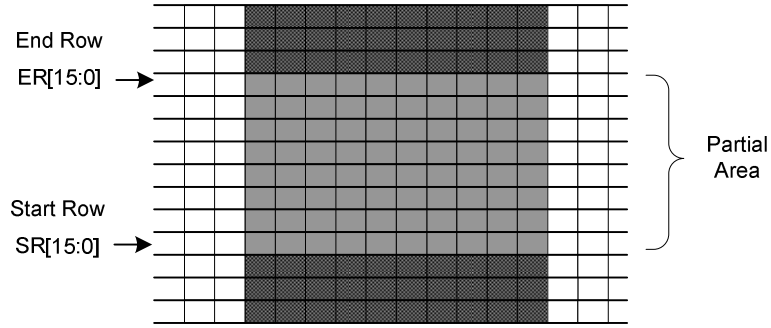
Description

This command defines the Partial Display mode's display area. There are two parameters associated with this command, the first defines the Start Row (SR) and the second the End Row (ER), as illustrated in the following figure. SR and ER refer to the Frame Memory

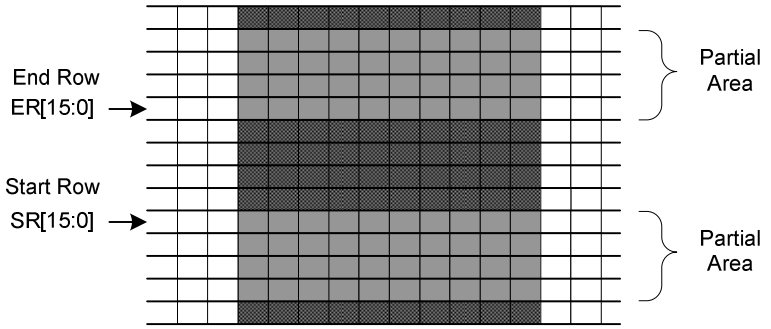
If End Row>Start Row when MADCTL B4=0:-



If End Row>Start Row when MADCTL B4=1:-



If End Row<Start Row when MADCTL B4=0:-



If End Row = Start Row then the Partial Area will be one row deep.

X = don't care.

Restriction

SR[15:0] and ER[15:0] cannot be 0000h nor exceed the last vertical line number (01EFh).

Register Availability

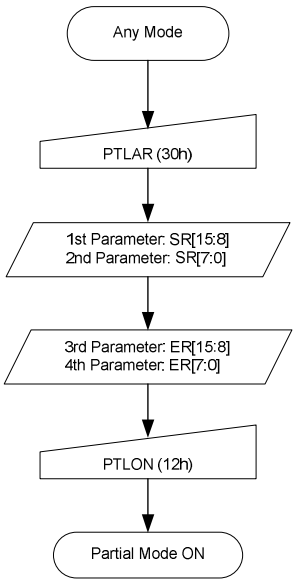
Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

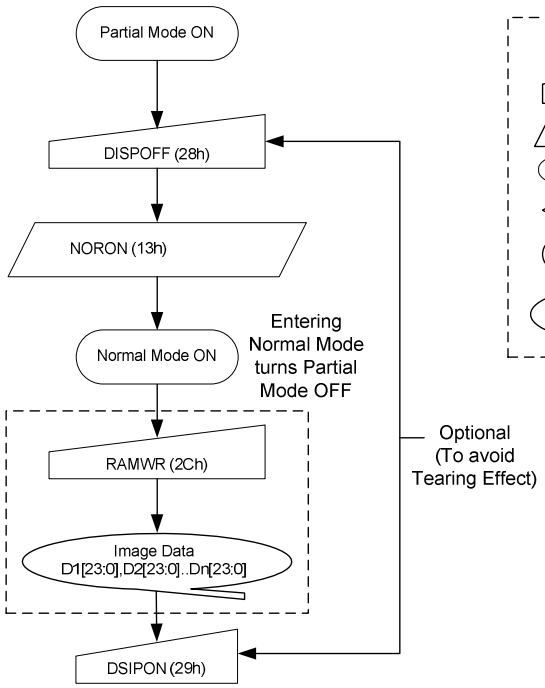
Status	Default Value	
Power On Sequence	SR[15:0]=0000_{HEX}	ER[15:0]=$01DF_{HEX}$
SW Reset	SR[15:0]=0000_{HEX}	ER[15:0]=$01DF_{HEX}$
HW Reset	SR[15:0]=0000_{HEX}	ER[15:0]=$01DF_{HEX}$

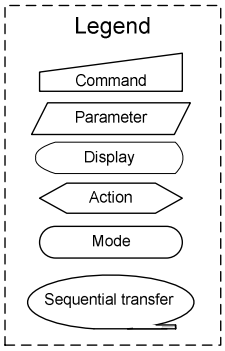
Flow Chart

1. To Enter Partial Mode



2. To Exit Partial Mode





8.2.25. Vertical Scrolling Definition (33h)

33h	VSCRDEF (Vertical Scrolling Definition)												
	D/CX	RDX	WRX	D[15:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XXXXXXXX	0	0	1	1	0	0	1	1	33h
1st Parameter	1	1	↑	XXXXXXXX	TFA[15:8]								XX
2nd Parameter	1	1	↑	XXXXXXXX	TFA[7:0]								XX
3rd Parameter	1	1	↑	XXXXXXXX	VSA[15:8]								XX
4th Parameter	1	1	↑	XXXXXXXX	VSA[7:0]								XX
5th Parameter	1	1	↑	XXXXXXXX	BFA[15:8]								XX
6th Parameter	1	1	↑	XXXXXXXX	BFA[7:0]								XX

Description

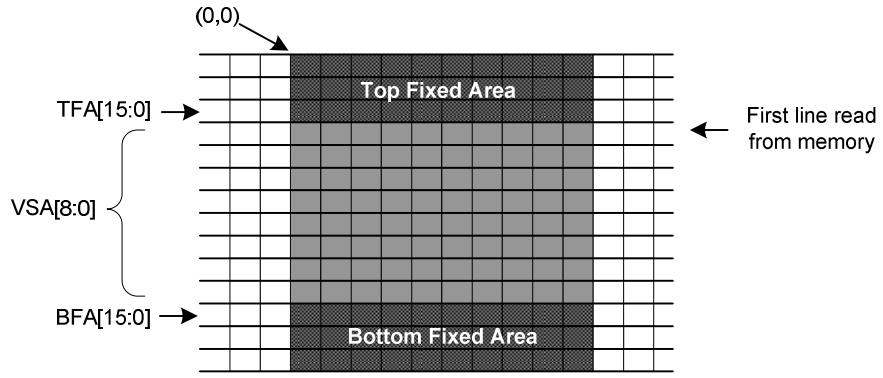
This command defines the display vertical scrolling area.

Memory Access Control (36h) B4 = 0:

The 1st & 2nd parameter, TFA[8:0], describes the Top Fixed Area in number of lines from the top of the frame memory. The top of the frame memory and top of the display device are aligned. The 3rd & 4th parameter, VSA[8:0], describes the height of the Vertical Scrolling Area in number of lines of frame memory from the Vertical Scrolling Start Address. The first line of the Vertical Scrolling Area starts immediately after the bottom most line of the Top Fixed Area. The last line of the Vertical Scrolling Area ends immediately before the top most line of the Bottom Fixed Area.

The 5th & 6th parameter, BFA[8:0], describes the Bottom Fixed Area in number of lines from the bottom of the frame memory. The bottom of the frame memory and bottom of the display device are aligned.

TFA, VSA and BFA refer to the Frame Memory Line Pointer.



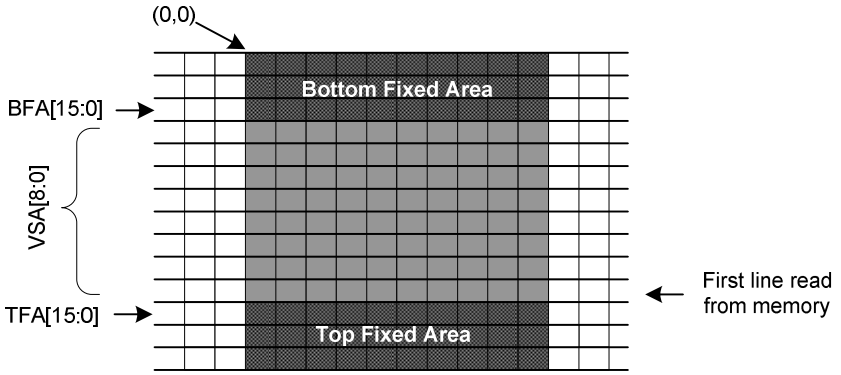
Memory Access Control (36h) B4 = 1:

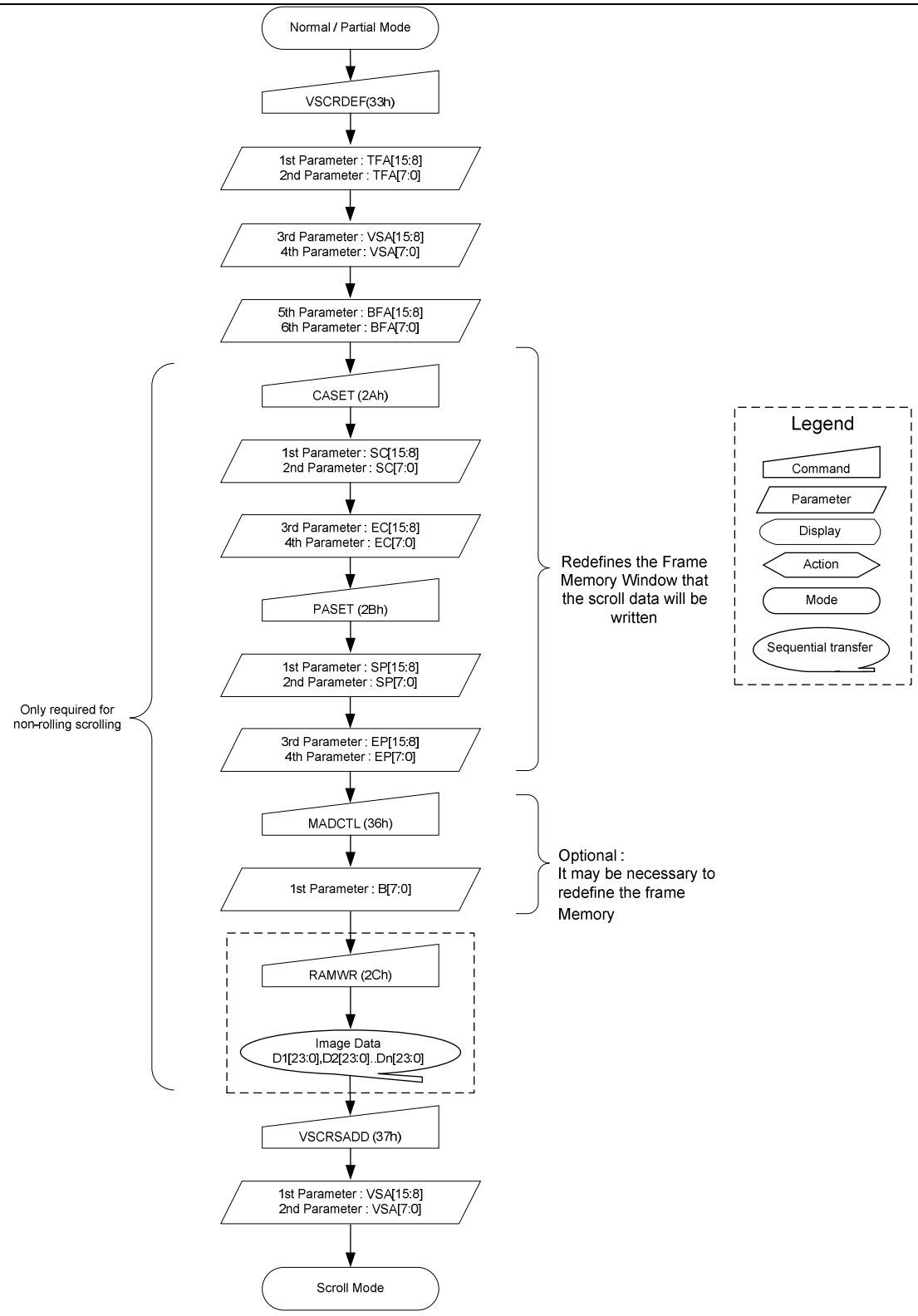
The 1st & 2nd parameter, TFA[8:0], describes the Top Fixed Area in number of lines from the bottom of the frame memory. The bottom of the frame memory and bottom of the display device are aligned.

The 3rd & 4th parameter, VSA[8:0], describes the height of the Vertical Scrolling Area in number of lines of frame memory from the Vertical Scrolling Start Address. The first line of the Vertical Scrolling Area starts immediately after the top most line of the Top Fixed Area. The last line of the Vertical Scrolling Area ends immediately before the bottom most line of the Bottom Fixed Area.

The 5th & 6th parameter, BFA[8:0], describes the Bottom Fixed Area in number of lines from the top of the frame memory. The top of the frame memory and top of the display device are aligned.

TFA, VSA and BFA refer to the Frame Memory Line Pointer.

<table>
<tr><td></td><td> 
</td></tr>
<tr><td>Restriction</td><td>The sum of TFA, VSA and BFA must equal the number of the display device’s horizontal lines (pages), otherwise Scrolling mode is undefined. In Vertical Scroll Mode, set_address_mode B5 should be set to ‘0’ – this only affects the Frame Memory Write.</td></tr>
<tr><td>Register Availability</td><td><table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table></td></tr>
<tr><td>Default</td><td><table>
<tr><th>Status</th><th colspan="3">Default Value</th></tr>
<tr><td>Power On Sequence</td><td>TFA[15:0]=0000_{HEX}</td><td>VSA[15:0]=$01E0_{HEX}$</td><td>BFA[15:0]=0000_{HEX}</td></tr>
<tr><td>SW Reset</td><td>TFA [15:0]=0000_{HEX}</td><td>VSA[15:0]=$01E0_{HEX}$</td><td>BFA[15:0]=0000_{HEX}</td></tr>
<tr><td>HW Reset</td><td>TFA [15:0]=0000_{HEX}</td><td>VSA[15:0]=$01E0_{HEX}$</td><td>BFA[15:0]=0000_{HEX}</td></tr>
</table></td></tr>
<tr><td>Flow Chart</td><td>1. To enter Vertical Scroll Mode:</td></tr>
</table>



Since the value of the Vertical Scrolling Start Address is absolute with reference to the Frame Memory, it must not enter the fixed area; otherwise an undesirable image may be shown on the Display Panel.

8.2.26. Tearing Effect Line OFF (34h)

34h	TEOFF (Tearing Effect Line OFF)												
	D/CX	RDX	WRX	D[15:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XXXXXXXX	0	0	1	1	0	1	0	0	34h
Parameter	No parameter												
Description	This command turns off ILI9486's Tearing Effect output signal on the TE signal line.												
Restriction	This command has no effect when the Tearing Effect output is already off.												

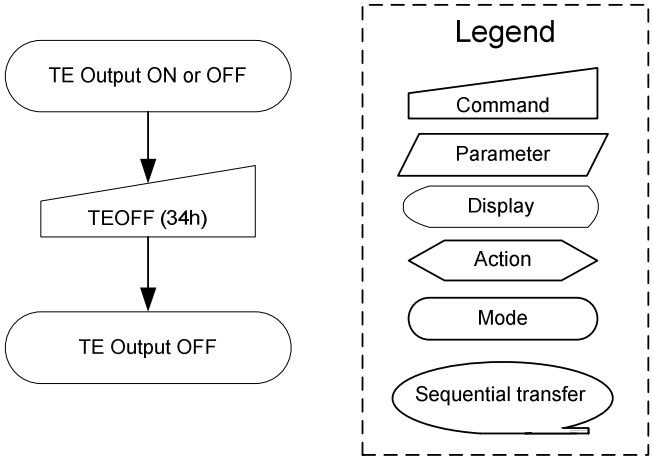
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	OFF
SW Reset	OFF
HW Reset	OFF

Flow Chart



8.2.27. Tearing Effect Line ON (35h)

35h	TEON (Tearing Effect Line ON)												
	D/CX	RDX	WRX	D[15:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XXXXXXXX	0	0	1	1	0	1	0	1	35h
Parameter	1	1	↑	XXXXXXXX	X	X	X	X	X	X	X	M	XX
Parameter	No parameter												

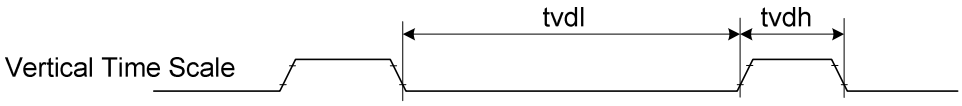
Description

This command is used to turn ON the Tearing Effect output signal from the TE signal line. This output is not affected by changing MADCTL bit B4. The Tearing Effect Line On has one parameter which describes the mode of the Tearing Effect Output Line.

(X=Don't Care).

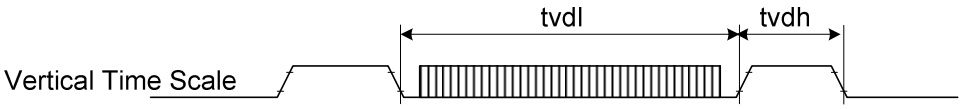
When **M=0**:

The Tearing Effect Output line consists of V-Blanking information only:



When **M=1**:

The Tearing Effect Output Line consists of both V-Blanking and H-Blanking information:



Note: During Sleep In Mode with Tearing Effect Line On, Tearing Effect Output pin will be active Low.

X = don't care.

Restriction

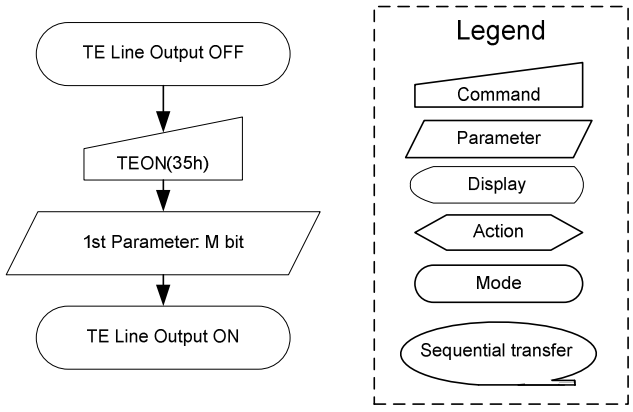
This command has no effect when the Tearing Effect output is already off.

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	OFF
SW Reset	OFF
HW Reset	OFF

Flow Chart	

8.2.28. Memory Access Control (36h)

36h	MADCTL (Memory Access Control)												
	D/CX	RDX	WRX	D[15:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XXXXXXXX	0	0	1	1	0	1	1	0	36h
Parameter	1	1	↑	XXXXXXXX	MY	MX	MV	ML	BGR	MH	X	X	XX

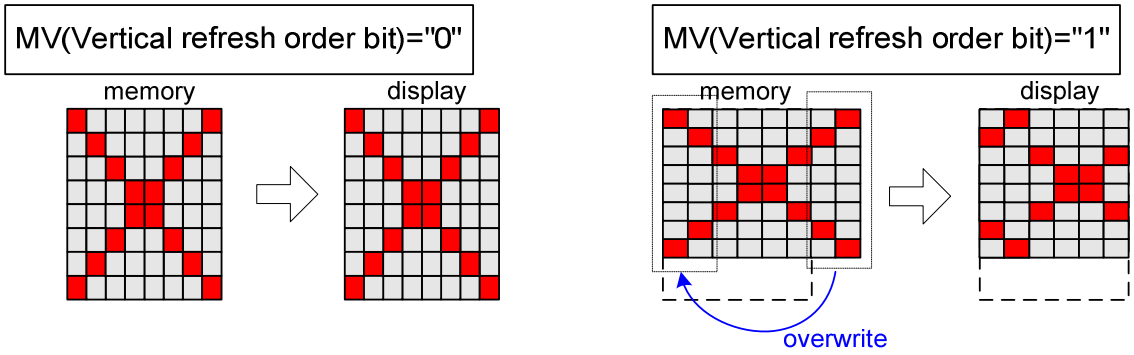
Description

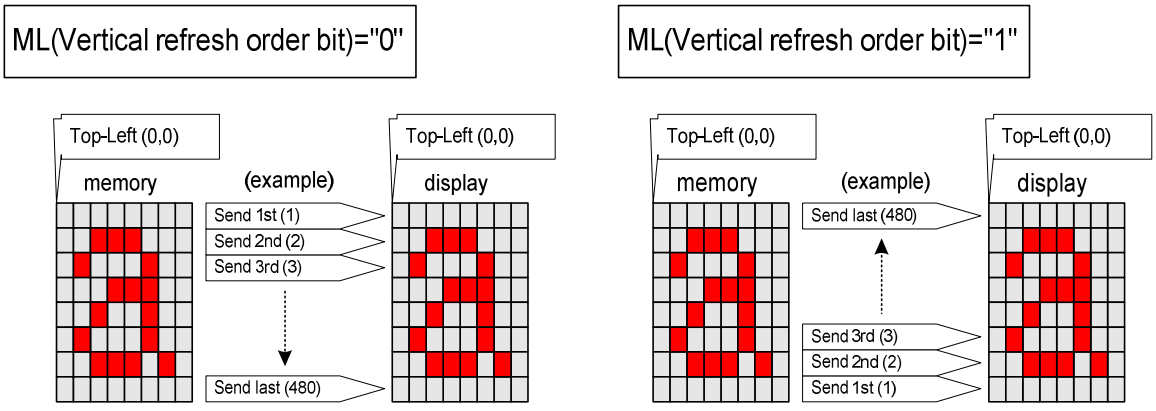
This command defines read/write scanning direction of frame memory.

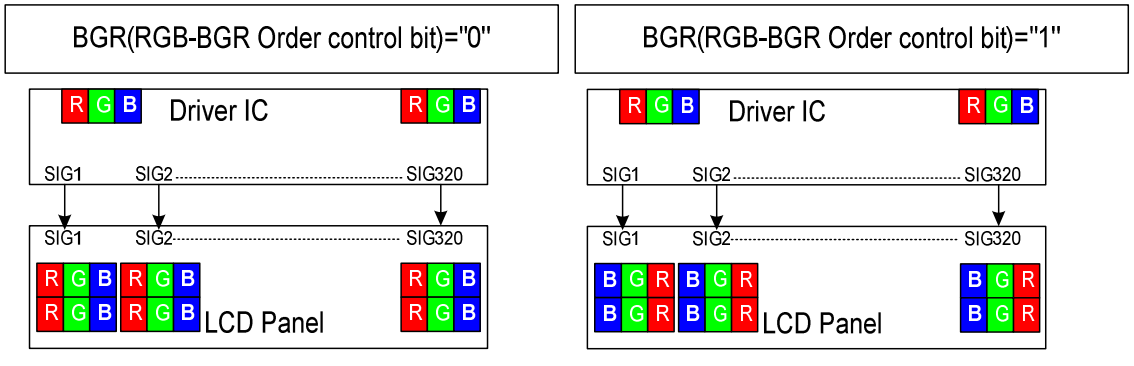
This command makes no change on the other driver status.

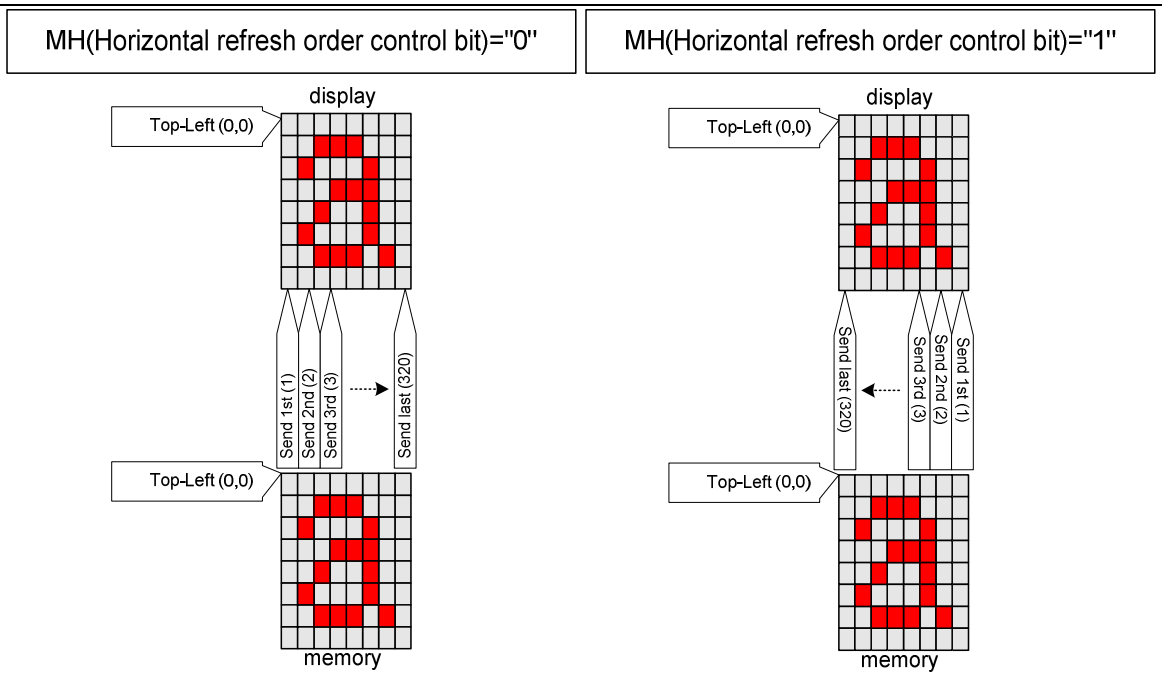
Bit	Symbol	Name	Description
D7	MY	Row Address Order	These 3 bits control MPU to memory write/read direction.
D6	MX	Column Address Order	
D5	MV	Row / Column Exchange	
D4	ML	Vertical Refresh Order	LCD vertical refresh direction control.
D3	BGR	RGB-BGR Order	Color selector switch control (0=RGB color filter panel, 1=BGR color filter panel)
D2	MH	Horizontal Refresh ORDER	LCD horizontal refreshing direction control.
D1	X	Reserved	Reserved
D0	X	Reserved	Reserved

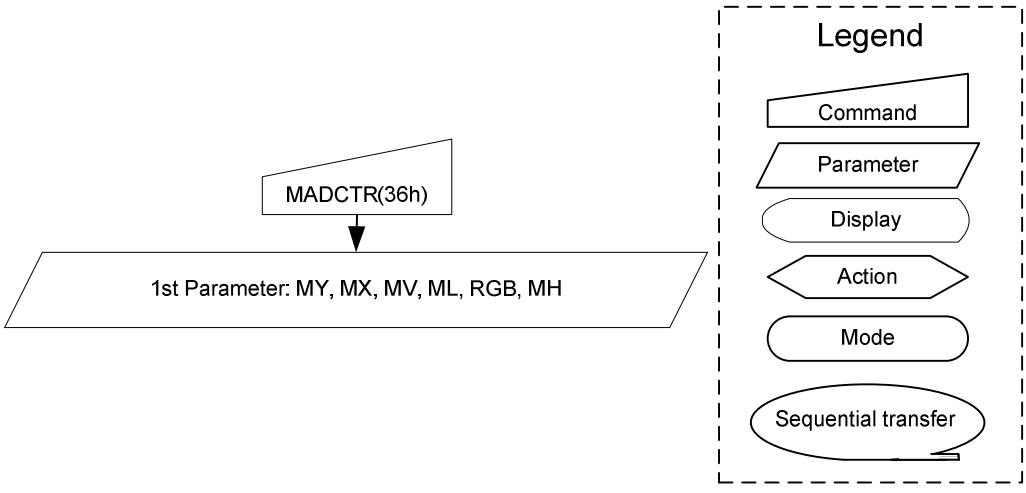
X = don't care.







<table>
<tr><td></td><td>


Note: Top-Left (0,0) means a physical memory location.
</td></tr>
<tr><td>Restriction</td><td></td></tr>
<tr><td>Register Availability</td><td>
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td>
<table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td>00h</td></tr>
<tr><td>SW Reset</td><td>No change</td></tr>
<tr><td>HW Reset</td><td>00h</td></tr>
</table>
</td></tr>
<tr><td>Flow Chart</td><td>


</td></tr>
</table>

8.2.29. Vertical Scrolling Start Address (37h)

37h	VSCRSADD (Vertical Scrolling Start Address)												
	D/CX	RDX	WRX	D[15:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XXXXXXXX	0	0	1	1	0	1	1	1	37h
1st Parameter	1	1	↑	XXXXXXXX	VSP[15:8]								XX
2nd Parameter	1	1	↑	XXXXXXXX	VSP[7:0]								XX

Description

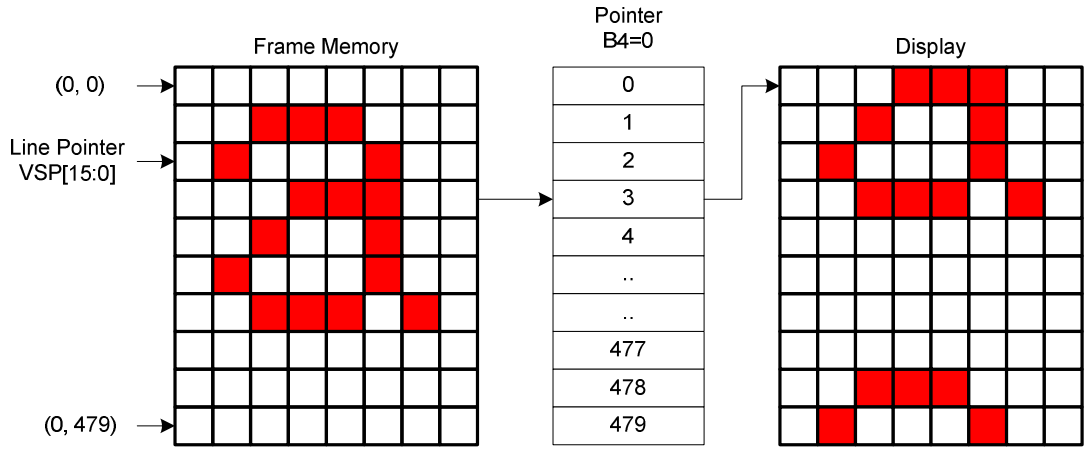
This command is used together with Vertical Scrolling Definition (33h). These two commands describe the scrolling area and the scrolling mode. The Vertical Scrolling Start Address command has one parameter which describes the address of the line in the Frame Memory that will be written as the first line after the last line of the Top Fixed Area

on the display as illustrated below:-

When MADCTL B4=0

Example:

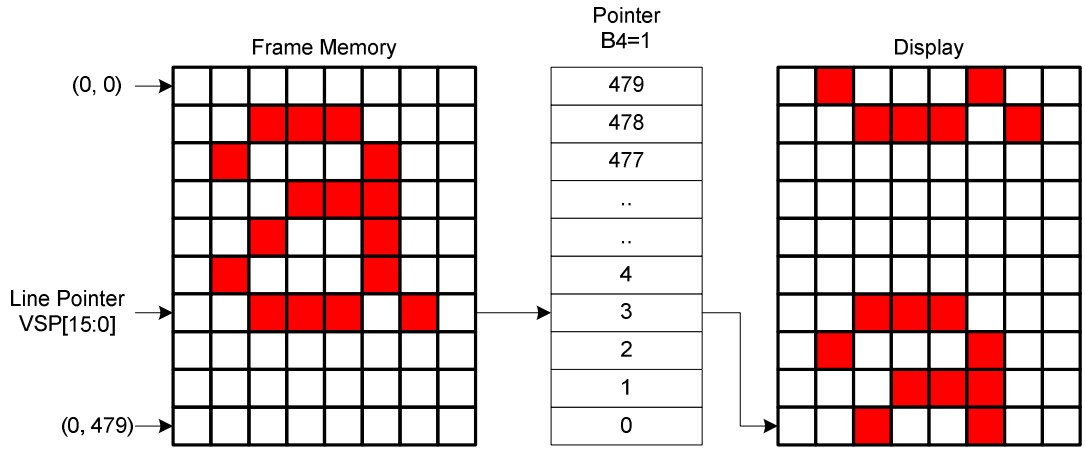
When Top Fixed Area = Bottom Fixed Area = 00, Vertical Scrolling Area = 480 and VSP='3'.



When MADCTL B4=1

Example:

When Top Fixed Area = Bottom Fixed Area = 00, Vertical Scrolling Area = 480 and VSP='3'.



Notes: (1) When new Pointer position and Picture Data are sent, the result on the display will happen at the next Panel Scan to avoid tearing effect.

VSP refers to the Frame Memory line Pointer.

X = Don't care

<table>
<tr><td>Restriction</td><td>Since the value of the Vertical Scrolling Start Address is absolute (with reference to the Frame Memory), it must not enter the fixed area (defined by Vertical Scrolling Definition (33h) – otherwise undesirable image will be displayed on the Panel.</td></tr>
<tr><td>Register Availability</td><td>
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td>
<table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td>00h</td></tr>
<tr><td>SW Reset</td><td>00h</td></tr>
<tr><td>HW Reset</td><td>00h</td></tr>
</table>
</td></tr>
<tr><td>Flow Chart</td><td>See Vertical Scrolling Definition (33h) description.</td></tr>
</table>

8.2.30. Idle Mode OFF (38h)

38h	IDMOFF (Idle Mode OFF)												
	D/CX	RDX	WRX	D[15:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XXXXXXXX	0	0	1	1	1	0	0	0	38h
Parameter	No parameter												
Description	This command causes ILI9486 to exit Idle mode. In Idle OFF mode, display panel can display maximum 262,144 colors.												
Restriction	This command has no effect when ILI9486 is not in Idle mode.												

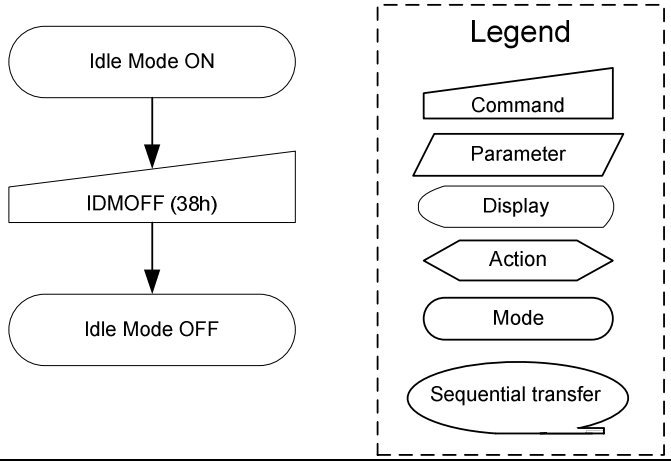
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Idle Mode Off
SW Reset	Idle Mode Off
HW Reset	Idle Mode Off

Flow Chart



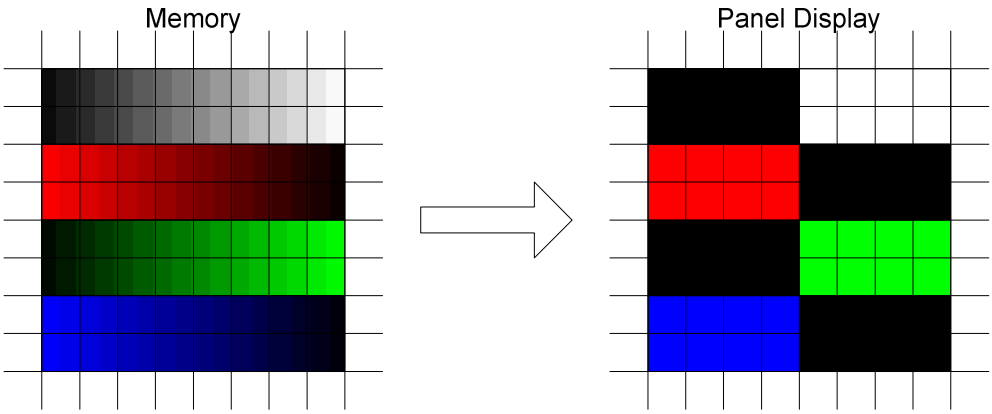
8.2.31. Idle Mode ON (39h)

39h	IDMON (Idle Mode ON)												
	D/CX	RDX	WRX	D[15:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XXXXXXXX	0	0	1	1	1	0	0	1	39h
Parameter	No parameter												

Description

This command is used to enter into Idle mode on.

In the idle on mode, color expression is reduced. The primary and the secondary colors using MSB of each R, G and B in the Frame Memory, 8 color depth data is displayed.



Memory Contents vs Display Color			
	R_5 R_4 R_3 R_2 R_1 R_0	G_5 G_4 G_3 G_2 G_1 G_0	B_5 B_4 B_3 B_2 B_1 B_0
Black	0XXXXX	0XXXXX	0XXXXX
Blue	0XXXXX	0XXXXX	1XXXXX
Red	1XXXXX	0XXXXX	0XXXXX
Magenta	1XXXXX	0XXXXX	1XXXXX
Green	0XXXXX	1XXXXX	0XXXXX
Cyan	0XXXXX	1XXXXX	1XXXXX
Yellow	1XXXXX	1XXXXX	0XXXXX
White	1XXXXX	1XXXXX	1XXXXX

X = don't care.

Restriction

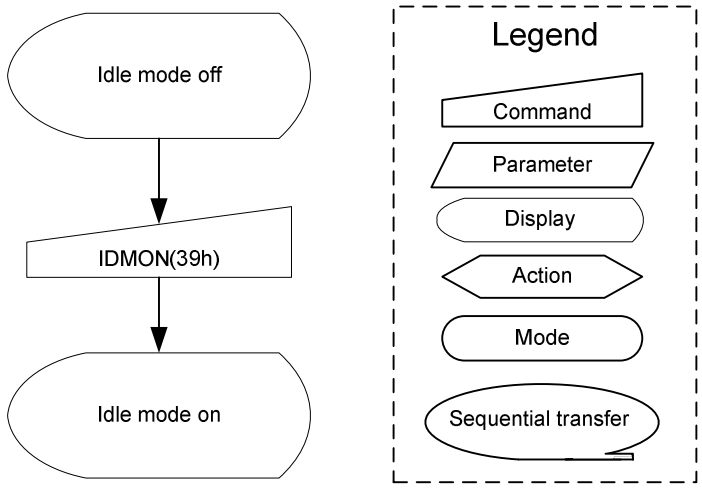
This command has no effect when module is already in idle off mode.

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Idle mode OFF
SW Reset	Idle mode OFF
HW Reset	Idle mode OFF

Flow Chart	

8.2.32. Interface Pixel Format (3Ah)

3Ah	COLMOD (Interface Pixel Format)												
	D/CX	RDX	WRX	D[15:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XXXXXXXX	0	0	1	1	1	0	1	0	3Ah
Parameter	1	1	↑	XXXXXXXX	DPI[3:0]				X	DBI[2:0]			XX

Description

This command sets the pixel format for the RGB image data used by the interface. DPI[3:0] is the pixel format select of RGB interface and DBI[2:0] is the pixel format of CPU interface. If a particular interface, either RGB interface or CPU interface, is not used then the corresponding bits in the parameter are ignored. The pixel format are shown in the table below.

DPI[3:0]				RGB Interface Format
0	0	0	0	Reserved
0	0	0	1	Reserved
0	0	1	0	Reserved
0	0	1	1	Reserved
0	1	0	0	Reserved
0	1	0	1	16 bits / pixel
0	1	1	0	18 bits / pixel
0	1	1	1	Reserved

DBI[2:0]			CPU Interface Format
0	0	0	Reserved
0	0	1	Reserved
0	1	0	Reserved
0	1	1	Reserved
1	0	0	Reserved
1	0	1	16 bits / pixel
1	1	0	18 bits / pixel
1	1	1	Reserved

X = don't care

Restriction

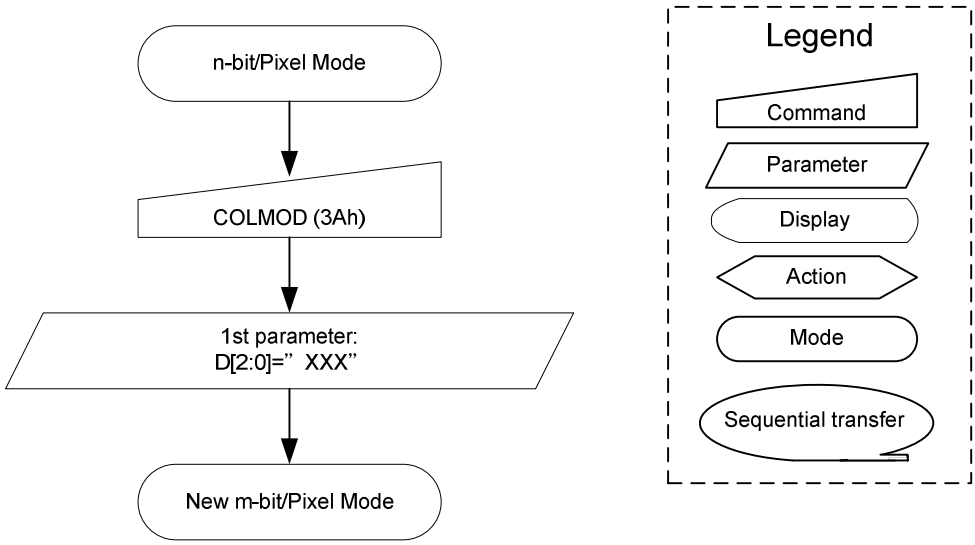
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	06h
SW Reset	06h
HW Reset	06h

Flow Chart



8.2.33. Memory Write Continue (3Ch)

3Ch	RAMWRC (Memory Write Continue)												
	D/CX	RDX	WRX	D[15:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XXXXXXXX	0	0	1	1	1	1	0	0	3Ch
1st Parameter	1	1	↑	D1[15:0]									XX
:	1	1	↑	Dx[15:0]									XX
Nth Parameter	1	1	↑	Dn[15:0]									XX

Description

This command is used to transfer data from MCU to frame memory, if there is wanted to continue memory write after "Memory Write (2Ch)" command.

This command makes no change to the other driver status.

When this command is accepted, the column register and the page register are not reset to the Start Column/Start Page positions as it has been done on "Memory Write (2Ch)" command.

Then D[15:0] is stored in frame memory and the column register and the page register incremented as table below: Column and Page Counter Control.

Condition	Column counter	Page Counter
When RAMWR/RAMRD command is accepted	Return to "Start Column"	Return to "Start Page"
Complete Pixel Read/Write action	Increment by 1	No change
The Column counter value is large than "End Column"	Return to "Start Column"	Increment by 1
The Page counter value is large than "End Page"	Return to "Start Column"	Return to "Start Page"

Sending any other command can stop frame Write.

X = don't care.

Restriction

There is no restriction on length of parameters.

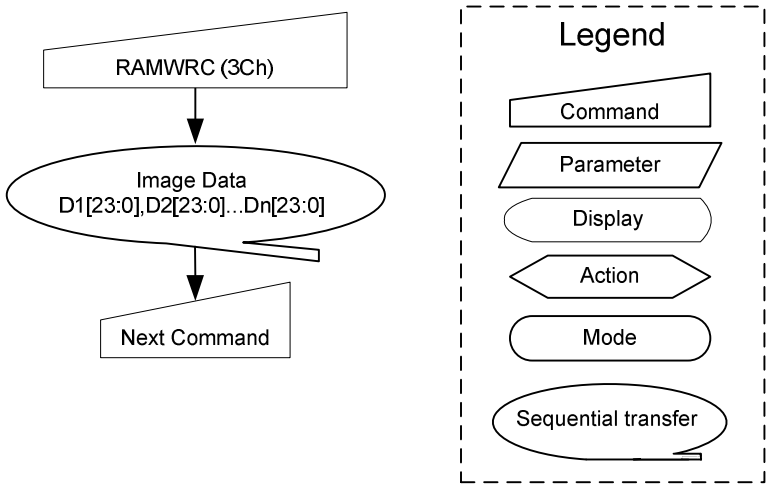
No access in the frame memory in Sleep In mode.

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

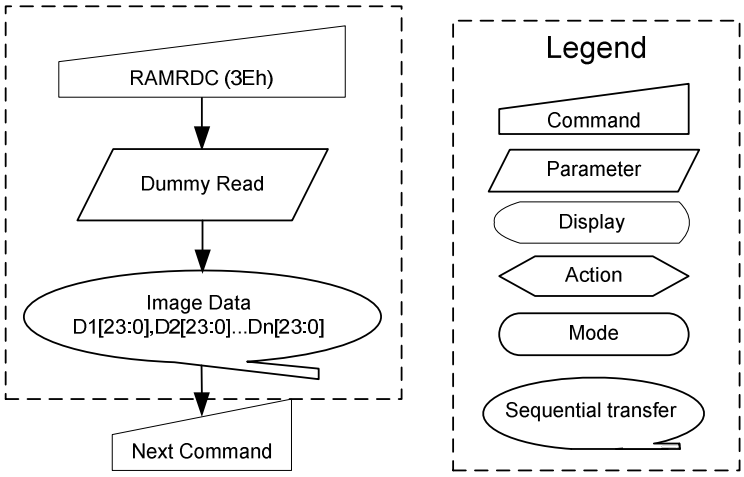
Default

Status	Default Value
Power On Sequence	Contents of memory is set randomly
SW Reset	Contents of memory is set randomly
HW Reset	Contents of memory is set randomly

Flow Chart	

8.2.34. Memory Read Continue (3Eh)

<table>
<tr><th>3Eh</th><th colspan="12">RAMRDRC (Memory Read Continue)</th></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D[15:8]</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XXXXXXXX</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>0</td><td>3Eh</td></tr>
<tr><td>1st Parameter</td><td>1</td><td>↑</td><td>1</td><td>XXXXXXXX</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>XX</td></tr>
<tr><td>2nd Parameter</td><td>1</td><td>↑</td><td>1</td><td colspan="9">D1[15:0]</td><td>XX</td></tr>
<tr><td>:</td><td>1</td><td>↑</td><td>1</td><td colspan="9">Dx[15:0]</td><td>XX</td></tr>
<tr><td>Nth Parameter</td><td>1</td><td>↑</td><td>1</td><td colspan="9">Dn[15:0]</td><td>XX</td></tr>
<tr><td>Description</td><td colspan="13">This command is used to transfer data from frame memory to MCU, if there is wanted to continue memory read after “Memory Read (2Eh)” command.
This command makes no change to the other driver status.
When this command is accepted, the column register and the page register are not reset to the Start Column/Start Page positions as it has been done on “Memory Read (2Eh)” command.
Then D[15:0] is read back from the frame memory and the column register and the page register incremented as table below:
Column and Page Counter Control.
<table>
<tr><th>Condition</th><th>Column counter</th><th>Page Counter</th></tr>
<tr><td>When RAMWR/RAMRD command is accepted</td><td>Return to “Start Column”</td><td>Return to “Start Page”</td></tr>
<tr><td>Complete Pixel Read/Write action</td><td>Increment by 1</td><td>No change</td></tr>
<tr><td>The Column counter value is large than “End Column”</td><td>Return to “Start Column”</td><td>Increment by 1</td></tr>
<tr><td>The Page counter value is large than “End Page”</td><td>Return to “Start Column”</td><td>Return to “Start Page”</td></tr>
</table>
Frame Read can be stopped by sending any other command.
X = can be ‘0’ or ‘1’</td></tr>
<tr><td>Restriction</td><td colspan="13">There is no restriction on length of parameters.
No access in the frame memory in Sleep In mode.</td></tr>
<tr><td>Register Availability</td><td colspan="13">
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td colspan="13">
<table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td>Contents of memory is set randomly</td></tr>
<tr><td>SW Reset</td><td>Contents of memory is set randomly</td></tr>
<tr><td>HW Reset</td><td>Contents of memory is set randomly</td></tr>
</table>
</td></tr>
</table>

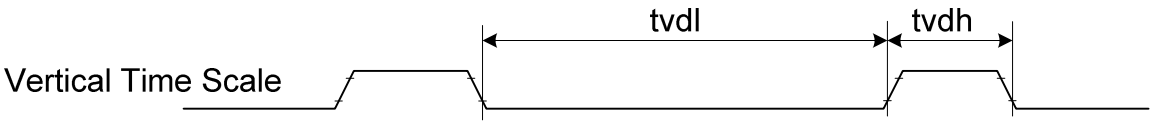
Flow Chart	

8.2.35. Write Tear Scan Line (44h)

44h	TESLWR (Write Tear Scan Line)												
	D/CX	RDX	WRX	D[15:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XXXXXXXX	0	1	0	0	0	1	0	0	44h
1st Parameter	1	1	↑	XXXXXXXX	N[15:8]								XX
2nd Parameter	1	1	↑	XXXXXXXX	N[7:0]								XX

Description

This command turns on the display Tearing Effect output signal on the TE signal line when the display reaches line N. The TE signal is not affected by changing Memory Access Control bit B4. The Tearing Effect Line On has one parameter that describes the Tearing Effect Output Line mode. The Tearing Effect Output line consists of V-Blanking information only.



Note that Set Tear Scan Line with N = 0 is equivalent to Tearing Effect Line ON with M = 0.

The Tearing Effect Output line shall be active low when ILI9486 is in Sleep mode.

Restriction

This command has no effect when Tearing Effect output is already ON.

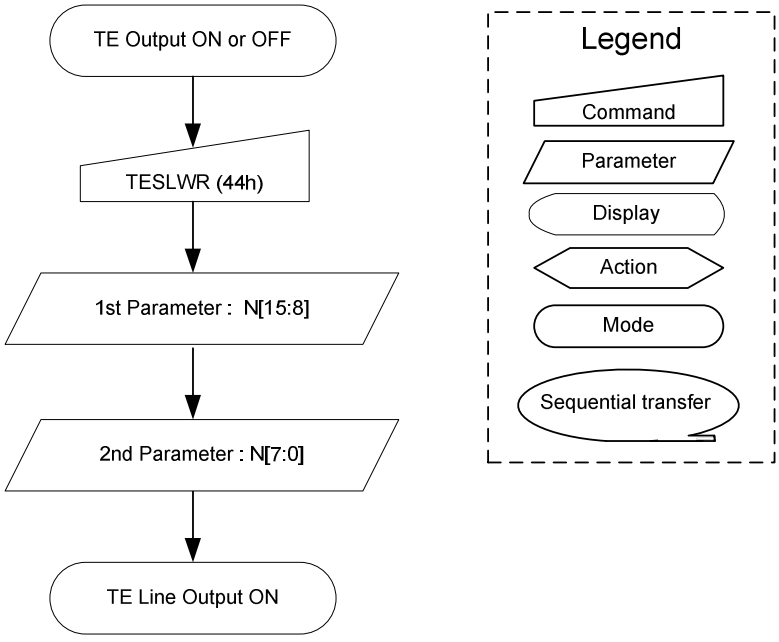
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h
SW Reset	No change
HW Reset	00h

Flow Chart



8.2.36. Read Scan Line (45h)

45h	TESLRD (Read Tear Scan Line)												
	D/CX	RDX	WRX	D[15:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XXXXXXXX	0	1	0	0	0	1	0	1	45h
1st Parameter	1	↑	1	XXXXXXXX	X	X	X	X	X	X	X	X	XX
2nd Parameter	1	↑	1	XXXXXXXX	N[15:8]								XX
3rd Parameter	1	↑	1	XXXXXXXX	N[7:0]								XX
Description	The display returns the current scan line, N, used to update the display device. The total number of scan lines on a display device is defined as VSYNC + VBP + VACT + VFP. The first scan line is defined as the first line of V-Sync and is denoted as Line 0. When in Sleep Mode, the value returned by Read Scan Line command is undefined.												
Restriction	None												

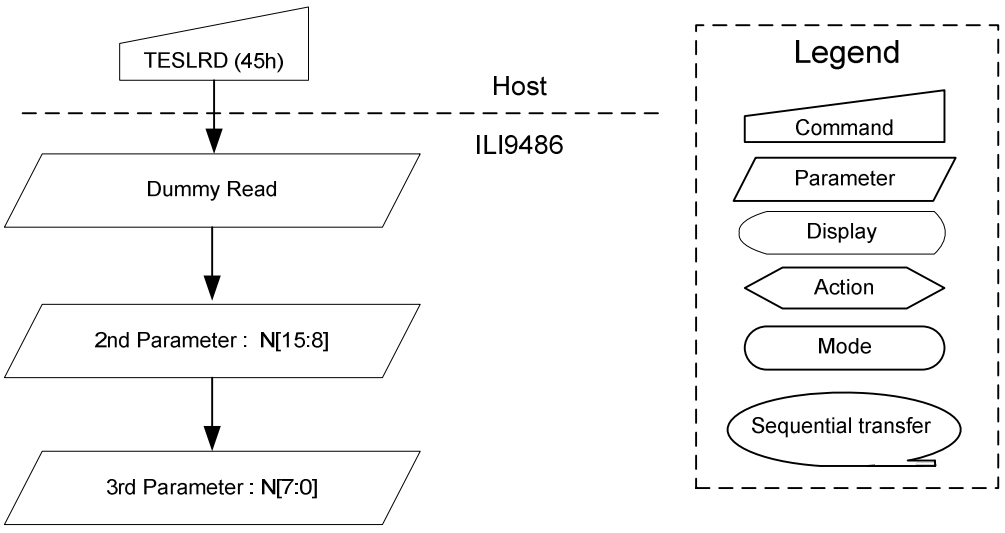
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

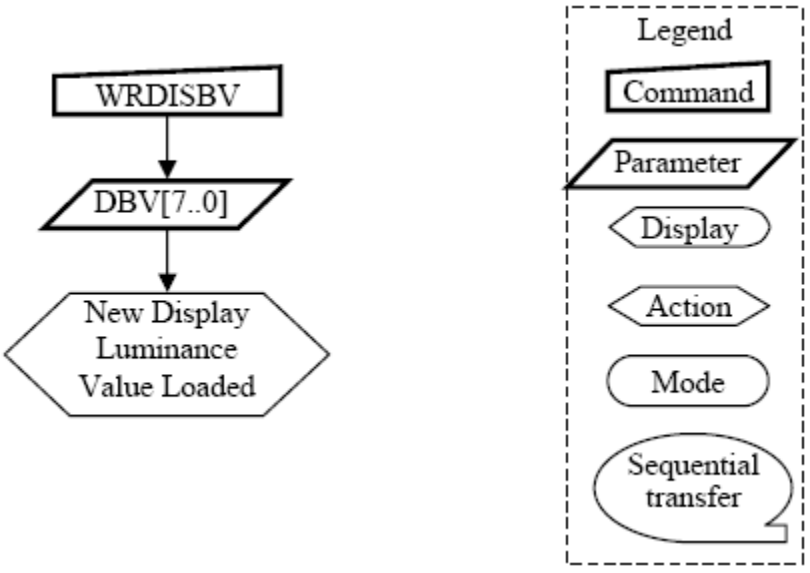
Default

Status	Default Value
Power On Sequence	00h
SW Reset	No change
HW Reset	00h

Flow Chart



8.2.37. Write Display Brightness Value (51h)

51h	WRDISBV (Write Display Brightness)												
	D/CX	RDX	WRX	D[15:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XXXXXXXX	0	1	0	1	0	0	0	1	51h
1st Parameter	1	1	↑	XXXXXXXX	DBV[7:0]								XX
Description	This command is used to adjust the brightness value of the display. **DBV[7:0]**: 8 bit, for display brightness of manual brightness setting and CABC in ILI9486. There is a PWM output signal, PWM_OUT pin, to control the LED driver IC in order to control display brightness. In principle relationship is that 00h value means the lowest brightness and FFh value means the highest brightness.												
Restriction													
Register Availability	Status / Availability Normal Mode ON, Idle Mode OFF, Sleep OUT: Yes Normal Mode ON, Idle Mode ON, Sleep OUT: Yes Partial Mode ON, Idle Mode OFF, Sleep OUT: Yes Partial Mode ON, Idle Mode ON, Sleep OUT: Yes Sleep IN: Yes												
Default	Status / Default Value Power ON Sequence: 00h H/W Reset: 00h												
Flow Chart													

8.2.38. Read Display Brightness Value (52h)

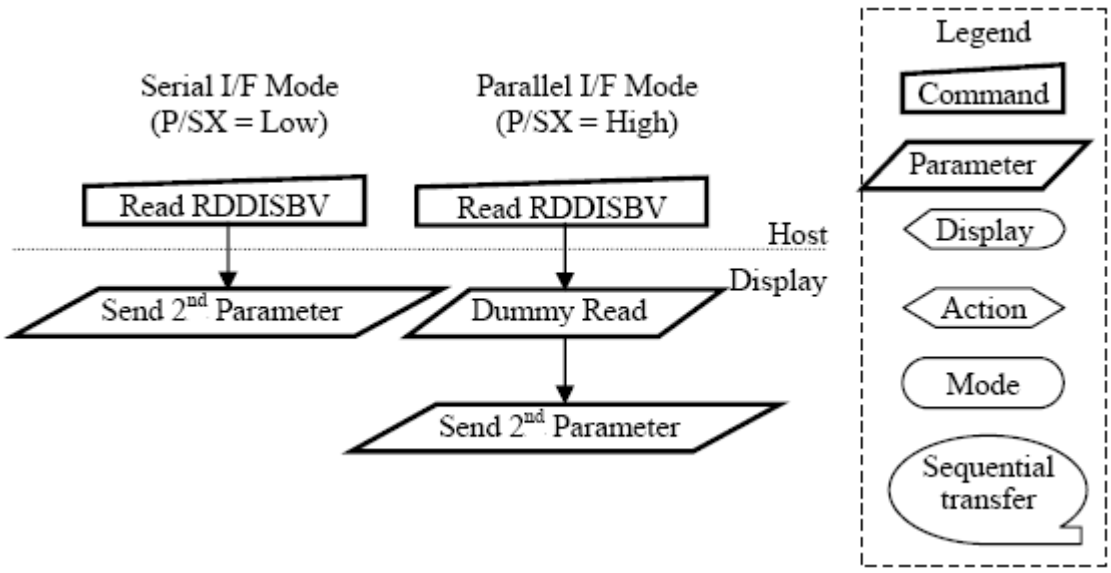
52h	RDDISBV (Read Display Brightness Value)												
	D/CX	RDX	WRX	D[15:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XXXXXXXX	0	1	0	1	0	0	1	0	52h
1st Parameter	1	↑	1	XXXXXXXX	X	X	X	X	X	X	X	X	XX
2nd Parameter	1	↑	1	XXXXXXXX	DBV[7:0]								XX
Description	This command is used to return the brightness value of the display. DBV[7:0] is reset when display is in sleep-in mode. DBV[7:0] is '0' when bit BCTRL of "Write CTRL Display (53h)" command is '0'. DBV[7:0] is manual set brightness specified with "Write CTRL Display (53h)" command when BCTRL bit is '1'. When bit BCTRL of "Write CTRL Display (53h)" command is '1' and C1/C0 bit of "Write Content Adaptive Brightness Control (55h)" command are '0', DBV[7:0] output is the brightness value specified with " Write Display Brightness (51h)" command.												
Restriction	ILI9486 is sending 2nd parameter value on the data lines if the MCU wants to read more than one parameter (= more than 2 RDX cycle) on parallel MCU interface. Only 2nd parameter is sent on DSI (The 1st parameter is not sent).												

Register Availability

Status	Availability
Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes
Normal Mode ON, Idle Mode ON, Sleep OUT	Yes
Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes
Partial Mode ON, Idle Mode ON, Sleep OUT	Yes
Sleep IN	Yes

Default

Status	Default Value
Power ON Sequence	00h
H/W Reset	00h



8.2.39. Write CTRL Display Value (53h)

53h	WRCTRLD (Write Control Display)												
	D/CX	RDX	WRX	D[15:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XXXXXXXX	0	1	0	1	0	0	1	1	53h
1st Parameter	1	1	↑	XXXXXXXX	X	X	BCTRL	X	DD	BL	X	X	XX

Description

This command is used to control display brightness.

BCTRL: Brightness Control Block On/Off, This bit is always used to switch brightness for display.

BCTRL	Description
0	Brightness Control Block OFF (DBV[7:0]=00h)
1	Brightness Control Block ON (DBV[7:0] is active)

DD: Display Dimming Control. This function is only for manual brightness setting.

DD	Description
0	Display Dimming OFF
1	Display Dimming ON

BL: Backlight Control On/Off

BL	Description
0	Backlight Control OFF
1	Backlight Control ON

Dimming function is adapted to the brightness registers for display when bit BCTRL is changed at DD=1, e.g. BCTRL: 0 -> 1 or 1-> 0.

When BL bit change from “On” to “Off”, backlight is turned off without gradual dimming, even if dimming-on (DD=1) are selected.

X = Don’t care

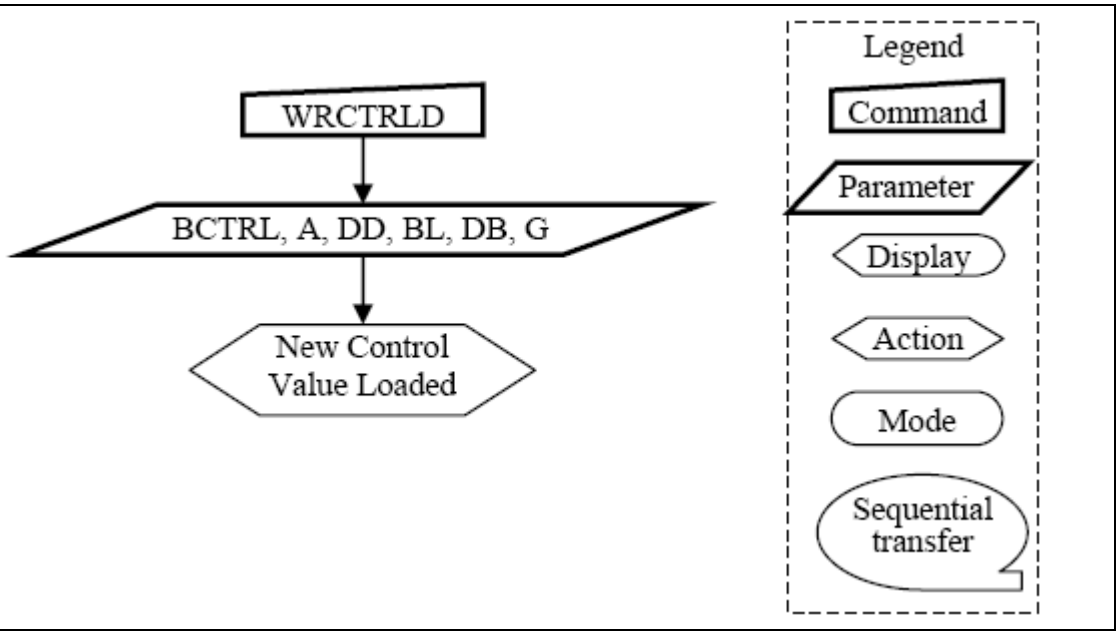
Restriction

Register Availability

Status	Availability
Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes
Normal Mode ON, Idle Mode ON, Sleep OUT	Yes
Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes
Partial Mode ON, Idle Mode ON, Sleep OUT	Yes
Sleep IN	Yes

Default

Status	Default Value
Power ON Sequence	00h
H/W Reset	00h

Flow Chart	

8.2.40. Read CTRL Display Value (54h)

54h	RDCTRLD (Read Control Display Value)												
	D/CX	RDX	WRX	D[15:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XXXXXXXX	0	1	0	1	0	1	0	0	54h
1st Parameter	1	↑	1	XXXXXXXX	X	X	X	X	X	X	X	X	XX
2nd Parameter	1	↑	1	XXXXXXXX	X	X	BCTRL	X	DD	BL	X	X	XX

Description

This command is used to control display brightness.

BCTRL: Brightness Control Block On/Off, This bit is always used to switch brightness for display.

BCTRL	Description
0	Brightness Control Block OFF (DBV[7:0]=00h)
1	Brightness Control Block ON (DBV[7:0] is active)

DD: Display Dimming Control. This function is only for manual brightness setting.

DD	Description
0	Display Dimming OFF
1	Display Dimming ON

BL: Backlight Control On/Off

BL	Description
0	Backlight Control OFF
1	Backlight Control ON

X = Don't care

Restriction

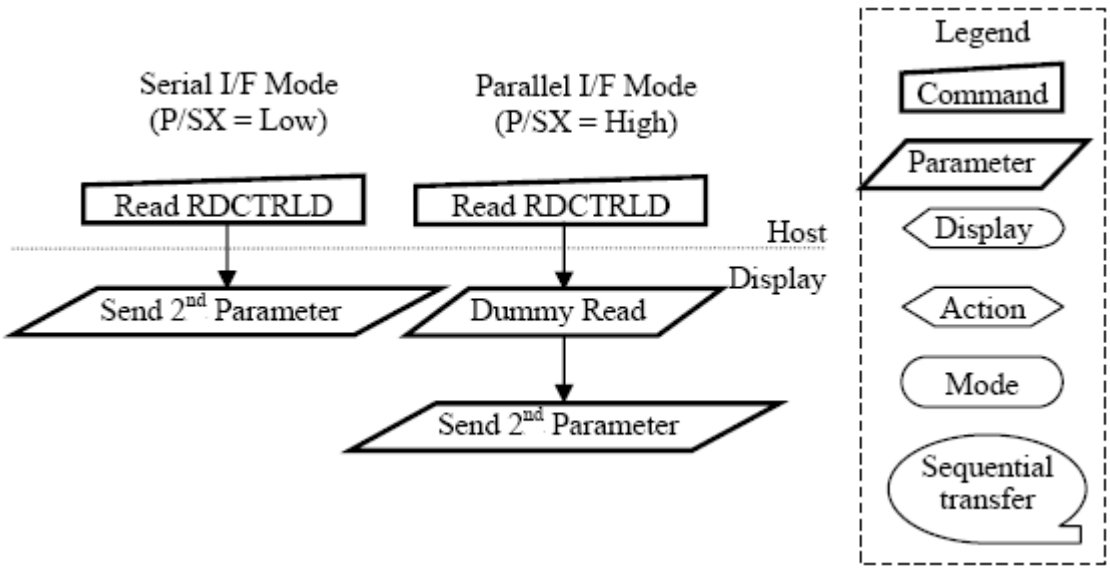
Register Availability

Status	Availability
Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes
Normal Mode ON, Idle Mode ON, Sleep OUT	Yes
Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes
Partial Mode ON, Idle Mode ON, Sleep OUT	Yes
Sleep IN	Yes

Default

Status	Default Value
Power ON Sequence	00h
H/W Reset	00h

Flow Chart



8.2.41. Write Content Adaptive Brightness Control Value (55h)

55h	WRCABC (Write Content Adaptive Brightness Control)												
	D/CX	RDX	WRX	D[15:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XXXXXXXX	0	1	0	1	0	1	0	1	55h
1st Parameter	1	1	↑	XXXXXXXX	X	X	X	X	X	X	C[1:0]		XX

Description

This command is used to set parameters for image content based adaptive brightness control functionality.

There is possible to use 4 different modes for content adaptive image functionality, which are defined on a table below.

C[1:0]		Description
0	0	CABC OFF
0	1	User Interface Image
1	0	Still Picture
1	1	Moving Image

X = Don't care

Restriction

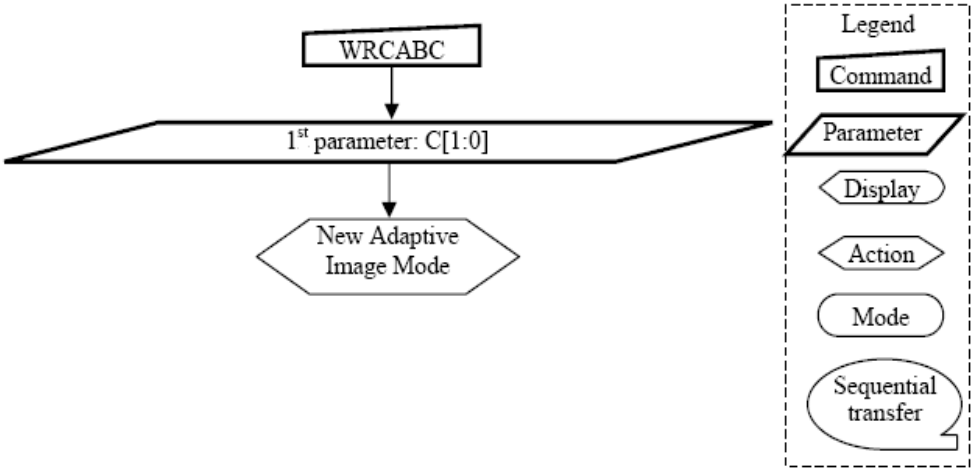
Register Availability

Status	Availability
Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes
Normal Mode ON, Idle Mode ON, Sleep OUT	Yes
Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes
Partial Mode ON, Idle Mode ON, Sleep OUT	Yes
Sleep IN	Yes

Default

Status	Default Value
Power ON Sequence	00h
H/W Reset	00h

Flow Chart



8.2.42. Read Content Adaptive Brightness Control Value (56h)

56h	RDCABC (Read Content Adaptive Brightness Control)												
	D/CX	RDX	WRX	D[15:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XXXXXXXX	0	1	0	1	0	1	1	0	56h
1st Parameter	1	↑	1	XXXXXXXX	X	X	X	X	X	X	X	X	XX
2nd Parameter	1	↑	1	XXXXXXXX	X	X	X	X	X	X	C[1:0]		XX

Description

This command is used to read the settings for image content based adaptive brightness control functionality. There is possible to use 4 different modes for content adaptive image functionality which are defined on the table below.

C[1:0]		Description
0	0	CABC OFF
0	1	User Interface Image
1	0	Still Picture
1	1	Moving Image

X = Don't care

Restriction

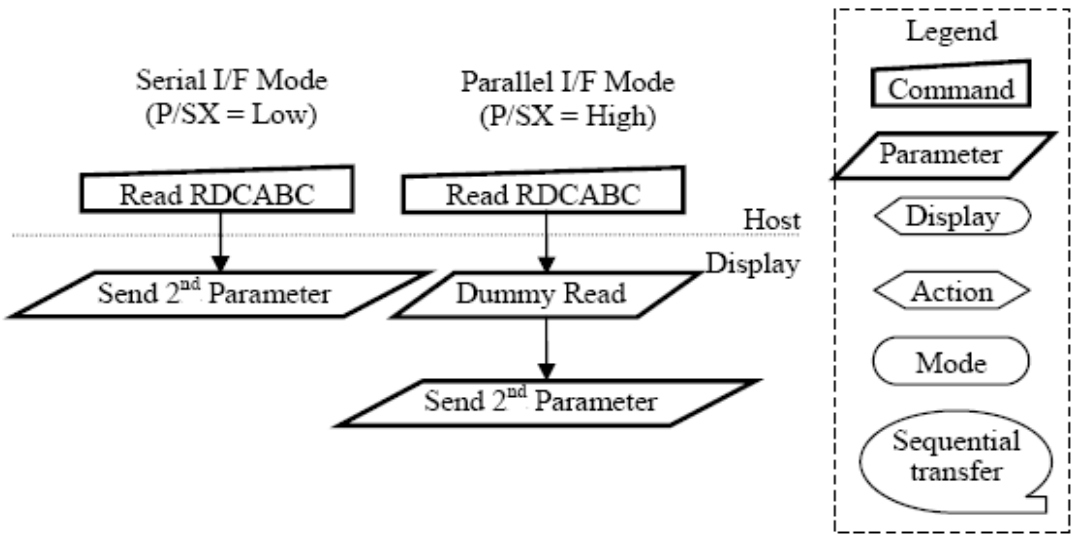
Register Availability

Status	Availability
Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes
Normal Mode ON, Idle Mode ON, Sleep OUT	Yes
Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes
Partial Mode ON, Idle Mode ON, Sleep OUT	Yes
Sleep IN	Yes

Default

Status	Default Value
Power ON Sequence	00h
H/W Reset	00h

Flow Chart



8.2.43. Write CABC Minimum Brightness (5Eh)

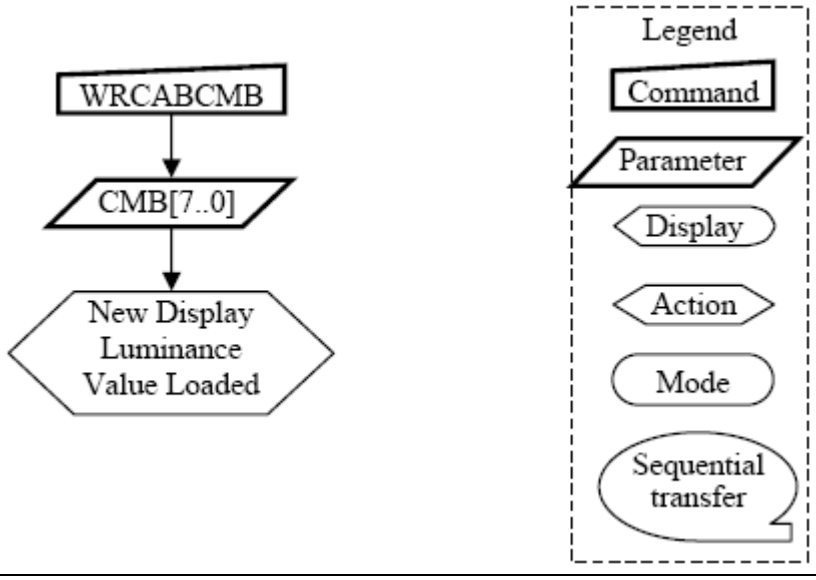
5Eh	WRCABCMB (Write CABC Minimum Brightness)												
	D/CX	RDX	WRX	D[15:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XXXXXXXX	0	1	0	1	1	1	1	0	5Eh
1st Parameter	1	1	↑	XXXXXXXX	CMB[7:0]								XX
Description	This command is used to set the minimum brightness value of the display for CABC function. **CMB[7:**0]: CABC minimum brightness control, this parameter is used to avoid too much brightness reduction. When CABC is active, CABC can not reduce the display brightness to less than CABC minimum brightness setting. Image processing function is worked as normal, even if the brightness can not be changed. This function does not affect to the other function, manual brightness setting. Manual brightness can be set the display brightness to less than CABC minimum brightness. Smooth transition and dimming function can be worked as normal. When display brightness is turned off (BCTRL=0 of "Write CTRL Display (53h)"), CABC minimum brightness setting is ignored. In principle relationship is that 00h value means the lowest brightness for CABC and FFh value means the highest brightness for CABC.												
Restriction													
Register Availability													

Status	Availability
Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes
Normal Mode ON, Idle Mode ON, Sleep OUT	Yes
Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes
Partial Mode ON, Idle Mode ON, Sleep OUT	Yes
Sleep IN	Yes

Default

Status	Default Value
Power ON Sequence	00h
H/W Reset	00h

Flow Chart



8.2.44. Read CABC Minimum Brightness (5Fh)

5Fh	RDCABCMB (Read CABC Minimum Brightness)												
	D/CX	RDX	WRX	D[15:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XXXXXXXX	0	1	0	1	1	1	1	1	5Fh
1st Parameter	1	↑	1	XXXXXXXX	X	X	X	X	X	X	X	X	XX
2nd Parameter	1	↑	1	XXXXXXXX	CMB[7:0]								XX

Description

This command returns the minimum brightness value of CABC function.

In principle the relationship is that 00h value means the lowest brightness and FFh value means the highest brightness.

CMB[7:0] is CABC minimum brightness specified with "Write CABC minimum brightness (5Eh)" command.

Restriction

ILI9486 is sending 2nd parameter value on the data lines if the MCU wants to read more than one parameter (= more than 2 RDX cycle) on parallel MCU interface.

Only 2nd parameter is sent on DSI (The 1st parameter is not sent).

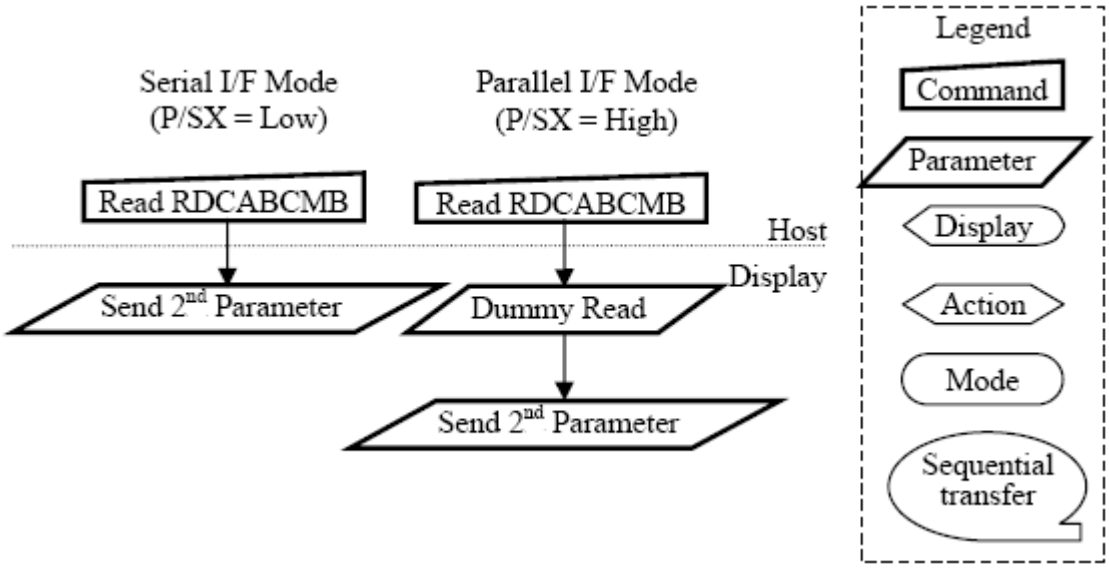
Register Availability

Status	Availability
Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes
Normal Mode ON, Idle Mode ON, Sleep OUT	Yes
Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes
Partial Mode ON, Idle Mode ON, Sleep OUT	Yes
Sleep IN	Yes

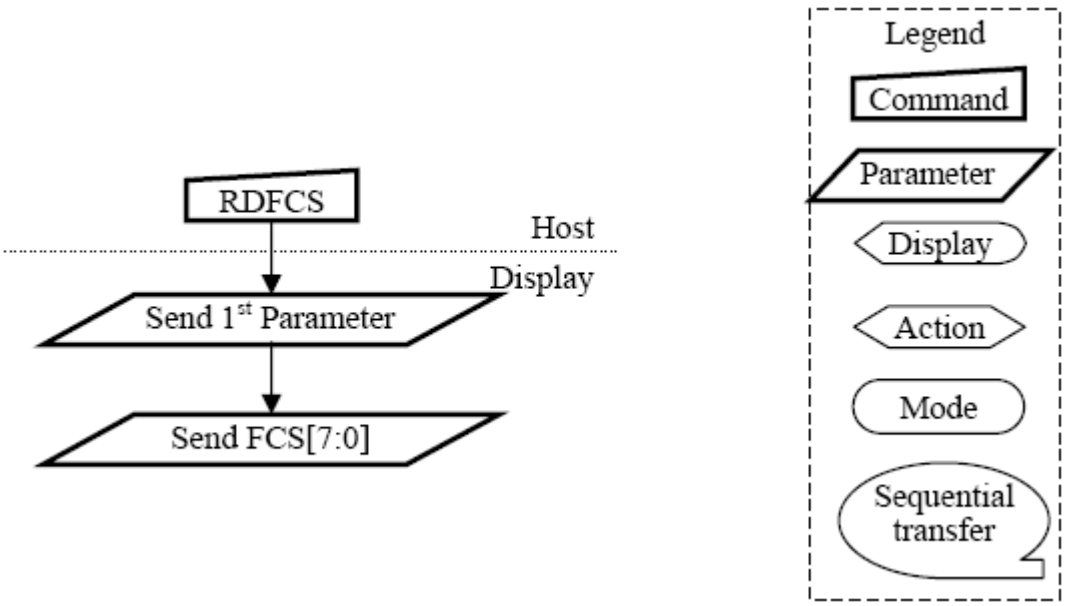
Default

Status	Default Value
Power ON Sequence	00h
H/W Reset	00h

Flow Chart



8.2.45. Read First Checksum (AAh)

AAh	RDFCS (Read First Checksum)												
	D/CX	RDX	WRX	D[15:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XXXXXXXX	1	0	1	0	1	0	1	0	AAh
1st Parameter	1	↑	1	XXXXXXXX	X	X	X	X	X	X	X	X	XX
2nd Parameter	1	↑	1	XXXXXXXX	FCS[7:0]								XX
Description	This command returns the first checksum what has been calculated from User's area registers and the frame memory after the write access to those registers and/or frame memory has been done. X = can be '0' or '1'												
Restriction	It will be necessary to wait 150ms after there is the last write access on User area registers before there can read this checksum value. ILI9486 is sending 2nd parameter value on the data lines if the MCU wants to read more than one parameter (= more than 2 RDX cycle) on parallel MCU interface. Only 2nd parameter is sent on DSI (The 1st parameter is not sent).												
Register Availability	Status / Availability Normal Mode ON, Idle Mode OFF, Sleep OUT: Yes Normal Mode ON, Idle Mode ON, Sleep OUT: Yes Partial Mode ON, Idle Mode OFF, Sleep OUT: Yes Partial Mode ON, Idle Mode ON, Sleep OUT: Yes Sleep IN: Yes												
Default	Status / Default Value Power ON Sequence: 00h H/W Reset: 00h												
Flow Chart													

8.2.46. Read Continue Checksum (AFh)

AFh	RDCFCS (Read Continue Checksum)												
	D/CX	RDX	WRX	D[15:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XXXXXXXX	1	0	1	0	1	1	1	1	AFh
1st Parameter	1	↑	1	XXXXXXXX	X	X	X	X	X	X	X	X	XX
2nd Parameter	1	↑	1	XXXXXXXX	CCS[7:0]								XX
Description	This command returns the continue checksum what has been calculated continuously after the first checksum has calculated from User's area registers and the frame memory after the write access to those registers and/or frame memory has been done. X = can be '0' or '1'												
Restriction	It will be necessary to wait 300ms after there is the last write access on User area registers before there can read this checksum value in the first time. ILI9486 is sending 2nd parameter value on the data lines if the MCU wants to read more than one parameter (= more than 2 RDX cycle) on parallel MCU interface. Only 2nd parameter is sent on DSI (The 1st parameter is not sent).												

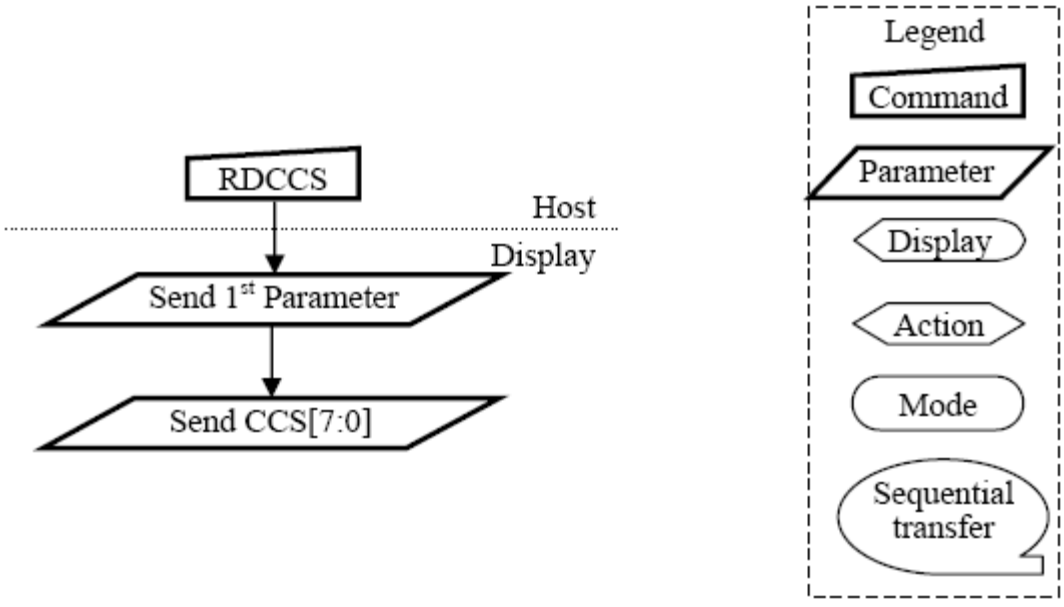
Register Availability

Status	Availability
Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes
Normal Mode ON, Idle Mode ON, Sleep OUT	Yes
Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes
Partial Mode ON, Idle Mode ON, Sleep OUT	Yes
Sleep IN	Yes

Default

Status	Default Value
Power ON Sequence	00h
H/W Reset	00h

Flow Chart



8.2.47. Read ID1 (DAh)

DAh	RDID1 (Read ID1)												
	D/CX	RDX	WRX	D[15:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XXXXXXXX	1	1	0	1	1	0	1	0	DAh
1st parameter	1	↑	1	XXXXXXXX	X	X	X	X	X	X	X	X	XX
2nd arameter	1	↑	1	XXXXXXXX	ID1[7:0]								XX
Description	This read byte identifies the LCD module's manufacturer ID and it is specified by User The 1st parameter is dummy data. The 2nd parameter is LCD module's manufacturer ID. X = Don't care												
Restriction	ILI9486 is sending 2nd parameter value on the data lines if the MCU wants to read more than one parameter (= more than 2 RDX cycle) on parallel MCU interface. Only 2nd parameter is sent on DSI (The 1st parameter is not sent).												

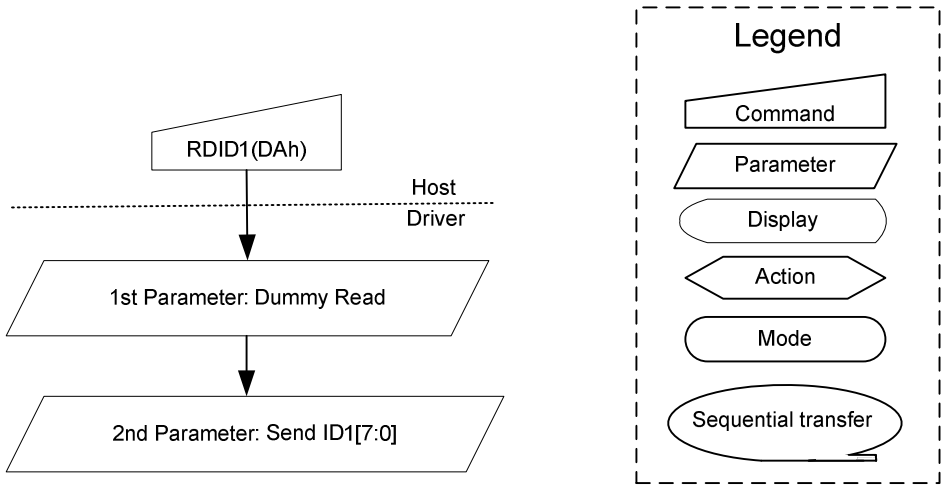
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	XXh
HW Reset	XXh

Flow Chart



8.2.48. Read ID2 (DBh)

DBh	RDID2 (Read ID2)												
	D/CX	RDX	WRX	D[15:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XXXXXXXX	1	1	0	1	1	0	1	1	DBh
1st parameter	1	↑	1	XXXXXXXX	X	X	X	X	X	X	X	X	XX
2nd arameter	1	↑	1	XXXXXXXX	1	ID2[6:0]							XX
Description	This read byte is used to track the LCD module/driver version. It is defined by display supplier (with User's agreement) and changes each time a revision is made to the display, material or construction specifications. The 1st parameter is dummy data. The 2nd parameter is LCD module/driver version ID and the ID parameter range is from 80h to FFh. The ID2 can be programmed by OTP function. X = Don't care												
Restriction	ILI9486 is sending 2nd parameter value on the data lines if the MCU wants to read more than one parameter (= more than 2 RDX cycle) on parallel MCU interface. Only 2nd parameter is sent on DSI (The 1st parameter is not sent).												

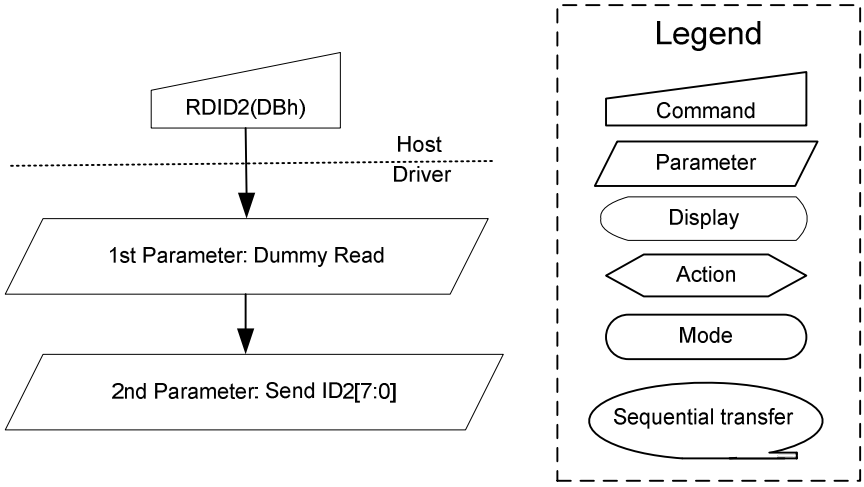
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value (Before OTP program)	Default Value (After OTP program)
Power On Sequence	80h	OTP value
SW Reset	80h	OTP value
HW Reset	80h	OTP value

Flow Chart



8.2.49. Read ID3 (DCh)

DCh	RDID3 (Read ID3)												
	D/CX	RDX	WRX	D[15:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XXXXXXXX	1	1	0	1	1	1	0	0	DCh
1st parameter	1	↑	1	XXXXXXXX	X	X	X	X	X	X	X	X	XX
2nd parameter	1	↑	1	XXXXXXXX	ID3[7:0]								XX
Description	This read byte identifies the LCD module/driver and It is specified by User. The 1st parameter is dummy data. The 2nd parameter is LCD module/driver ID. The ID3 can be programmed by OTP function. X = Don't care												
Restriction	ILI9486 is sending 2nd parameter value on the data lines if the MCU wants to read more than one parameter (= more than 2 RDX cycle) on parallel MCU interface. Only 2nd parameter is sent on DSI (The 1st parameter is not sent).												

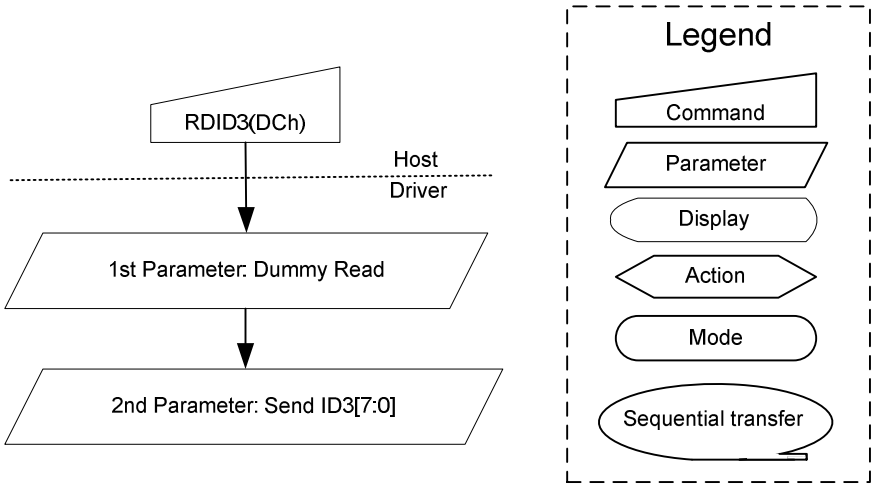
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

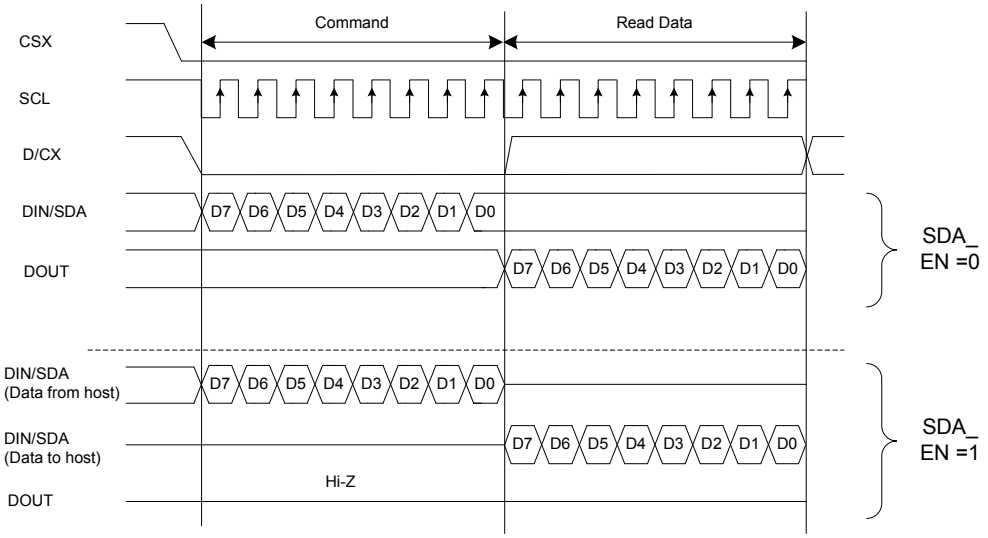
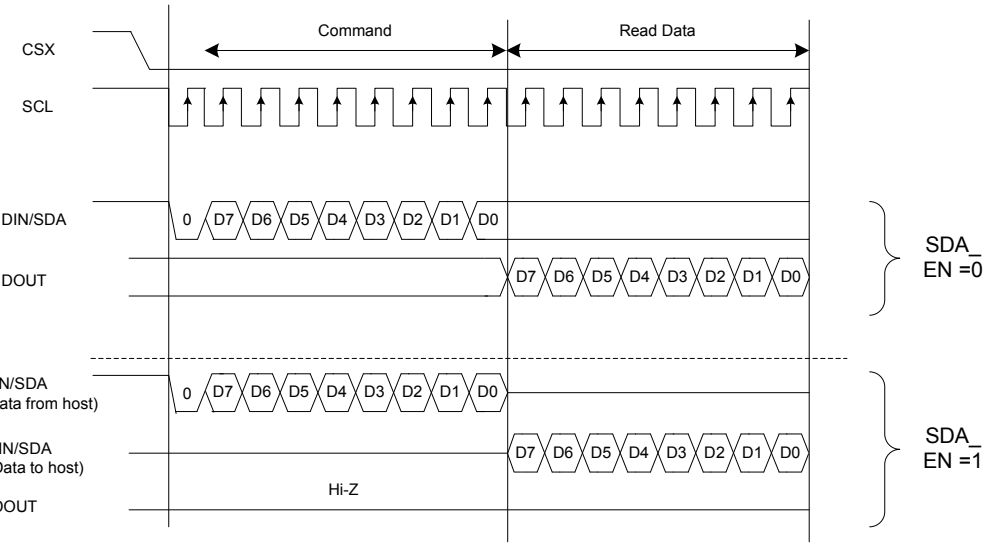
Default

Status	Default Value (Before OTP program)	Default Value (After OTP program)
Power On Sequence	00h	OTP value
SW Reset	00h	OTP value
HW Reset	00h	OTP value

Flow Chart



8.2.50. Interface Mode Control (B0h)

B0h	IFMODE (Interface Mode Control)												
	D/CX	RDX	WRX	D[15:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XXXXXXXX	1	0	1	1	0	0	0	0	B0h
1st Parameter	1	1	↑	XXXXXXXX	SDA_EN	0	0	0	VSPL	HSPL	DPL	EPL	XX
Description	Sets the operation status of the display interface. The setting becomes effective as soon as the command is received. **EPL**: DE polarity ("0"= High enable for RGB interface, "1"=Low enable for RGB interface) **DPL**: PCLK polarity set ("0"=data fetched at the rising time, "1"=data fetched at the falling time) **HSPL**: HSYNC polarity ("0"=Low level sync clock, "1"=High level sync clock) **VSPL**: VSYNC polarity ("0"= Low level sync clock, "1"= High level sync clock) **SDA_EN:** 3/4 wire serial interface selection SDA_EN = "0", DIN and DOUT pins are used for 3/4 wire serial interface. SDA_EN = "1", DIN/SDA pin is used for 3/4 wire serial interface and DOUT pin is not used.  												
Restriction													

Register Availability

Status	Availability
Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes
Normal Mode ON, Idle Mode ON, Sleep OUT	Yes
Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes
Partial Mode ON, Idle Mode ON, Sleep OUT	Yes
Sleep IN	Yes

Default

Status	Default Value				
	SDA_EN	EPL	DPL	HSPL	VSPL
Power ON Sequence	0b	0b	0b	0b	0b
H/W Reset	`0b	0b	0b	0b	0b

8.2.51. Frame Rate Control (In Normal Mode/Full Colors) (B1h)

B1h	FRMCTR1 (Frame Rate Control (In Normal Mode / Full colors))												
	D/CX	RDX	WRX	D[15:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XXXXXXXX	1	0	1	1	0	0	0	1	B1h
1st Parameter	1	1	↑	XXXXXXXX	FRS[3:0]				0	0	DIVA[1:0]		XX
2nd parameter	1	1	↑	XXXXXXXX	0	0	0	RTNA[4:0]					XX

Description

FRS[3:0]: Sets the frame frequency of full color normal mode.

FRS[3:0]				Frame rate(Hz)
0	0	0	0	28
0	0	0	1	30
0	0	1	0	32
0	0	1	1	34
0	1	0	0	36
0	1	0	1	39
0	1	1	0	42
0	1	1	1	46
1	0	0	0	50
1	0	0	1	56
1	0	1	0	62
1	0	1	1	70
1	1	0	0	81
1	1	0	1	96
1	1	1	0	117
1	1	1	1	117

DIVA [1:0] : division ratio for internal clocks when Normal mode.

DIVA[1:0]		Division Ratio
0	0	fosc
0	1	fosc / 2
1	0	fosc / 4
1	1	fosc / 8

RTNA [4:0] : RTNA[4:0] is used to set 1H (line) period of Normal mode at CPU interface.

RTNA[4:0]					Clock per Line
0	0	0	0	0	Setting prohibited
0	0	0	0	1	Setting prohibited
0	0	0	1	0	Setting prohibited
0	0	0	1	1	Setting prohibited
0	0	1	0	0	Setting prohibited
0	0	1	0	1	Setting prohibited
0	0	1	1	0	Setting prohibited
0	0	1	1	1	Setting prohibited
0	1	0	0	0	Setting prohibited
0	1	0	0	1	Setting prohibited

RTNA[4:0]					Clock per Line
0	1	0	1	1	Setting prohibited
0	1	1	0	0	Setting prohibited
0	1	1	0	1	Setting prohibited
0	1	1	1	0	Setting prohibited
0	1	1	1	1	Setting prohibited
1	0	0	0	0	16 clocks
1	0	0	0	1	17 clocks
1	0	0	1	0	18 clocks
1	0	0	1	1	19 clocks
1	0	1	0	0	20 clocks

RTNA[4:0]					Clock per Line
1	0	1	1	0	22 clocks
1	0	1	1	1	23 clocks
1	0	0	0	0	24 clocks
1	0	0	0	1	25 clocks
1	0	0	1	0	26 clocks
1	0	1	1	1	27 clocks
1	1	0	0	0	28 clocks
1	1	0	0	1	29 clocks
1	1	0	1	0	30 clocks
1	1	1	1	1	31 clocks

<table>
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<tr><td>Normal Mode ON, Idle Mode ON, Sleep OUT</td><td>Yes</td></tr>
<tr><td>Partial Mode ON, Idle Mode OFF, Sleep OUT</td><td>Yes</td></tr>
<tr><td>Partial Mode ON, Idle Mode ON, Sleep OUT</td><td>Yes</td></tr>
<tr><td>Sleep IN</td><td>Yes</td></tr>
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<tr><td>Default</td><td>
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<tr><th>FRS [3:0]</th><th>DIVA[1:0]</th><th>RTNA[4:0]</th></tr>
<tr><td>Power ON Sequence</td><td>4’b1011</td><td>2’b00</td><td>5’b10001</td></tr>
<tr><td>H/W Reset</td><td>4’b1011</td><td>2’b00</td><td>5’b10001</td></tr>
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8.2.52. Frame Rate Control (In Idle Mode/8 colors) (B2h)

B2h	FRMCTR2 (Frame Rate Control (In Idle Mode / 8 colors))												
	D/CX	RDX	WRX	D[15:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XXXXXXXX	1	0	1	1	0	0	1	0	B2h
1st Parameter	1	1	↑	XXXXXXXX	0	0	0	0	0	0	DIVB[1:0]		XX
2nd parameter	1	1	↑	XXXXXXXX	0	0	0	RTNB[4:0]					XX

Description

Sets the division ratio for internal clocks of Idle mode at CPU interface.

DIVB [1:0] : division ratio for internal clocks when Idle mode.

DIVB[1:0]		Division Ratio
0	0	fosc
0	1	fosc / 2
1	0	fosc / 4
1	1	fosc / 8

RTNB [4:0] : RTNB[4:0] is used to set 1H (line) period of Idle mode at CPU interface.

RTNB[4:0]					Clock per Line
0	0	0	0	0	Setting prohibited
0	0	0	0	1	Setting prohibited
0	0	0	1	0	Setting prohibited
0	0	0	1	1	Setting prohibited
0	0	1	0	0	Setting prohibited
0	0	1	0	1	Setting prohibited
0	0	1	1	0	Setting prohibited
0	0	1	1	1	Setting prohibited
0	1	0	0	0	Setting prohibited
0	1	0	0	1	Setting prohibited
0	1	0	1	0	Setting prohibited

RTNB[4:0]					Clock per Line
0	1	0	1	1	Setting prohibited
0	1	1	0	0	Setting prohibited
0	1	1	0	1	Setting prohibited
0	1	1	1	0	Setting prohibited
0	1	1	1	1	Setting prohibited
1	0	0	0	0	16 clocks
1	0	0	0	1	17 clocks
1	0	0	1	0	18 clocks
1	0	0	1	1	19 clocks
1	0	1	0	0	20 clocks
1	0	1	0	1	21 clocks

RTNB[4:0]					Clock per Line
1	0	1	1	0	22 clocks
1	0	1	1	1	23 clocks
1	0	0	0	0	24 clocks
1	0	0	0	1	25 clocks
1	0	0	1	0	26 clocks
1	0	1	1	1	27 clocks
1	1	0	0	0	28 clocks
1	1	0	0	1	29 clocks
1	1	0	1	0	30 clocks
1	1	1	1	1	31 clocks

Restriction

Register Availability

Status	Availability
Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes
Normal Mode ON, Idle Mode ON, Sleep OUT	Yes
Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes
Partial Mode ON, Idle Mode ON, Sleep OUT	Yes
Sleep IN	Yes

Default

Status	Default Value	
	DIVB[1:0]	RTNB[4:0]
Power ON Sequence	2'b00	5'b10001
H/W Reset	2'b00	5'b10001

8.2.53. Frame Rate control (In Partial Mode/Full Colors) (B3h)

B3h	FRMCTR3 (Frame Rate Control (In Partial Mode / Full colors))												
	D/CX	RDX	WRX	D[15:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XXXXXXXX	1	0	1	1	0	0	1	1	B3h
1st Parameter	1	1	↑	XXXXXXXX	0	0	0	0	0	0	DIVC[1:0]		XX
2nd parameter	1	1	↑	XXXXXXXX	0	0	0	RTNC[4:0]					XX

Description

Sets the division ratio for internal clocks of Partial mode (Idle mode off) at CPU interface.

DIVC [1:0] : division ratio for internal clocks when Partial mode.

DIVC[1:0]		Division Ratio
0	0	fosc
0	1	fosc / 2
1	0	fosc / 4
1	1	fosc / 8

RTNC [4:0] : RTNC[4:0] is used to set 1H (line) period of Partial mode at CPU interface.

RTNC[4:0]					Clock per Line
0	0	0	0	0	Setting prohibited
0	0	0	0	1	Setting prohibited
0	0	0	1	0	Setting prohibited
0	0	0	1	1	Setting prohibited
0	0	1	0	0	Setting prohibited
0	0	1	0	1	Setting prohibited
0	0	1	1	0	Setting prohibited
0	0	1	1	1	Setting prohibited
0	1	0	0	0	Setting prohibited
0	1	0	0	1	Setting prohibited
0	1	0	1	0	Setting prohibited

RTNC[4:0]					Clock per Line
0	1	0	1	1	Setting prohibited
0	1	1	0	0	Setting prohibited
0	1	1	0	1	Setting prohibited
0	1	1	1	0	Setting prohibited
0	1	1	1	1	Setting prohibited
1	0	0	0	0	16 clocks
1	0	0	0	1	17 clocks
1	0	0	1	0	18 clocks
1	0	0	1	1	19 clocks
1	0	1	0	0	20 clocks
1	0	1	0	1	21 clocks

RTNC[4:0]					Clock per Line
1	0	1	1	0	22 clocks
1	0	1	1	1	23 clocks
1	0	0	0	0	24 clocks
1	0	0	0	1	25 clocks
1	0	0	1	0	26 clocks
1	0	1	1	1	27 clocks
1	1	0	0	0	28 clocks
1	1	0	0	1	29 clocks
1	1	0	1	0	30 clocks
1	1	1	1	1	31 clocks

Restriction

Register Availability

Status	Availability
Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes
Normal Mode ON, Idle Mode ON, Sleep OUT	Yes
Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes
Partial Mode ON, Idle Mode ON, Sleep OUT	Yes
Sleep IN	Yes

Default

Status	Default Value	
	DIVC[1:0]	RTNC[4:0]
Power ON Sequence	2'b00	5'b10001
H/W Reset	2'b00	5'b10001

8.2.54. Display Inversion Control (B4h)

B4h	INVTR (Display Inversion Control)												
	D/CX	RDX	WRX	D[15:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XXXXXXXX	1	0	1	1	0	1	0	0	B4h
1st Parameter	1	1	↑	XXXXXXXX	0	0	0	ZINV	0	0	DINV[1:0]		XX

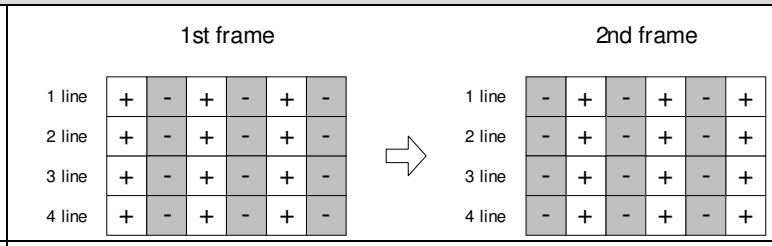
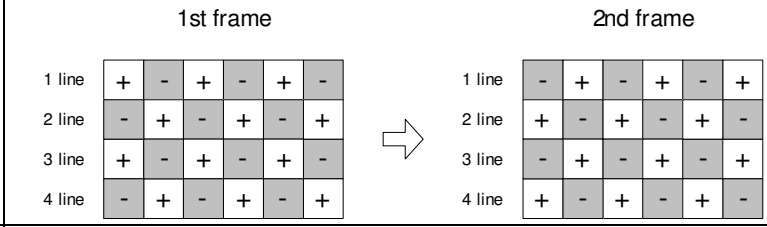
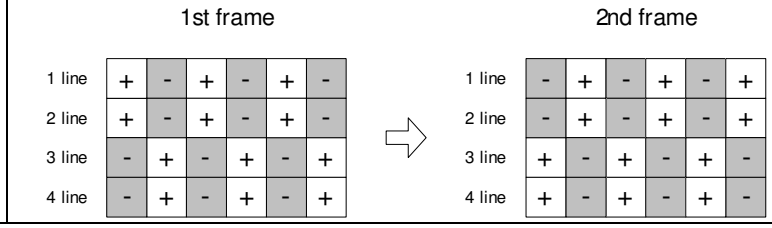
Description

ZINV : Set Z-inversion mode

0 : Disable Z-inversion

1 : Enable Z-inversion mode

DINV[1:0] : Set the inversion mode

DINV [1:0]	Dot inversion mode	
2'b00	Column inversion	
2'b01	1-dot inversion	
2'b10	2-dot inversion	
2'b11	Setting prohibited	

Restriction

Register Availability

Status	Availability
Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes
Normal Mode ON, Idle Mode ON, Sleep OUT	Yes
Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes
Partial Mode ON, Idle Mode ON, Sleep OUT	Yes
Sleep IN	Yes

Default

Status	Default Value	
	ZINV	DINV[1:0]
Power ON Sequence	1'b0	2'b00
H/W Reset	1'b0	2'b00

8.2.55. Blanking Porch Control (B5h)

B5h	PRCTR (Blanking Porch)												
	D/CX	RDX	WRX	D[15:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XXXXXXXX	1	0	1	1	0	1	0	1	B5h
1st parameter	1	1	↑	XXXXXXXX	VFP[7:0]								XX
2nd parameter	1	1	↑	XXXXXXXX	VBP[7:0]								XX
3nd parameter	1	1	↑	XXXXXXXX	0	0	0	HFP[4:0]					XX
4nd parameter	1	1	↑	XXXXXXXX	HBP[7:0]								XX

Description

VFP [7:0] / **VBP [7:0]:** The FP [7:0] and BP [7:0] bits specify the line number of vertical front and back porch period respectively.

FP[7:0]	Number of lines of front porch
00000000	Setting prohibited
00000001	Setting prohibited
00000010	2
00000011	3
:	:
11111100	252
11111101	253
11111110	254
11111111	255

BP[7:0]	Number of lines of back porch
00000000	Setting prohibited
00000001	Setting prohibited
00000010	2
00000011	3
:	:
11111100	252
11111101	253
11111110	254
11111111	254

HFP [4:0]: The HFP [4:0] bits specify the dotclk number of horizontal front porch period.

HFP[4:0]	Number of dotclk of front porch
00000	Setting prohibited
00001	Setting prohibited
00010	2
00011	3
:	:
11100	28
11101	29
11110	30
11111	31

HBP [7:0]: The HBP[7:0] bits specify the dotclk number of horizontal back porch period.

HBP[7:0]	Number of dotclk of front porch
00000000	Setting prohibited
00000001	Setting prohibited
00000010	2
00000011	3
:	:
11111100	252
11111101	253
11111110	254
11111111	255

Restriction

Register Availability

Status	Availability
Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes
Normal Mode ON, Idle Mode ON, Sleep OUT	Yes
Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes
Partial Mode ON, Idle Mode ON, Sleep OUT	Yes
Sleep IN	Yes

Default

Status	Default Value			
	VFP[7:0]	VBP[7:0]	HFP[4:0]	HBP[7:0]
Power ON Sequence	8'b00000010	8'b00000010	8'b00001010	8'b00000100
H/W Reset	8'b00000010	8'b00000010	8'b00001010	8'b00000100

8.2.56. Display Function Control (B6h)

B6h	DISCTRL (Display Function Control)												
	D/CX	RDX	WRX	D[15:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XXXXXXXX	1	0	1	1	0	1	1	0	B6h
1st parameter	1	1	↑	XXXXXXXX	BYPASS	0	RM	DM	PTG[1:0]		PT[1:0]		XX
2nd parameter	1	1	↑	XXXXXXXX	0	GS	SS	SM	ISC[3:0]				XX
3rd Parameter	1	1	↑	XXXXXXXX	0	0	NL[5:0]						XX

Description

DM: Select the display operation mode.

DM	Interface Mode
0	Internal system clock
1	RGB interface

RM: Select the interface to access the GRAM. When RM='0', the driver will write display data to GRAM via system interface and the driver will write display data to GRAM via RGB interface when RM='1'.

RM	Interface for RAM access
0	System interface
1	RGB interface

BYPASS: Select the display data path whether memory or direct to shift register when RGB interface is used.

BYPASS	Display data path
0	Memory
1	Direct to shift register

Note: *RGB input signal, when set to bypass mode the Hsync low≧3,HBP≧3, HFP≧10.*

PTG [1:0]: Set the scan mode in non-display area.

PTG1	PTG0	Gate outputs in non-display area	Source outputs in non-display area
0	0	Normal scan	Set with the PT[2:0] bits
0	1	Setting prohibited	---
1	0	Interval scan	Set with the PT[2:0] bits
1	1	Setting prohibited	---

PT [1:0]: Determine source/VCOM output in a non-display area in the partial display mode.

PT[1:0]		Source output on non-display area
0	0	V63
0	1	V0
1	0	AGND
1	1	Hi-Z

SS: Select the shift direction of outputs from the source driver.

SS	Source Output Scan Direction
0	S1 → S960
1	S960 → S1

In addition to the shift direction, the settings for both SS and BGR bits are required to change the assignment of R, G, B dots to the source driver pins.

To assign R, G, B dots to the source driver pins from S1 to S960, set SS = 0.

To assign R, G, B dots to the source driver pins from S960 to S1, set SS = 1.

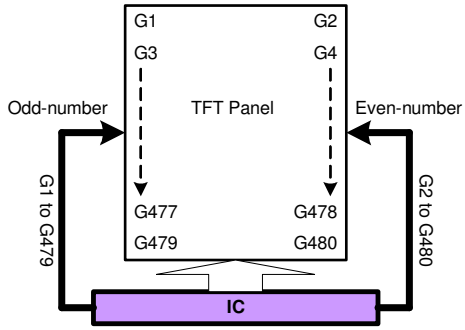
ISC[3:0]: Set the scan cycle when PTG selects interval scan in non-display area drive period. The scan cycle is defined by n frame periods, where n is an odd number from 3 to 31. The polarity of liquid crystal drive voltage from the gate driver is inverted in the same timing as the interval scan cycle.

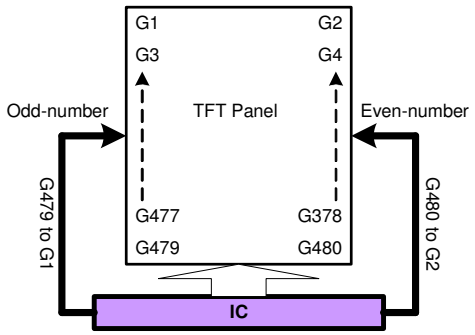
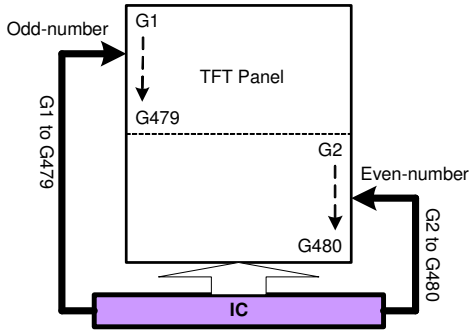
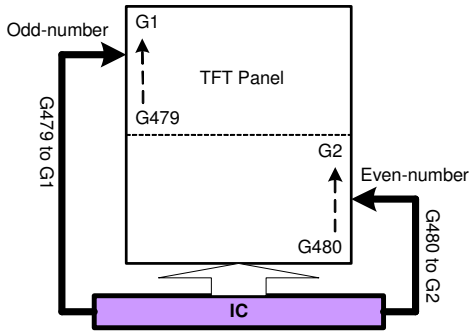
ISC[3:0]	Scan cycle	(f_{FRAME})=60Hz
4'h0	Setting inhibited	–
4'h1	3 frames	50ms
4'h2	5 frames	84ms
4'h3	7 frames	117ms
4'h4	9 frames	150ms
4'h5	11 frames	184ms
4'h6	13 frames	217ms
4'h7	15 frames	251ms
4'h8	17 frames	284ms
4'h9	19 frames	317ms
4'hA	21 frames	351ms
4'hB	23 frames	384ms
4'hC	25 frames	418ms
4'hD	27 frames	451ms
4'hE	29 frames	484ms
4'hF	31 frames	518ms

GS: Sets the direction of scan by the gate driver.

GS	Gate Output Scan Direction
0	G1 → G480
1	G480 → G1

SM: Sets the gate driver pin arrangement in combination with the GS bit (R60h) to select the optimal scan mode for the module.

SM	GS	Scan Direction	Gate Output Sequence
0	0		G1, G2, G3, G4, …,G476 G477, G478, G479, G480

0	1		G480, G479, G478, …, G9 G7, G5, G4, G3, G2, G1
1	0		G1, G3, G5, G7, …,G471 G473, G475, G477, G479 G2, G4, G6, G8, …,G472 G474, G476, G478, G480
1	1		G480, G478, G476, …,G14 G12, G10, G8, G6, G4, G2 G479, G477, G475,…,G13 G11, G9, G7, G5, G3, G1

NL [5:0]: Sets the number of lines to drive the LCD at an interval of 8 lines. The GRAM address mapping is not affected by the number of lines set by NL[5:0]. The number of lines must be the same or more than the number of lines necessary for the size of the liquid crystal panel.

NL[5:0]	LCD Drive Line
6'h00 ~ 6'h3B	8 * (NL5:0]+1) lines
Others	Setting inhibited

Restriction

Register Availability

Status	Availability
Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes
Normal Mode ON, Idle Mode ON, Sleep OUT	Yes
Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes
Partial Mode ON, Idle Mode ON, Sleep OUT	Yes
Sleep IN	Yes

Default

Status	Default Value						
	PTG[1:0]	PT[1:0]	GS	SS	SM	ISC[3:0]	NL[5:0]
Power ON Sequence	2'b00	2'b00	1'b0	1'b0	1'b0	4'b0010	6'b111011
H/W Reset	2'b00	2'b00	1'b0	1'b0	1'b0	4'b0010	6'b111011

Status	Default Value		
	RM	DM	BYPASS
Power ON Sequence	1'b0	1'b0	1'b1
H/W Reset	1'b0	1'b0	1'b1

8.2.57. Entry Mode Set (B7h)

B7h	ETMOD (Entry Mode Set)												
	D/CX	RDX	WRX	D[15:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XXXXXXXX	1	0	1	1	0	1	1	1	B7h
Parameter	1	1	↑	XXXXXXXX	EPF[1:0]		0	0	DSTB	GON	DTE	GAS	XX

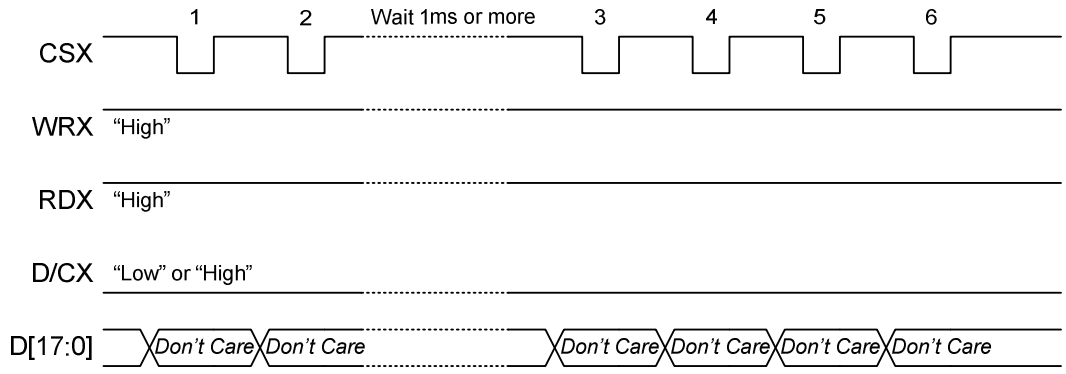
Description

DSTB: The ILI9486 driver enters the Deep Standby Mode when DSTB is set to high ("1"). In Deep Standby mode, both internal logic power and SRAM power are turn off, the display data stored in the Frame Memory and the instructions are not saved. Rewrite Frame Memory content and instructions after the Deep Standby Mode is exited.

Note: ILI9486 provides two ways to exit the Deep Standby Mode:

(1) Exit Deep Standby Mode by pull down CSX to low ("0") 6 times.

(2) Input a RESX pulse with effective low level duration to start up the inside logic regulator and makes a transition to the initial state.



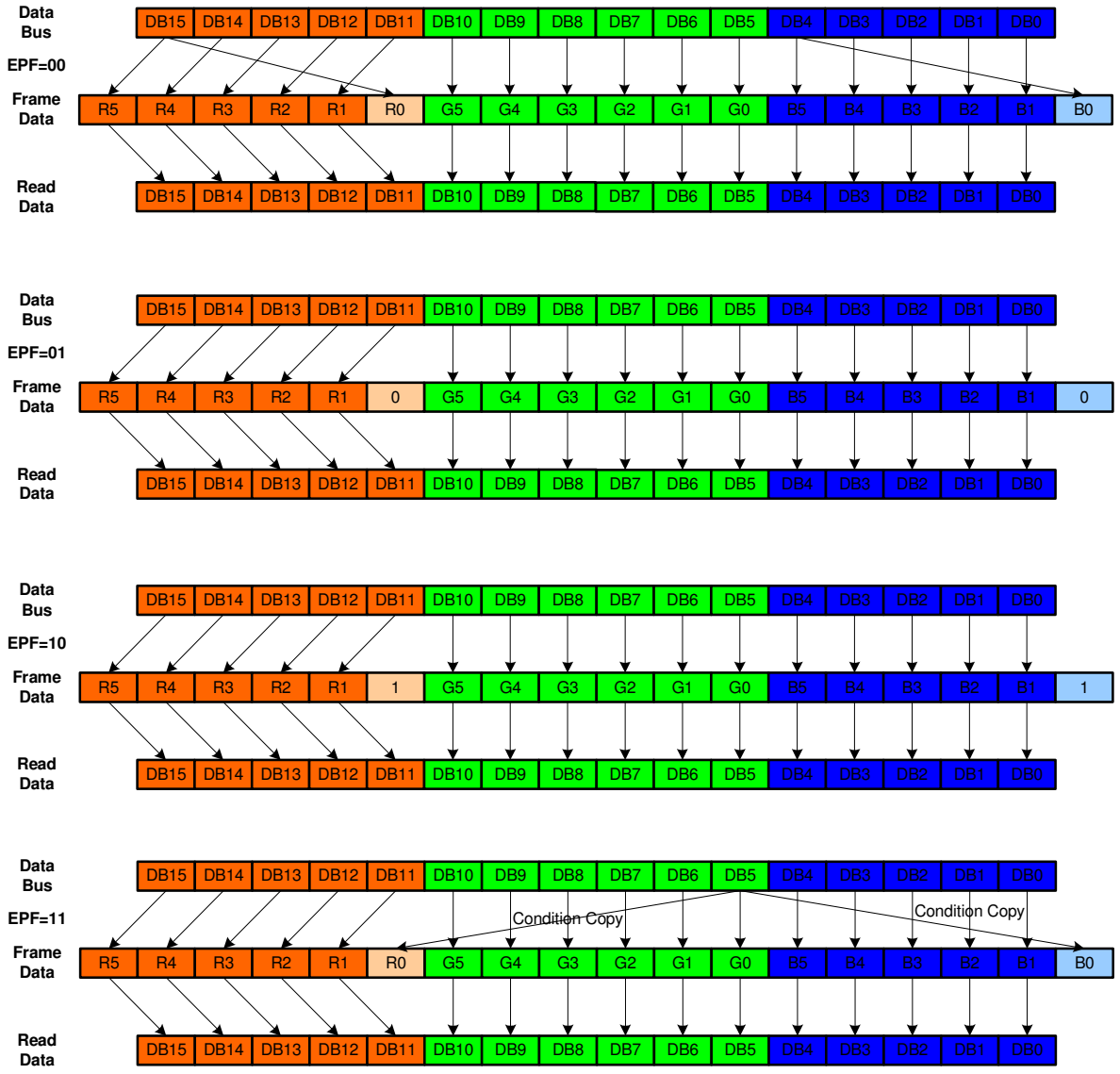
GAS: Low voltage detection control.

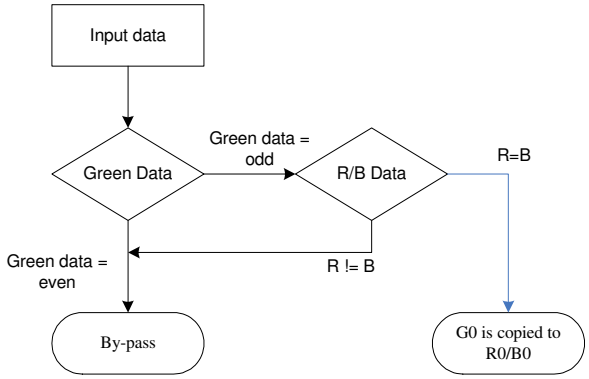
GAS	Low voltage detection
0	Enable
1	Disable

GON/DTE: Set the output level of gate driver G1 ~ G320 as follows

GON	DTE	G1~G320 Gate Output
0	0	VGH
0	1	VGH
1	0	VGL
1	1	Normal display

EPF[1:0] Set the data format when 16bbp (R,G,B) to 18 bbp (r, g, b) is stored in the internal GRAM





Restriction	

Register Availability

Status	Availability
Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes
Normal Mode ON, Idle Mode ON, Sleep OUT	Yes
Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes
Partial Mode ON, Idle Mode ON, Sleep OUT	Yes
Sleep IN	Yes

Default

Status	Default Value				
	EPF[1:0]	DSTB	GON	DTE	GAS
Power ON Sequence	2'b00	1'b0	1'b1	1'b1	1'b0
H/W Reset	2b'00	1'b0	1'b1	1'b1	1'b0

8.2.58. Power Control 1 (C0h)

C0h	PWCTRL 1 (Power Control 1)												
	D/CX	RDX	WRX	D[15:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XXXXXXXX	1	1	0	0	0	0	0	0	C0h
1st Parameter	1	1	↑	XXXXXXXX	0	0	0	VRH1[4:0]					XX
2nd Parameter	1	1	↑	XXXXXXXX	0	0	0	VRH2[4:0]					XX

Description

VRH1[4:0]: Sets the VREG1OUT voltage for positive gamma

VRH1[4:0]	VREG1OUT	VRH1[4:0]	VREG1OUT
5'h00	Halt (Vreg1out =Hiz)	5'h10	1.25 x 3.65 = 4.5625
5'h01	1.25 x 2.90 = 3.6250	5'h11	1.25 x 3.70 = 4.6250
5'h02	1.25 x 2.95 = 3.6875	5'h12	1.25 x 3.75 = 4.6875
5'h03	1.25 x 3.00 = 3.7500	5'h13	1.25 x 3.80 = 4.7500
5'h04	1.25 x 3.05 = 3.8125	5'h14	1.25 x 3.85 = 4.8125
5'h05	1.25 x 3.10 = 3.8750	5'h15	1.25 x 3.90 = 4.8750
5'h06	1.25 x 3.15 = 3.9375	5'h16	1.25 x 3.95 = 4.9375
5'h07	1.25 x 3.20 = 4.0000	5'h17	1.25 x 4.00 = 5.0000
5'h08	1.25 x 3.25 = 4.0625	5'h18	1.25 x 4.05 = 5.0625
5'h09	1.25 x 3.30 = 4.1250	5'h19	1.25 x 4.10 = 5.1250
5'h0A	1.25 x 3.35 = 4.1875	5'h1A	1.25 x 4.15 = 5.1875
5'h0B	1.25 x 3.40 = 4.2500	5'h1B	1.25 x 4.20 = 5.2500
5'h0C	1.25 x 3.45 = 4.3125	5'h1C	1.25 x 4.25 = 5.3125
5'h0D	1.25 x 3.50 = 4.3750	5'h1D	1.25 x 4.30 = 5.3750
5'h0E	1.25 x 3.55 = 4.4375	5'h1E	1.25 x 4.35 = 5.4375
5'h0F	1.25 x 3.60 = 4.5000	5'h1F	1.25 x 4.40 = 5.5000

VRH2[4:0]: Sets the VREG2OUT voltage for negative gamma

VRH2[4:0]	VREG2OUT	VRH2[4:0]	VREG2OUT
5'h00	Halt (Vreg2out =Hiz)	5'h10	-1.25 x 3.65 = -4.5625
5'h01	-1.25 x 2.90 = -3.6250	5'h11	-1.25 x 3.70 = -4.6250
5'h02	-1.25 x 2.95 = -3.6875	5'h12	-1.25 x 3.75 = -4.6875
5'h03	-1.25 x 3.00 = -3.7500	5'h13	-1.25 x 3.80 = -4.7500
5'h04	-1.25 x 3.05 = -3.8125	5'h14	-1.25 x 3.85 = -4.8125
5'h05	-1.25 x 3.10 = -3.8750	5'h15	-1.25 x 3.90 = -4.8750
5'h06	-1.25 x 3.15 = -3.9375	5'h16	-1.25 x 3.95 = -4.9375
5'h07	-1.25 x 3.20 = -4.0000	5'h17	-1.25 x 4.00 = -5.0000
5'h08	-1.25 x 3.25 = -4.0625	5'h18	-1.25 x 4.05 = -5.0625
5'h09	-1.25 x 3.30 = -4.1250	5'h19	-1.25 x 4.10 = -5.1250
5'h0A	-1.25 x 3.35 = -4.1875	5'h1A	-1.25 x 4.15 = -5.1875
5'h0B	-1.25 x 3.40 = -4.2500	5'h1B	-1.25 x 4.20 = -5.2500
5'h0C	-1.25 x 3.45 = -4.3125	5'h1C	-1.25 x 4.25 = -5.3125
5'h0D	-1.25 x 3.50 = -4.3750	5'h1D	-1.25 x 4.30 = -5.3750
5'h0E	-1.25 x 3.55 = -4.4375	5'h1E	-1.25 x 4.35 = -5.4375
5'h0F	-1.25 x 3.60 = -4.5000	5'h1F	-1.25 x 4.40 = -5.5000

Restriction

<table>
<tr><td>Register
Availability</td><td>
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode ON, Idle Mode OFF, Sleep OUT</td><td>Yes</td></tr>
<tr><td>Normal Mode ON, Idle Mode ON, Sleep OUT</td><td>Yes</td></tr>
<tr><td>Partial Mode ON, Idle Mode OFF, Sleep OUT</td><td>Yes</td></tr>
<tr><td>Partial Mode ON, Idle Mode ON, Sleep OUT</td><td>Yes</td></tr>
<tr><td>Sleep IN</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td>
<table>
<tr><th>Status</th><th>VRH1</th><th>VRH2</th></tr>
<tr><td>Power ON Sequence</td><td>5’b01110</td><td>5’b01110</td></tr>
<tr><td>H/W Reset</td><td>5’b01110</td><td>5’b01110</td></tr>
</table>
</td></tr>
</table>

8.2.59. Power Control 2 (C1h)

C1h	PWCTRL 2 (Power Control 2)												
	D/CX	RDX	WRX	D[15:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XXXXXXXX	1	1	0	0	0	0	0	1	C1h
1st parameter	1	1	↑	XXXXXXXX	0	SAP[2:0]			0	BT[2:0]			XX
2nd parameter	1	1	↑	XXXXXXXX	0	0	0	0	0	VC[2:0]			XX

Description

BT [2:0]: Sets the factor used in the step-up circuits.

Select the optimal step-up factor for the operating voltage. To reduce power consumption, set a smaller factor.

BT[2:0]	DDVDH	DDVDL	VCL	VGH	VGL
4'h0	Vci1 x 2	-(VCI1-VCL)	- Vci1	Vci1 x 6	- Vci1 x 5
4'h1					- Vci1 x 4
4'h2					- Vci1 x 3
4'h3				Vci1 x 5	- Vci1 x 5
4'h4					- Vci1 x 4
4'h5					- Vci1 x 3
4'h6				Vci1 x 4	- Vci1 x4
4'h7					- Vci1 x3

Note: To prevent the device damage, please keep VGH – DDVDH < 8V condition.

SAP [2:0]: It is used to adjust the constant current in the operational amplifier circuit in the LCD power supply circuit. Larger constant current enhances the drivability of the LCD, but it also increases the current consumption. Adjust the constant current taking the trade-off between the display quality and the current consumption into account.

SAP[2:0]			Description	Gamma bias control
0	0	0	Small	0.71 x I
0	0	1	Small	0.71 x I
0	1	0	Small	0.71 x I
0	1	1	Small	0.71 x I
1	0	0	Medium	1.00 x I
1	0	1	Medium to Large	1.25 x I
1	1	0	Large	1.43 x I
1	1	1	Large	1.43 x I

When starting the charge-pump of LCD in the Power ON stage, make sure that SAP=0, and set the SAP=1, after starting up the LCD power supply circuit.

VC [2:0]: Sets VCI1 regulator output voltage.

VC[2:0]	Vci1 voltage
3'h0	External VCI
3'h1	3.1V
3'h2	3.0V
3'h3	2.9V
3'h4	2.8V
3'h5	2.7V
3'h6	2.6V
3'h7	2.5V

Restriction

Register Availability

Status	Availability
Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes
Normal Mode ON, Idle Mode ON, Sleep OUT	Yes
Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes
Partial Mode ON, Idle Mode ON, Sleep OUT	Yes
Sleep IN	Yes

Default

Status	Default Value		
	BT[2:0]	SAP[2:0]	VC[2:0]
Power ON Sequence	3'b000	3'b110	3'b000
H/W Reset	3'b000	3'b110	3'b000

8.2.60. Power Control 3 (For Normal Mode) (C2h)

C2h	PWCTRL 3 (Power Control 3)												
	D/CX	RDX	WRX	D[15:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XXXXXXXX	1	1	0	0	0	0	1	0	C2h
1st parameter	1	1	↑	XXXXXXXX	0	DCA1[2:0]			0	DCA0[2:0]			XX

Description

DCA0 [2:0]: Selects the operating frequency of the step-up circuit 1/4/5 for Normal mode. The higher step-up operating frequency enhances the drivability of the step-up circuit and the quality of display but increases the current consumption. Adjust the frequency taking the trade-off between the display quality and the current consumption into account.

DCA1 [2:0]: Selects the operating frequency of the step-up circuit 2/3 for Normal mode. The higher step-up operating frequency enhances the drivability of the step-up circuit and the quality of display but increases the current consumption. Adjust the frequency taking the trade-off between the display quality and the current consumption into account.

DCA0[2:0]			Step-up cycle for step-up circuit 1/4/5
0	0	0	1/8 H
0	0	1	1/4 H
0	1	0	1/2 H
0	1	1	1 H
1	0	0	2 H
1	0	1	4 H
1	1	0	8 H
1	1	1	16 H

DCA1[2:0]			Step-up cycle for step-up circuit 2/3
0	0	0	1/2 H
0	0	1	1 H
0	1	0	2 H
0	1	1	4 H
1	0	0	8 H
1	0	1	16 H
1	1	0	32 H
1	1	1	64 H

Restriction

Register Availability

Status	Availability
Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes
Normal Mode ON, Idle Mode ON, Sleep OUT	Yes
Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes
Partial Mode ON, Idle Mode ON, Sleep OUT	Yes
Sleep IN	Yes

Default

Status	Default Value	
	DCA0[2:0]	DCA1[2:0]
Power ON Sequence	3'b011	3'b011
H/W Reset	3'b011	3'b011

8.2.61. Power Control 4 (For Idle Mode) (C3h)

C3h	PWCTRL 4 (Power Control 4)												
	D/CX	RDX	WRX	D[15:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XXXXXXXX	1	1	0	0	0	0	1	1	C3h
1st Parameter	1	1	↑	XXXXXXXX	0	DCB1[2:0]			0	DCB0[2:0]			XX

Description

DCB0 [2:0]: Selects the operating frequency of the step-up circuit 1/4/5 for Idle mode. The higher step-up operating frequency enhances the drivability of the step-up circuit and the quality of display but increases the current consumption. Adjust the frequency taking the trade-off between the display quality and the current consumption into account.

DCB1 [2:0]: Selects the operating frequency of the step-up circuit 2/3 for Idle mode. The higher step-up operating frequency enhances the drivability of the step-up circuit and the quality of display but increases the current consumption. Adjust the frequency taking the trade-off between the display quality and the current consumption into account.

DCB0[2:0]			Step-up cycle for step-up circuit 1/4/5
0	0	0	1/8 H
0	0	1	1/4 H
0	1	0	1/2 H
0	1	1	1 H
1	0	0	2 H
1	0	1	4 H
1	1	0	8 H
1	1	1	16 H

DCB1[2:0]			Step-up cycle for step-up circuit 2/3
0	0	0	1/2 H
0	0	1	1 H
0	1	0	2 H
0	1	1	4 H
1	0	0	8 H
1	0	1	16 H
1	1	0	32 H
1	1	1	64 H

Restriction

Register Availability

Status	Availability
Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes
Normal Mode ON, Idle Mode ON, Sleep OUT	Yes
Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes
Partial Mode ON, Idle Mode ON, Sleep OUT	Yes
Sleep IN	Yes

Default

Status	Default Value	
	DCB0[2:0]	DCB1[2:0]
Power ON Sequence	3'b011	3'b011
H/W Reset	3'b011	3'b011

8.2.62. Power Control 5 (For Partial Mode) (C4h)

C4h	PWCTRL 5 (Power Control 5)												
	D/CX	RDX	WRX	D[15:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XXXXXXXX	1	1	0	0	0	1	0	0	C4h
1st Parameter	1	1	↑	XXXXXXXX	0	DCC1[2:0]			0	DCC0[2:0]			XX

Description

DCC0 [2:0]: Selects the operating frequency of the step-up circuit 1/4/5 for Partial mode. The higher step-up operating frequency enhances the drivability of the step-up circuit and the quality of display but increases the current consumption. Adjust the frequency taking the trade-off between the display quality and the current consumption into account.

DCC1 [2:0]: Selects the operating frequency of the step-up circuit 2/3 for Partial mode. The higher step-up operating frequency enhances the drivability of the step-up circuit and the quality of display but increases the current consumption. Adjust the frequency taking the trade-off between the display quality and the current consumption into account.

DCC0[2:0]			Step-up cycle for step-up circuit 1/4/5
0	0	0	1/8 H
0	0	1	1/4 H
0	1	0	1/2 H
0	1	1	1 H
1	0	0	2 H
1	0	1	4 H
1	1	0	8 H
1	1	1	16 H

DCC1[2:0]			Step-up cycle for step-up circuit 2/3
0	0	0	1/2 H
0	0	1	1 H
0	1	0	2 H
0	1	1	4 H
1	0	0	8 H
1	0	1	16 H
1	1	0	32 H
1	1	1	64 H

Restriction

Register Availability

Status	Availability
Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes
Normal Mode ON, Idle Mode ON, Sleep OUT	Yes
Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes
Partial Mode ON, Idle Mode ON, Sleep OUT	Yes
Sleep IN	Yes

Default

Status	Default Value	
	DCC0[2:0]	DCC1[2:0]
Power ON Sequence	3'b011	3'b011
H/W Reset	3'b011	3'b011

8.2.63. VCOM Control (C5h)

C5h	VMCTRL (VCOM Control)												
	D/CX	RDX	WRX	D[15:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XXXXXXXX	1	1	0	0	0	1	0	1	C5h
1st Parameter	1	↑	1	XXXXXXXX	0	0	0	0	0	0	0	nVM	XX
2ndParameter	1	1	↑	XXXXXXXX	VCM_REG[7:0]								XX
3rdParameter	1	1	↑	XXXXXXXX	VCM_REG_EN	0	0	0	0	0	0	0	XX
4rdParameter	1	↑	1	XXXXXXXX	VCM_OUT[7:0]								XX

Description

nVM : When the NV memory is programmed, the nVM will be set as '1' automatically.
0 : NV memory is not programmed
1 : NV memory is programmed

VCM_REG [7:0] is used to set factor to generate VCOM voltage from the reference voltage VREG2OUT.

VCM[7:0]								VCOM
0	0	0	0	0	0	0	0	-2
0	0	0	0	0	0	0	1	-1.98438
0	0	0	0	0	0	1	0	-1.96875
0	0	0	0	0	0	1	1	-1.95313
0	0	0	0	0	1	0	0	-1.9375
0	0	0	0	0	1	0	1	-1.92188
0	0	0	0	0	1	1	0	-1.90625
0	0	0	0	0	1	1	1	-1.89063
0	0	0	0	1	0	0	0	-1.875
0	0	0	0	1	0	0	1	-1.85938
0	0	0	0	1	0	1	0	-1.84375
0	0	0	0	1	0	1	1	-1.82813
0	0	0	0	1	1	0	0	-1.8125
0	0	0	0	1	1	0	1	-1.79688
0	0	0	0	1	1	1	0	-1.78125
0	0	0	0	1	1	1	1	-1.76563
0	0	0	1	0	0	0	0	-1.75
0	0	0	1	0	0	0	1	-1.73438
0	0	0	1	0	0	1	0	-1.71875
0	0	0	1	0	0	1	1	-1.70313
0	0	0	1	0	1	0	0	-1.6875
0	0	0	1	0	1	0	1	-1.67188
0	0	0	1	0	1	1	0	-1.65625
0	0	0	1	0	1	1	1	-1.64063
0	0	0	1	1	0	0	0	-1.625
0	0	0	1	1	0	0	1	-1.60938
0	0	0	1	1	0	1	0	-1.59375
0	0	0	1	1	0	1	1	-1.57813
0	0	0	1	1	1	0	0	-1.5625
0	0	0	1	1	1	0	1	-1.54688
0	0	0	1	1	1	1	0	-1.53125
0	0	0	1	1	1	1	1	-1.51563
0	0	1	0	0	0	0	0	-1.5
0	0	1	0	0	0	0	1	-1.48438
0	0	1	0	0	0	1	0	-1.46875
0	0	1	0	0	0	1	1	-1.45313
0	0	1	0	0	1	0	0	-1.4375
0	0	1	0	0	1	0	1	-1.42188
0	0	1	0	0	1	1	0	-1.40625
0	0	1	0	0	1	1	1	-1.39063
0	0	1	0	1	0	0	0	-1.375
0	0	1	0	1	0	0	1	-1.35938
0	0	1	0	1	0	1	0	-1.34375
0	0	1	0	1	0	1	1	-1.32813

		0	0	1	0	1	1	0	0	-1.3125
		0	0	1	0	1	1	0	1	-1.29688
		0	0	1	0	1	1	1	0	-1.28125
		0	0	1	0	1	1	1	1	-1.26563
		0	0	1	1	0	0	0	0	-1.25
		0	0	1	1	0	0	0	1	-1.23438
		0	0	1	1	0	0	1	0	-1.21875
		0	0	1	1	0	0	1	1	-1.20313
		0	0	1	1	0	1	0	0	-1.1875
		0	0	1	1	0	1	0	1	-1.17188
		0	0	1	1	0	1	1	0	-1.15625
		0	0	1	1	0	1	1	1	-1.14063
		0	0	1	1	1	0	0	0	-1.125
		0	0	1	1	1	0	0	1	-1.10938
		0	0	1	1	1	0	1	0	-1.09375
		0	0	1	1	1	0	1	1	-1.07813
		0	0	1	1	1	1	0	0	-1.0625
		0	0	1	1	1	1	0	1	-1.04688
		0	0	1	1	1	1	1	0	-1.03125
		0	0	1	1	1	1	1	1	-1.01563
		0	1	0	0	0	0	0	0	-1
		0	1	0	0	0	0	0	1	-0.98438
		0	1	0	0	0	0	1	0	-0.96875
		0	1	0	0	0	0	1	1	-0.95313
		0	1	0	0	0	1	0	0	-0.9375
		0	1	0	0	0	1	0	1	-0.92188
		0	1	0	0	0	1	1	0	-0.90625
		0	1	0	0	0	1	1	1	-0.89063
		0	1	0	0	1	0	0	0	-0.875
		0	1	0	0	1	0	0	1	-0.85938
		0	1	0	0	1	0	1	0	-0.84375
		0	1	0	0	1	0	1	1	-0.82813
		0	1	0	0	1	1	0	0	-0.8125
		0	1	0	0	1	1	0	1	-0.79688
		0	1	0	0	1	1	1	0	-0.78125
		0	1	0	0	1	1	1	1	-0.76563
		0	1	0	1	0	0	0	0	-0.75
		0	1	0	1	0	0	0	1	-0.73438
		0	1	0	1	0	0	1	0	-0.71875
		0	1	0	1	0	0	1	1	-0.70313
		0	1	0	1	0	1	0	0	-0.6875
		0	1	0	1	0	1	0	1	-0.67188
		0	1	0	1	0	1	1	0	-0.65625
		0	1	0	1	0	1	1	1	-0.64063
		0	1	0	1	1	0	0	0	-0.625
		0	1	0	1	1	0	0	1	-0.60938
		0	1	0	1	1	0	1	0	-0.59375
		0	1	0	1	1	0	1	1	-0.57813
		0	1	0	1	1	1	0	0	-0.5625
		0	1	0	1	1	1	0	1	-0.54688
		0	1	0	1	1	1	1	0	-0.53125
		0	1	0	1	1	1	1	1	-0.51563
		0	1	1	0	0	0	0	0	-0.5
		0	1	1	0	0	0	0	1	-0.48438
		0	1	1	0	0	0	1	0	-0.46875
		0	1	1	0	0	0	1	1	-0.45313
		0	1	1	0	0	1	0	0	-0.4375
		0	1	1	0	0	1	0	1	-0.42188

0	1	1	0	0	1	1	0	-0.40625
0	1	1	0	0	1	1	1	-0.39063
0	1	1	0	1	0	0	0	-0.375
0	1	1	0	1	0	0	1	-0.35938
0	1	1	0	1	0	1	0	-0.34375
0	1	1	0	1	0	1	1	-0.32813
0	1	1	0	1	1	0	0	-0.3125
0	1	1	0	1	1	0	1	-0.29688
0	1	1	0	1	1	1	0	-0.28125
0	1	1	0	1	1	1	1	-0.26563
0	1	1	1	0	0	0	0	-0.25
0	1	1	1	0	0	0	1	-0.23438
0	1	1	1	0	0	1	0	-0.21875
0	1	1	1	0	0	1	1	-0.20313
0	1	1	1	0	1	0	0	-0.1875
0	1	1	1	0	1	0	1	-0.17188
0	1	1	1	0	1	1	0	-0.15625
0	1	1	1	0	1	1	1	-0.14063
0	1	1	1	1	0	0	0	-0.125
0	1	1	1	1	0	0	1	-0.10938
0	1	1	1	1	0	1	0	-0.09375
0	1	1	1	1	0	1	1	-0.07813
0	1	1	1	1	1	0	0	-0.0625
0	1	1	1	1	1	0	1	-0.04688
0	1	1	1	1	1	1	0	-0.03125
0	1	1	1	1	1	1	1	-0.01563
1	0	0	0	0	0	0	0	0
10000001~11111110								Inbibit
11111111								Halt

VCM_REG_EN: Select the Vcom value from **VCM_REG [7:0]** or **NV memory**.

0: VCOM value from NV memory.
1: VCOM value from VCM_REG [7:0].

VCM_OUT [7:0]: NV memory programmed value.

Restriction

Register Availability

Status	Availability
Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes
Normal Mode ON, Idle Mode ON, Sleep OUT	Yes
Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes
Partial Mode ON, Idle Mode ON, Sleep OUT	Yes
Sleep IN	Yes

Default

Status	Default Value			
	VCM_OUT[7:0]	VCM_REG_EN	VCM_REG[7:0]	nVM
Power ON Sequence	8'bXXXXXXXX	1'b0	8'b01100000	X
H/W Reset	8'bXXXXXXXX	1'b0	8'b01100000	X

8.2.64. CABC Control 1 (C6h)

C6h	CABCCTRL9 (CABC Control 9)												
	D/CX	RDX	WRX	D[15:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XXXXXXXX	1	1	0	0	0	1	1	0	C6h
1st Parameter	1	1	↑	XXXXXXXX	SCD_VLINE[7:0]								XX
2nd Parameter	1	1	↑	XXXXXXXX	0	0	0	0	0	SCD_VLINE[10:8]			XX

Description

SCD_VLINE [10:0]: This parameter is used set the display line per frame while partial mode ON.

SCD_VLINE[8:0]											Display line
D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	
0	0	0	0	0	0	0	0	0	0	0	Setting prohibited
0	0	0	0	0	0	0	0	0	0	1	1 line
0	0	0	0	0	0	0	0	0	1	0	2 lines
0	0	0	0	0	0	0	0	0	1	1	3 lines
0	0	0	0	0	0	0	0	1	0	0	4 lines
:											:
:											:
0	0	1	1	1	0	1	1	1	0	1	477 lines
0	0	1	1	1	0	1	1	1	1	0	478 lines
0	0	1	1	1	0	1	1	1	1	1	479 lines
0	0	1	1	1	1	0	0	0	0	0	480 lines
Others											Setting prohibited

Restriction

Register Availability

Status	Availability
Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes
Normal Mode ON, Idle Mode ON, Sleep OUT	Yes
Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes
Partial Mode ON, Idle Mode ON, Sleep OUT	Yes
Sleep IN	Yes

Default

Status	Default Value
Power ON Sequence	11'b00111100000
S/W Reset	11'b00111100000
H/W Reset	11'b00111100000

8.2.65. CABC Control 2 (C8h)

C8h	CABCCTRL1 (CABC Control 1)												
	D/CX	RDX	WRX	D[15:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XXXXXXXX	1	1	0	0	1	0	0	0	C8h
1st Parameter	1	1	↑	XXXXXXXX	0	0	0	0	0	LEDONR	LEDONPOL	PWMPOL	XX

Description

PWMPOL: The bit is used to define polarity of CABC_PWM signal.

BL	LEDPWMPOL	CABC_PWM pin
0	0	Always low
0	1	Always high
1	0	Original polarity of PWM signal
1	1	Inversed polarity of PWM signal

LEDONPOL: This bit is used to control CABC_ON pin.

BL	LEDONPOL	CABC_ON pin
0	0	0
0	1	1
1	0	LEDONR
1	1	Inversed LEDONR

LEDONR: This bit is used to control CABC_ON pin.

LEDONR	Description
0	Low
1	High

Restriction

Register Availability

Status	Availability
Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes
Normal Mode ON, Idle Mode ON, Sleep OUT	Yes
Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes
Partial Mode ON, Idle Mode ON, Sleep OUT	Yes
Sleep IN	Yes

Default

Status	Default Value		
	LEDONR	LEDONPOL	LEDPWMPOL
Power On Sequence	1'b0	1'b0	1'b0
SW Reset	No change	No change	No change
HW Reset	1'b0	1'b0	1'b0

8.2.66. CABC Control 3 (C9h)

C9h	CABCCTRL2 (CABC Control 2)												
	D/CX	RDX	WRX	D[15:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XXXXXXXX	1	1	0	0	1	0	0	1	C9h
1st Parameter	1	1	↑	XXXXXXXX	THRES_MOV[3:0]				THRES_STILL[3:0]				XX

Description

THRES_MOV [3:0]: This parameter is used to set the ratio (percentage) of the maximum number of pixels that makes display image white (data="63) to the total of pixels by image process in MOVING image mode. After this parameter sets the number of pixels that makes display image white, threshold grayscale value (DTH) that makes display image white is set so that the number of the pixels set by this parameter does not change.

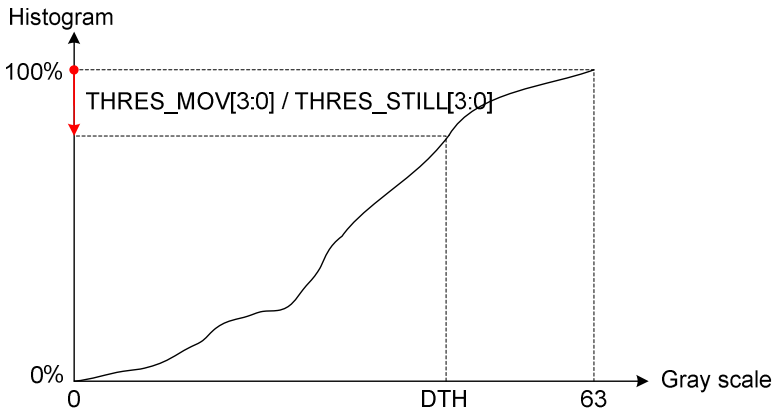
THRES_MOV[3:0]				Description
D3	D2	D1	D0	
0	0	0	0	99 %
0	0	0	1	98 %
0	0	1	0	96 %
0	0	1	1	94 %
0	1	0	0	92 %
0	1	0	1	90 %
0	1	1	0	88 %
0	1	1	1	86 %

THRES_MOV[3:0]				Description
D3	D2	D1	D0	
1	0	0	0	84 %
1	0	0	1	82 %
1	0	1	0	80 %
1	0	1	1	78 %
1	1	0	0	76 %
1	1	0	1	74 %
1	1	1	0	72 %
1	1	1	1	70 %

THRES_STILL [3:0]: This parameter is used to set the ratio (percentage) of the maximum number of pixels that makes display image white (data="63) to the total of pixels by image process in STILL mode. After this parameter sets the number of pixels that makes display image white, threshold grayscale value (DTH) that makes display image white is set so that the number of the pixels set by this parameter does not change.

THRES_STILLI[3:0]				Description
D3	D2	D1	D0	
0	0	0	0	99 %
0	0	0	1	98 %
0	0	1	0	96 %
0	0	1	1	94 %
0	1	0	0	92 %
0	1	0	1	90 %
0	1	1	0	88 %
0	1	1	1	86 %

THRES_STILL[3:0]				Description
D3	D2	D1	D0	
1	0	0	0	84 %
1	0	0	1	82 %
1	0	1	0	80 %
1	0	1	1	78 %
1	1	0	0	76 %
1	1	0	1	74 %
1	1	1	0	72 %
1	1	1	1	70 %



Restriction

Register Availability

Status	Availability
Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes
Normal Mode ON, Idle Mode ON, Sleep OUT	Yes
Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes
Partial Mode ON, Idle Mode ON, Sleep OUT	Yes
Sleep IN	Yes

Default

Status	Default Value	
	THRES_MOV[3:0]	THRES_STILL[3:0]
Power ON Sequence	4'b1011 b	4'b1011 b
S/W Reset	4'b1011 b	4'b1011 b
H/W Reset	4'b1011 b	4'b1011 b

8.2.67. CABC Control 4 (CAh)

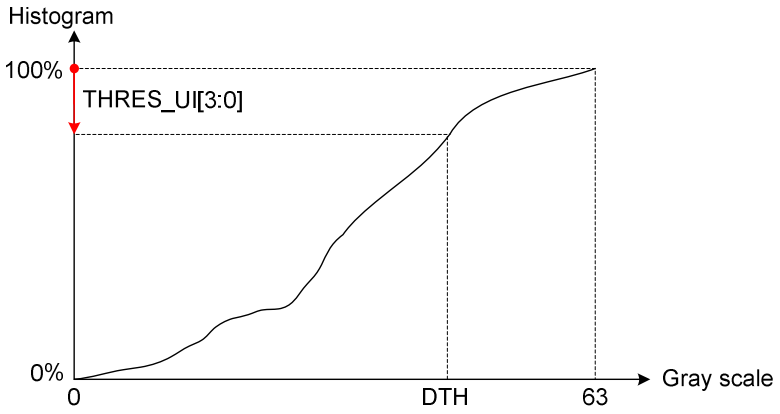
CAh	CABCCTRL3 (CABC Control 3)												
	D/CX	RDX	WRX	D[15:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XXXXXXXX	1	1	0	0	1	0	1	0	CAh
1st Parameter	1	1	↑	XXXXXXXX	0	0	0	0	THRES_UI[3:0]				XX

Description

THRES_UI [3:0]: This parameter is used to set the ratio (percentage) of the maximum number of pixels that makes display image white (data="63) to the total of pixels by image process in USER INTERFACE mode. After this parameter sets the number of pixels that makes display image white, threshold grayscale value (DTH) that makes display image white is set so that the number of the pixels set by this parameter does not change.

THRES_UI[3:0]				Description
D3	D2	D1	D0	
0	0	0	0	99 %
0	0	0	1	98 %
0	0	1	0	96 %
0	0	1	1	94 %
0	1	0	0	92 %
0	1	0	1	90 %
0	1	1	0	88 %
0	1	1	1	86 %

THRES_UI[3:0]				Description
D3	D2	D1	D0	
1	0	0	0	84 %
1	0	0	1	82 %
1	0	1	0	80 %
1	0	1	1	78 %
1	1	0	0	76 %
1	1	0	1	74 %
1	1	1	0	72 %
1	1	1	1	70 %



Restriction

Register Availability

Status	Availability
Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes
Normal Mode ON, Idle Mode ON, Sleep OUT	Yes
Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes
Partial Mode ON, Idle Mode ON, Sleep OUT	Yes
Sleep IN	Yes

Default

Status	Default Value
Power ON Sequence	4'b1011 b
S/W Reset	4'b1011 b
H/W Reset	4'b1011 b

8.2.68. CABC Control 5 (CBh)

CBh	CABCCTRL4 (CABC Control 4)												
	D/CX	RDX	WRX	D[15:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XXXXXXXX	1	1	0	0	1	0	1	1	CBh
1st Parameter	1	1	↑	XXXXXXXX	DTH_MOV[3:0]				DTH_STILL[3:0]				XX

Description

DTH_MOV [3:0]: This parameter is used set the minimum limitation of grayscale threshold value in MOVING image mode.

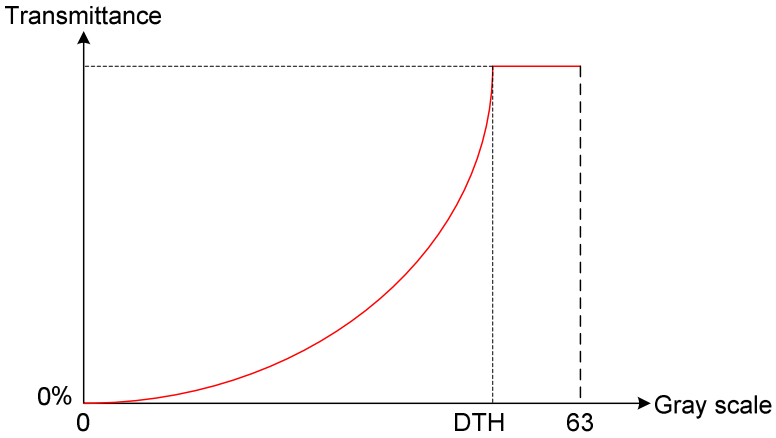
DTH_MOV[3:0]				Description
D3	D2	D1	D0	
0	0	0	0	224
0	0	0	1	220
0	0	1	0	216
0	0	1	1	212
0	1	0	0	208
0	1	0	1	204
0	1	1	0	200
0	1	1	1	196

DTH_MOV[3:0]				Description
D3	D2	D1	D0	
1	0	0	0	192
1	0	0	1	188
1	0	1	0	184
1	0	1	1	180
1	1	0	0	176
1	1	0	1	172
1	1	1	0	168
1	1	1	1	164

DTH_OPT [2:0]: This parameter is used to set the minimum limitation of grayscale threshold value in STILL image mode.

DTH_STILLI[3:0]				Description
D3	D2	D1	D0	
0	0	0	0	224
0	0	0	1	220
0	0	1	0	216
0	0	1	1	212
0	1	0	0	208
0	1	0	1	204
0	1	1	0	200
0	1	1	1	196

DTH_STILL[3:0]				Description
D3	D2	D1	D0	
1	0	0	0	192
1	0	0	1	188
1	0	1	0	184
1	0	1	1	180
1	1	0	0	176
1	1	0	1	172
1	1	1	0	168
1	1	1	1	164



Restriction

Register Availability

Status	Availability
Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes
Normal Mode ON, Idle Mode ON, Sleep OUT	Yes
Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes
Partial Mode ON, Idle Mode ON, Sleep OUT	Yes
Sleep IN	Yes

Default

Status	Default Value	
	DTH_MOV[3:0]	DTH_STILL[3:0]
Power ON Sequence	4'b1010 b	4'b1000 b
S/W Reset	4'b1010 b	4'b1000 b
H/W Reset	4'b1010 b	4'b1000 b

8.2.69. CABC Control 6 (CCh)

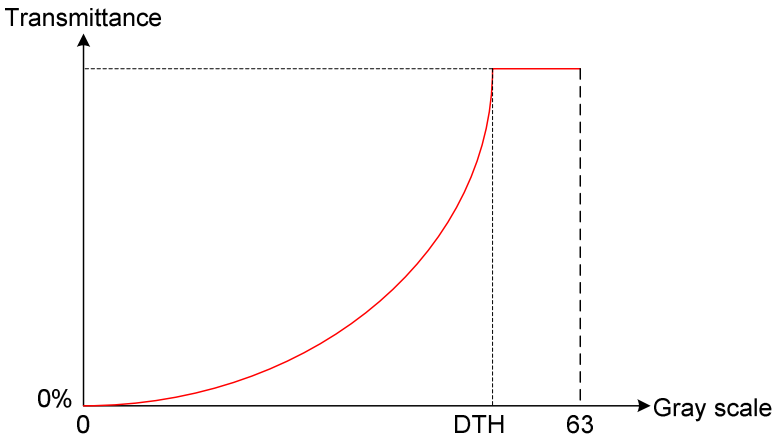
CCh	CABCCTRL5 (CABC Control 5)												
	D/CX	RDX	WRX	D[15:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XXXXXXXX	1	1	0	0	1	1	0	0	CCh
1st Parameter	1	1	↑	XXXXXXXX	0	0	0	0	DTH_UI[3:0]				XX

Description

DTH_UI [3:0]: This parameter is used set the minimum limitation of grayscale threshold value in USER INTERFACE mode.

DTH_UI[3:0]				Description
D3	D2	D1	D0	
0	0	0	0	252
0	0	0	1	248
0	0	1	0	244
0	0	1	1	240
0	1	0	0	236
0	1	0	1	232
0	1	1	0	228
0	1	1	1	224

DTH_UI[3:0]				Description
D3	D2	D1	D0	
1	0	0	0	220
1	0	0	1	216
1	0	1	0	212
1	0	1	1	208
1	1	0	0	204
1	1	0	1	200
1	1	1	0	196
1	1	1	1	192



Restriction

Register Availability

Status	Availability
Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes
Normal Mode ON, Idle Mode ON, Sleep OUT	Yes
Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes
Partial Mode ON, Idle Mode ON, Sleep OUT	Yes
Sleep IN	Yes

Default

Status	Default Value
Power ON Sequence	4'b0100 b
S/W Reset	4'b0100 b
H/W Reset	4'b0100 b

8.2.70. CABC Control 7 (CDh)

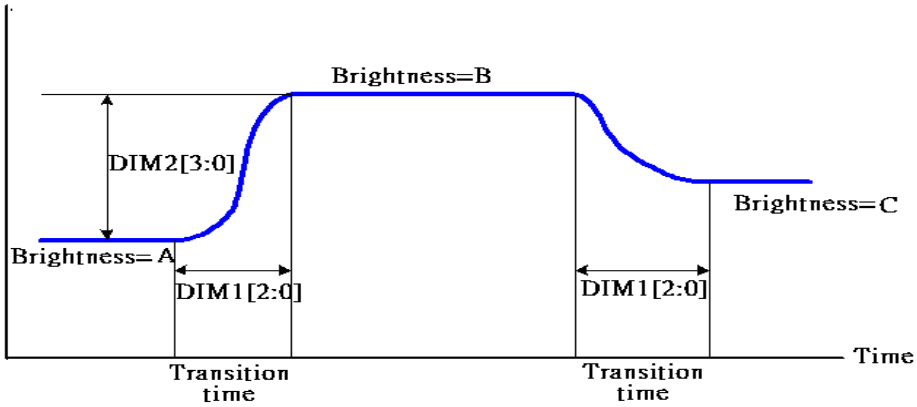
CDh	CABCCTRL6 (CABC Control 6)												
	D/CX	RDX	WRX	D[15:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XXXXXXXX	1	1	0	0	1	1	0	1	CDh
1st Parameter	1	1	↑	XXXXXXXX	0	DIM_MOV[2:0]			0	DIM_STILL[2:0]			XX

Description

DIM_STILL [2:0]: This parameter is used set the transition time of brightness level change to avoid the sharp brightness change on vision in still mode.

DIM_MOV [2:0]: This parameter is used set the transition time of brightness level change to avoid the sharp brightness change on vision in still mode.

DIM_MOV[2:0]/DIM_STILL[2 :0]			Description
D2	D1	D0	
0	0	0	1 frame
0	0	1	1 frame
0	1	0	2 frames
0	1	1	4 frames
1	0	0	8 frames
1	0	1	16 frames
1	1	0	32 frames
1	1	1	64 frames



*Note: As above picture **DIM1[2:0]** mean **DIM_MOV[2:0]** or **DIM_STILL[2:0]** or **DIM_UI[2:0]** in different mode.*

Restriction

Register Availability

Status	Availability
Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes
Normal Mode ON, Idle Mode ON, Sleep OUT	Yes
Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes
Partial Mode ON, Idle Mode ON, Sleep OUT	Yes
Sleep IN	Yes

Default

Status	Default Value	
	DIM_MOV[2:0]	DIM_STILL[2:0]
Power ON Sequence	4'b100 b	3'b011 b
S/W Reset	4'b100 b	3'b011 b
H/W Reset	4'b100 b	3'b011 b

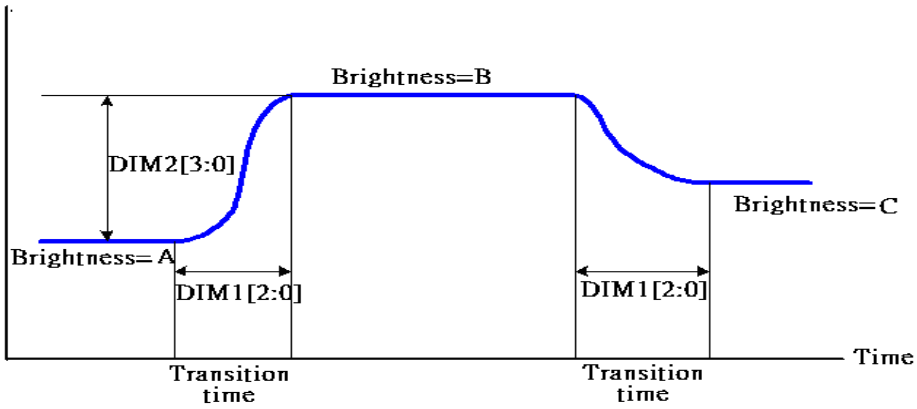
8.2.71. CABC Control 8 (CEh)

CEh	CABCCTRL7 (CABC Control 7)												
	D/CX	RDX	WRX	D[15:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XXXXXXXX	1	1	0	0	1	1	1	0	CEh
1st Parameter	1	1	↑	XXXXXXXX	DIM_MIN[3:0]				0	DIM_UI[2:0]			XX

Description

DIM_UI [2:0]: This parameter is used set the transition time of brightness level change to avoid the sharp brightness change on vision in UI mode.

DIM_MOV[2:0]/DIM_STILL[2 :0]			Description
D2	D1	D0	
0	0	0	1 frame
0	0	1	1 frame
0	1	0	2 frames
0	1	1	4 frames
1	0	0	8 frames
1	0	1	16 frames
1	1	0	32 frames
1	1	1	64 frames



*Note1: As above picture **DIM1[2:0]** mean **DIM_MOV[2:0]** or **DIM_STILL[2:0]** or **DIM_UI[2:0]** in different mode.*

*Note2: As above picture **DIM2[3:0]** mean **DIM_MIN[3:0]**.*

DIM_MIN [3:0]: The parameter is used to set the imitation of minimum brightness change. If the parameter is large than the difference between target brightness and current brightness, then the brightness will not change.

Restriction

Register Availability

Status	Availability
Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes
Normal Mode ON, Idle Mode ON, Sleep OUT	Yes
Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes
Partial Mode ON, Idle Mode ON, Sleep OUT	Yes
Sleep IN	Yes

Default

Status	Default Value	
	DIM_MIN[3:0]	DIM_UI[2:0]
Power ON Sequence	4'b0000 b	3'b010 b
S/W Reset	4'b0000 b	3'b010 b
H/W Reset	4'b0000 b	3'b010 b

8.2.72. CABC Control 9 (CFh)

CFh	CABCCTRL8 (CABC Control 8)												
	DCX	RDX	WRX	D[15:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XXXXXXXX	1	1	0	0	1	1	1	1	CFh
1st Parameter	1	1	↑	XXXXXXXX	PWM_DIV[7:0]								XX

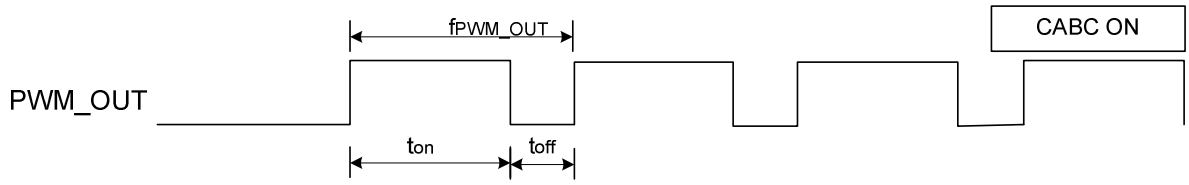
Description

PWM_DIV [7:0]: PWM_OUT output period control. This command is used to adjust the PWM waveform period of PWM_OUT.

The PWM period can be calculated using the equation in the following.

$$f_{PWM\_OUT} = \frac{18MHz}{(PWM\_DIV[7:0]+1)\times 255}$$

PWM_DIV[7:0]								f_{PWM_OUT}
D7	D6	D5	D4	D3	D2	D1	D0	
0	0	0	0	0	0	0	0	70.58 KHz
0	0	0	0	0	0	0	1	35.29 KHz
0	0	0	0	0	0	1	0	23.53 KHz
0	0	0	0	0	0	1	1	17.64 KHz
0	0	0	0	0	1	0	0	14.11KHz
:								:
1	1	1	1	1	0	1	1	280.0Hz
1	1	1	1	1	1	0	0	279.0 Hz
1	1	1	1	1	1	0	1	277.9 Hz
1	1	1	1	1	1	1	0	276.8 Hz
1	1	1	1	1	1	1	1	275.8 Hz



Note : The output frequency tolerance of internal frequency divider in CABC is ±10%

Restriction: EXTC should be high to enable this command

Register Availability

Status	Availability
Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes
Normal Mode ON, Idle Mode ON, Sleep OUT	Yes
Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes
Partial Mode ON, Idle Mode ON, Sleep OUT	Yes
Sleep IN	Yes

Default

Status	Default Value
Power ON Sequence	8'b00011000
H/W Reset	8'b00011000

8.2.73. NV Memory Write (D0h)

<table>
<tr><th>D0h</th><th colspan="13">NVMWR (NV Memory Write)</th></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D[15:8]</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XXXXXXXX</td><td>1</td><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>D0h</td></tr>
<tr><td>1st Parameter</td><td>1</td><td>1</td><td>↑</td><td>XXXXXXXX</td><td>0</td><td>0</td><td>0</td><td colspan="5">PGM_ADR[4:0]</td><td>XX</td></tr>
<tr><td>2nd Parameter</td><td>1</td><td>1</td><td>↑</td><td>XXXXXXXX</td><td colspan="8">PGM_DATA[7:0]</td><td>XX</td></tr>
<tr><td>Description</td><td colspan="13">This command is used to program the NV memory data. After a successful OTP operation, the information of PGM_DATA [7:0] will programmed to NV memory.

PGM_ADR [4:0]: The select bits of ID2, ID3 and VMF[6:0] programming.
<table>
<tr><th colspan="5">PGM_ADR[4:0]</th><th>Programmed NV Memory Selection</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>ID2 programming</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>ID3 programming</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>VMF[6:0] programming</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>MDDI V1.2 programing</td></tr>
<tr><td colspan="5">Others</td><td>Reserved</td></tr>
</table>
PGM_DATA [7:0]: The programmed data.</td></tr>
<tr><td>Restriction</td><td colspan="13"></td></tr>
<tr><td>Register Availability</td><td colspan="13">
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode ON, Idle Mode OFF, Sleep OUT</td><td>Yes</td></tr>
<tr><td>Normal Mode ON, Idle Mode ON, Sleep OUT</td><td>Yes</td></tr>
<tr><td>Partial Mode ON, Idle Mode OFF, Sleep OUT</td><td>Yes</td></tr>
<tr><td>Partial Mode ON, Idle Mode ON, Sleep OUT</td><td>Yes</td></tr>
<tr><td>Sleep IN</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td colspan="13">
<table>
<tr><th rowspan="2">Status</th><th colspan="2">Default Value</th></tr>
<tr><th>PGM_ADR[4:0]</th><th>PGM_DATA[7:0]</th></tr>
<tr><td>Power ON Sequence</td><td>3’b00000</td><td>8’bXXXXXXXX</td></tr>
<tr><td>H/W Reset</td><td>3’b00000</td><td>8’bXXXXXXXX</td></tr>
</table>
</td></tr>
</table>

8.2.74. NV Memory Protection Key (D1h)

D1h	NVMPKEY (NV Memory Protection Key)												
	D/CX	RDX	WRX	D[15:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XXXXXXXX	1	1	0	1	0	0	0	1	D1h
1st Parameter	1	1	↑	XXXXXXXX	KEY[23:16]								55h
2nd Parameter	1	1	↑	XXXXXXXX	KEY[15:8]								AAh
3rd Parameter	1	1	↑	XXXXXXXX	KEY[7:0]								66h
Description	**KEY [23:0]:** NV memory programming protection key. When writing OTP data to D0h, this register must be set to 0x55AA66h to enable OTP programming. If D1h register is not written with 0x55AA66h, then NV memory programming will be aborted.												
Restriction													
Register Availability													

Status	Availability
Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes
Normal Mode ON, Idle Mode ON, Sleep OUT	Yes
Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes
Partial Mode ON, Idle Mode ON, Sleep OUT	Yes
Sleep IN	Yes

Default

Status	Default Value
Power ON Sequence	24'h55AA66h
H/W Reset	24'h55AA66h

8.2.75. NV Memory Status Read (D2h)

D2h	RDNVM (NV Memory Status Read)												
	D/CX	RDX	WRX	D[15:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XXXXXXXX	1	1	0	1	0	0	1	0	D2h
1st Parameter	1	↑	1	XXXXXXXX	X	X	X	X	X	X	X	X	XX
2nd Parameter	1	↑	1	XXXXXXXX	ID2_CNT[3:0]				ID1_CNT[3:0]				XX
3rd Parameter	1	↑	1	XXXXXXXX	VMF_CNT[3:0]				ID3_CNT[3:0]				XX
4th Parameter	1	↑	1	XXXXXXXX	BUSY	0	0	0	0	0	0	MDDI_V12	XX
5th Parameter	1	↑	1	XXXXXXXX	OTP_DATA[7:0]								XX

Description

PGM_CNT [1:0]: NV memory program record. The bits will increase "+1" automatically after writing the NV_VMF [5:0] to NV memory.

ID1_CNT[3:0]/ID2_CNT[3:0] / ID3_CNT[3:0] / VMF_CNT[3:0]				Description
0	0	0	0	No Programmed
0	0	0	1	Programmed 1 time
0	0	1	1	Programmed 2 times
0	1	1	1	Programmed 3 times
1	1	1	1	Programmed 4 times

MDDI_V12: The bit =0, mean MDDI Version 1.0, the bit=1, mean MDDI Version 1.2.

BUSY: The status bit of NV memory programming.

BUSY	The Status of NV Memory
0	Idle
1	Busy

OTP_DATA [7:0]: The programmed value of VMF parameter in NV memory. This function is only for read operation.

Restriction

Register Availability

Status	Availability
Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes
Normal Mode ON, Idle Mode ON, Sleep OUT	Yes
Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes
Partial Mode ON, Idle Mode ON, Sleep OUT	Yes
Sleep IN	Yes

Default

Status	Default Value						
	MDDI_V12	ID3_CNT	ID2_CNT	ID1_CNT	VMF_CNT	BUSY	OTP_DATA
Power ON Sequence	X	X	X	X	X	X	X
H/W Reset	X	X	X	X	X	X	X

8.2.76. Read ID4 (D3h)

D3h	RDID4 (Read ID4)												
	D/CX	RDX	WRX	D[15:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XXXXXXXX	1	1	0	1	0	0	1	1	D3h
1st Parameter	1	↑	1	XXXXXXXX	X	X	X	X	X	X	X	X	XX
2ndParameter	1	↑	1	XXXXXXXX	0	0	0	0	0	0	0	0	00h
3rdParameter	1	↑	1	XXXXXXXX	1	0	0	1	0	1	0	0	94h
4th Parameter	1	↑	1	XXXXXXXX	1	0	0	0	0	0	1	0	86h
Description	Read IC device code. The 1st parameter is dummy read period. The 2nd parameter means the IC version. The 3rd and 4th parameter mean the IC model name.												
Restriction													

Register Availability

Status	Availability
Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes
Normal Mode ON, Idle Mode ON, Sleep OUT	Yes
Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes
Partial Mode ON, Idle Mode ON, Sleep OUT	Yes
Sleep IN	Yes

Default

Status	Default Value
Power ON Sequence	ID4=24'h009486h
H/W Reset	ID4=24'h009486h

8.2.77. PGAMCTRL(Positive Gamma Control) (E0h)

	PGAMCTRL (Positive Gamma Control)												
	D/CX	RDX	WRX	D[15:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XXXXXXXX	1	1	1	0	0	0	0	0	E0h
1st Parameter	1	1	↑	XXXXXXXX	0	0	0	VP0[4:0]					XX
2ndParameter	1	1	↑	XXXXXXXX	0	0	VP1[5:0]						XX
3rdParameter	1	1	↑	XXXXXXXX	0	0	VP2[5:0]						XX
4th Parameter	1	1	↑	XXXXXXXX	0	0	0	0	VP4[3:0]				XX
5th Parameter	1	1	↑	XXXXXXXX	0	0	0	VP6[4:0]					XX
6th Parameter	1	1	↑	XXXXXXXX	0	0	0	0	VP13[3:0]				XX
7th Parameter	1	1	↑	XXXXXXXX	0	VP20[6:0]							XX
8th Parameter	1	1	↑	XXXXXXXX	VP36[3:0]				VP27[3:0]				XX
9th Parameter	1	1	↑	XXXXXXXX	0	VP43[6:0]							XX
10thParameter	1	1	↑	XXXXXXXX	0	0	0	0	VP50[3:0]				XX
11thParameter	1	1	↑	XXXXXXXX	0	0	0	VP57[4:0]					XX
12thParameter	1	1	↑	XXXXXXXX	0	0	0	0	VP59[3:0]				XX
13thParameter	1	1	↑	XXXXXXXX	0	0	VP61[5:0]						XX
14thParameter	1	1	↑	XXXXXXXX	0	0	VP62[5:0]						XX
15thParameter	1	1	↑	XXXXXXXX	0	0	0	VP63[4:0]					XX
Description	Set the gray scale voltage to adjust the gamma characteristics of the TFT panel.												
Restriction													

Register Availability

Status	Availability
Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes
Normal Mode ON, Idle Mode ON, Sleep OUT	Yes
Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes
Partial Mode ON, Idle Mode ON, Sleep OUT	Yes
Sleep IN	Yes

8.2.78. NGAMCTRL (Negative Gamma Correction) (E1h)

	NGAMCTRL (Negative Gamma Correction)												
	D/CX	RDX	WRX	D[15:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XXXXXXXX	1	1	1	0	0	0	0	1	E1h
1st Parameter	1	1	↑	XXXXXXXX	0	0	0	VN0[4:0]					XX
2ndParameter	1	1	↑	XXXXXXXX	0	0	VN1[5:0]						XX
3rdParameter	1	1	↑	XXXXXXXX	0	0	VN2[5:0]						XX
4th Parameter	1	1	↑	XXXXXXXX	0	0	0	0	VN4[3:0]				XX
5th Parameter	1	1	↑	XXXXXXXX	0	0	0	RVN6[4:0]					XX
6th Parameter	1	1	↑	XXXXXXXX	0	0	0	0	VN13[3:0]				XX
7th Parameter	1	1	↑	XXXXXXXX	0	VN20[6:0]							XX
8th Parameter	1	1	↑	XXXXXXXX	VN36[3:0]				VN27[3:0]				XX
9th Parameter	1	1	↑	XXXXXXXX	0	VN43[6:0]							XX
10thParameter	1	1	↑	XXXXXXXX	0	0	0	0	VN50[3:0]				XX
11thParameter	1	1	↑	XXXXXXXX	0	0	0	VN57[4:0]					XX
12thParameter	1	1	↑	XXXXXXXX	0	0	0	0	VN59[3:0]				XX
13thParameter	1	1	↑	XXXXXXXX	0	0	VN61[5:0]						XX
14thParameter	1	1	↑	XXXXXXXX	0	0	VN62[5:0]						XX
15thParameter	1	1	↑	XXXXXXXX	0	0	0	VN63[4:0]					XX
Description	Set the gray scale voltage to adjust the gamma characteristics of the TFT panel.												
Restriction													

Register Availability

Status	Availability
Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes
Normal Mode ON, Idle Mode ON, Sleep OUT	Yes
Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes
Partial Mode ON, Idle Mode ON, Sleep OUT	Yes
Sleep IN	Yes

8.2.79. Digital Gamma Control 1 (E2h)

E2h	DGAMCTRL (Digital Gamma Control 1)												
	D/CX	RDX	WRX	D[15:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XXXXXXXX	1	1	1	0	0	0	1	0	E2h
1st Parameter	1	1	↑	XXXXXXXX	RCA0[3:0]				BCA0[3:0]				XX
:	1	1	↑	XXXXXXXX	RCAx[3:0]				BCAx[3:0]				XX
16rdParameter	1	1	↑	XXXXXXXX	RCA15[3:0]				BCA15[3:0]				XX
Description	**RCAx [3:0]:** Gamma Macro-adjustment registers for red gamma curve. **BCAx [3:0]:** Gamma Macro-adjustment registers for blue gamma curve.												
Restriction													

Register Availability

Status	Availability
Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes
Normal Mode ON, Idle Mode ON, Sleep OUT	Yes
Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes
Partial Mode ON, Idle Mode ON, Sleep OUT	Yes
Sleep IN	Yes

Default

Status	Default Value	
	RCAx[3:0]	BCAx[3:0]
Power ON Sequence	TBD	TBD
H/W Reset	TBD	TBD

8.2.80. Digital Gamma Control 2 (E3h)

E3h	DGAMCTRL (Digital Gamma Control 2)												
	D/CX	RDX	WRX	D[15:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XXXXXXXX	1	1	1	0	0	0	1	1	E3h
1st Parameter	1	1	↑	XXXXXXXX	RFA0[3:0]				BFA0[3:0]				XX
:	1	1	↑	XXXXXXXX	RFAx[3:0]				BFAx[3:0]				XX
64rdParameter	1	1	↑	XXXXXXXX	RFA63[3:0]				BFA63[3:0]				XX
Description	**RFAx [3:0]:** Gamma Micro-adjustment register for red gamma curve. **BFAx [3:0]:** Gamma Micro-adjustment register for blue gamma curve.												
Restriction													

Register Availability

Status	Availability
Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes
Normal Mode ON, Idle Mode ON, Sleep OUT	Yes
Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes
Partial Mode ON, Idle Mode ON, Sleep OUT	Yes
Sleep IN	Yes

Default

Status	Default Value	
	RFAx[3:0]	BFAx[3:0]
Power ON Sequence	TBD	TBD
H/W Reset	TBD	TBD

8.2.81. SPI Read Command Setting(FBh)

FBh	DGAMCTRL (Digital Gamma Control 2)												
	D/CX	RDX	WRX	D[15:8]	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XXXXXXXX	1	1	1	1	1	0	1	1	FBh
1st Parameter	1	1	↑	XXXXXXXX	0	0	0	SPI_READ_EN	SPI_CNT[3:0]				XX
Description	**SPI_READ_EN:** SPI read enable (see note). **SPI_CNT [3:0]:** SPI read parameter number (see note) *Note: Set "RFBh" once only usefull to read one parameter of register one time, the next read need to set "RFBh" again.*												
Restriction													

Register Availability

Status	Availability
Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes
Normal Mode ON, Idle Mode ON, Sleep OUT	Yes
Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes
Partial Mode ON, Idle Mode ON, Sleep OUT	Yes
Sleep IN	Yes

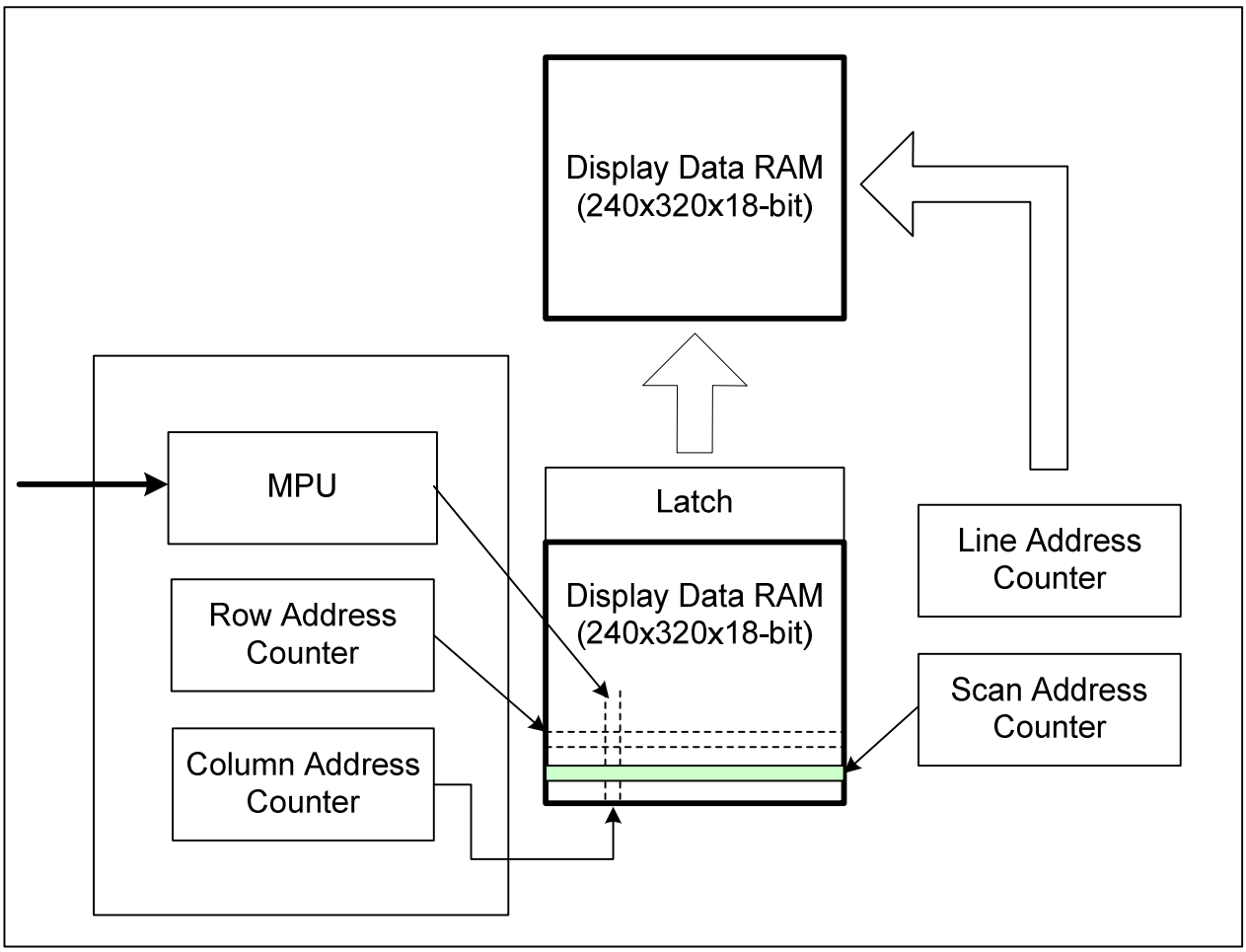
Default

Status	Default Value	
	SPI_READ_EN	SPI_CNT[3:0]
Power ON Sequence	1'b0	4'b0000
H/W Reset	1'b0	4'b0000

9. Display Data RAM

9.1. Configuration

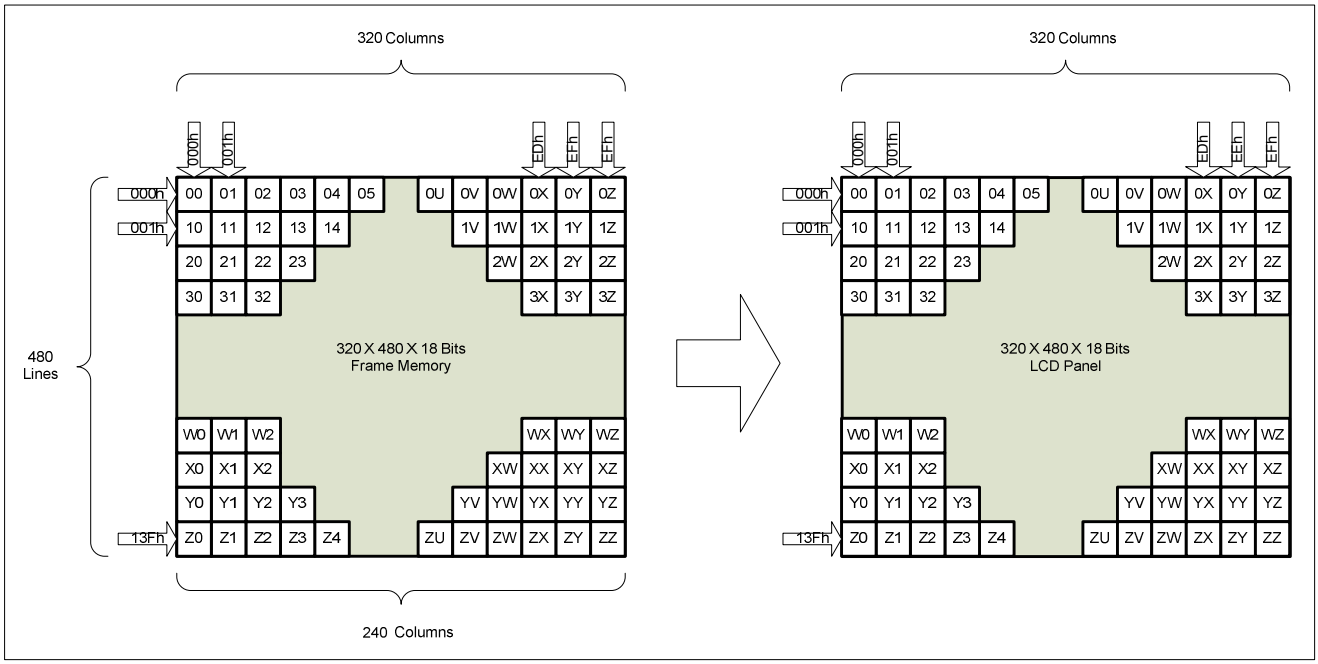
The display data RAM stores display dots and consists of 345,600 bits (320x480x18 bits). There is no restriction on access to the RAM even when the display data on the same address is loaded to DAC. There will be no abnormal visible effect on the display when there is a simultaneous Panel Read and Interface Read or Write to the same location of the Frame Memory.



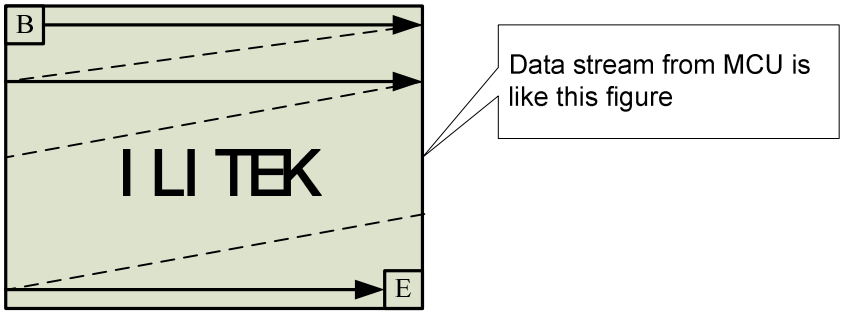
9.2. Memory to Display Address Mapping

In this mode, the content of the frame memory within an area where column pointer is 0000h to 013Fh and page pointer is 0000h to 01DFh is displayed.

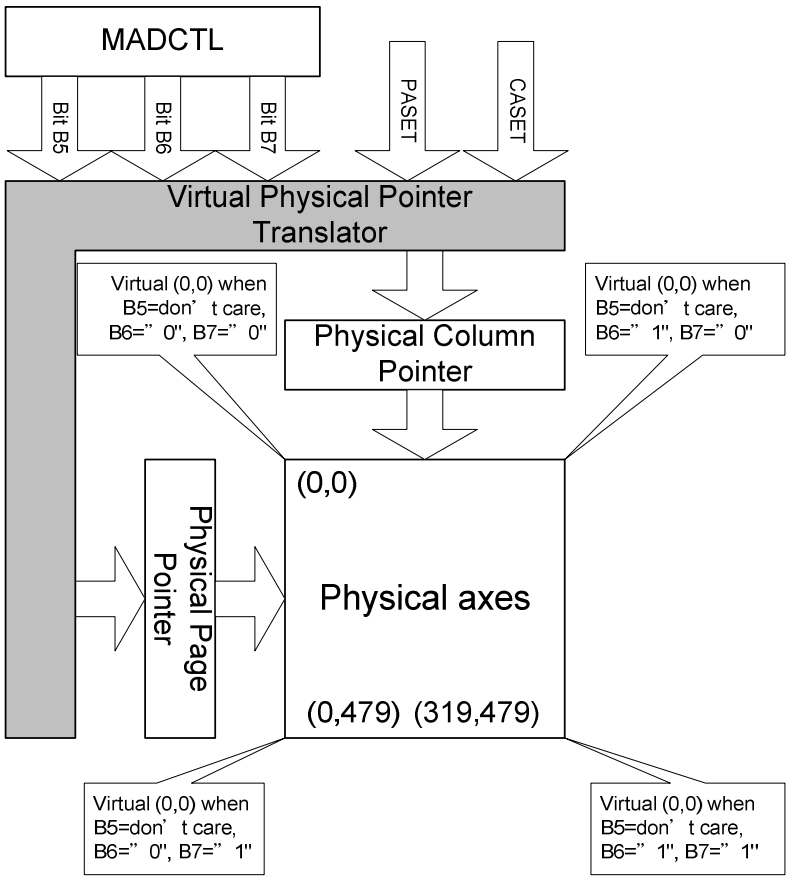
To display a dot on leftmost top corner, store the dot data at (column pointer, page pointer) = (0,0)



9.3. MCU to memory write/read direction



The data is written in the order illustrated above. The Counter which dictates where in the physical memory the data is to be written is controlled by “Memory Data Access Control” Command, Bits B5, B6, and B7 as described below.



B5	B6	B7	CASET	PASET
0	0	0	Direct to Physical Column Pointer	Direct to Physical Page Pointer
0	0	1	Direct to Physical Column Pointer	Direct to (479-Physical Page Pointer)
0	1	0	Direct to (319-Physical Column Pointer)	Direct to Physical Page Pointer
0	1	1	Direct to (319-Physical Column Pointer)	Direct to (479-Physical Page Pointer)
1	0	0	Direct to Physical Page Pointer	Direct to Physical Column Pointer
1	0	1	Direct to (479-Physical Page Pointer)	Direct to Physical Column Pointer
1	1	0	Direct to Physical Page Pointer	Direct to (319-Physical Column Pointer)
1	1	1	Direct to (479-Physical Page Pointer)	Direct to (319-Physical Column Pointer)

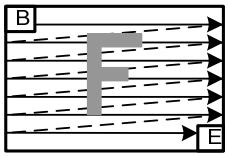
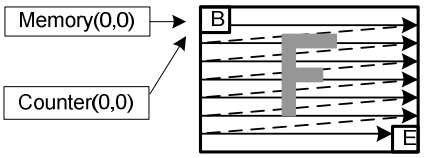
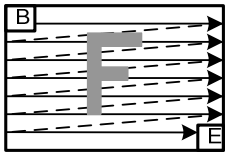
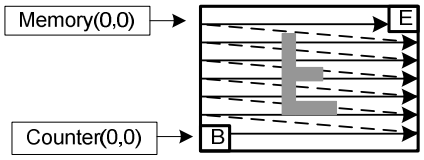
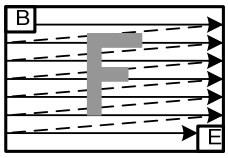
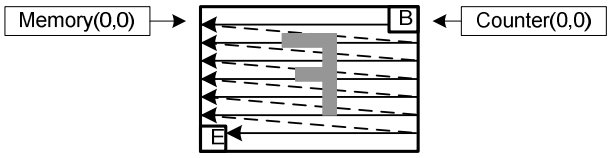
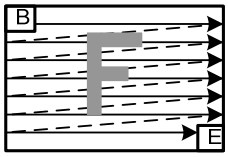
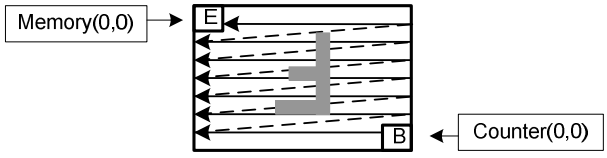
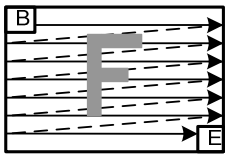
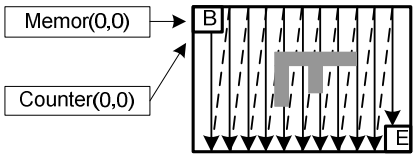
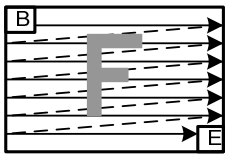
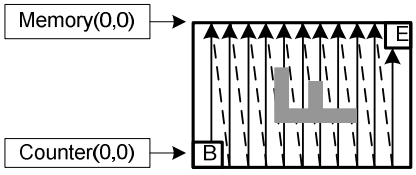
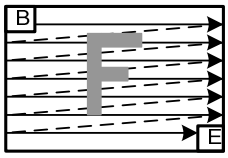
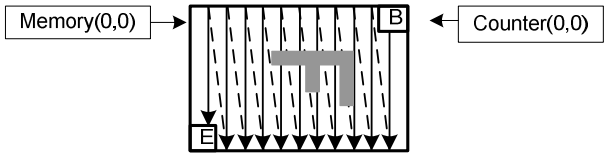
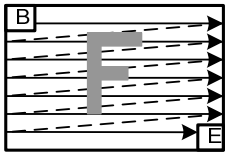
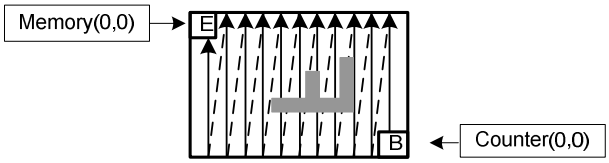
Condition	Column Counter	Page counter
When RAMWR/RAMRD command is accepted	Return to “Start column”	Return to “Start Page”
Complete Pixel Read/Write action	Increment by 1	No change
The Column values is large than “End Column”	Return to “Start column”	Increment by 1
The Page counter is large than “End Page”	Return to “Start column”	Return to “Start Page”

Note: Data is always written to the Frame Memory in the same order, regardless of the Memory Write Direction set by MADCTL bits B7, B6 and B5.

The write order for each pixel unit is

D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0

One pixel unit represents 1 column and 1 page counter value on the Frame Memory.

Display Data Direction	MADCTR Parameter			Image in the Memory (MPU)	Image in the Driver (Frame Memory)
	MV	MX	MY		
Normal	0	0	0		
Y-Mirror	0	0	1		
X-Mirror	0	1	0		
X-Mirror Y-Mirror	0	1	1		
X-Y Exchange	1	0	0		
X-Y Exchange Y-Mirror	1	0	1		
XY Exchange X-Mirror	1	1	0		
XY Exchange X-YMirror	1	1	1		

10. Tearing Effect Information

The Tearing Effect output supplies to the MCU a Panel synchronization information (= Tearing Effect Information) which is telling the position of the refreshing on the display panel, to the MCU which can decide when it can send image information to ILI9486 (Mainly used for a moving image e.g. video clips) that there can avoid the abnormal visual effect on the display panel of ILI9486.

This information can be enabled or disabled by the Tearing Effect Line Off & On commands. The mode of the Tearing Effect Signal is defined by the parameter of the Tearing Effect Line Off & On commands.

This Tearing Effect information can be sent in two different ways:

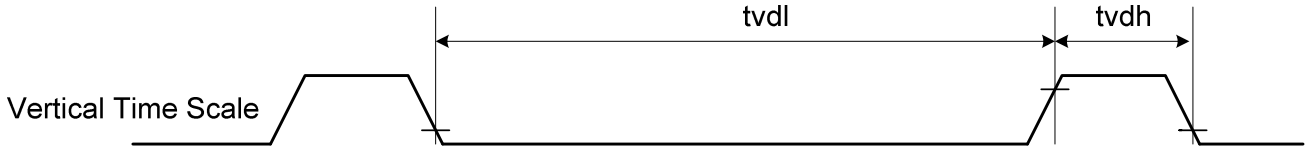
- Separated Line, which is so-called Tearing Effect (TE) line.
- Bus, which is so-called Tearing Effect (TEE) Bus Trigger, when ILI9486 is sending a trigger to the MCU.

The TE line is used in MCU parallel interface. The TE line can also be used in DSI case if the tearing Effect (TEE) Bus Trigger is not possible to use.The Tearing Effect (TEE) Bus Trigger is only used in DSI case.

10.1. Tearing Effect Line

10.1.1. Tearing Effect Line Modes

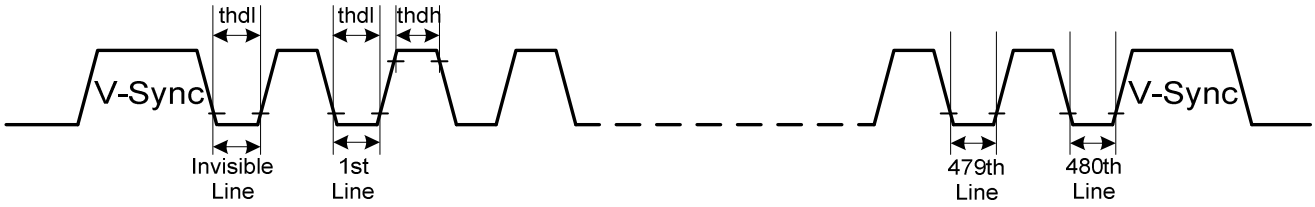
Mode 1, the Tearing Effect Output signal consists of V-Sync information only:



tvdh = The LCD display is not updated from the Frame Memory.

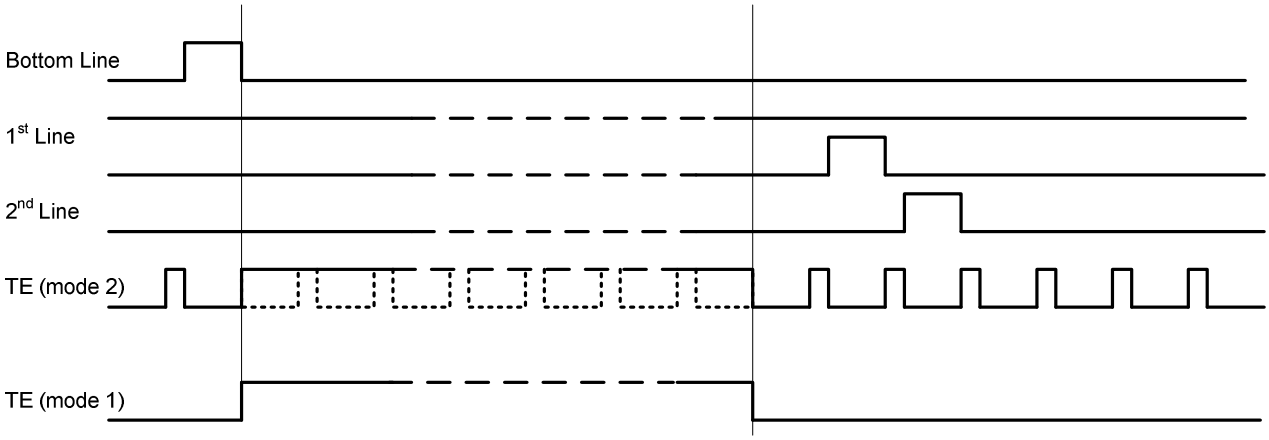
tvdl = The LCD display is updated from the Frame Memory (except Invisible Line – see below).

Mode 2, the tearing effect output signal consists of V-Sync and H-Sync information; there is one V-sync and 480 H-sync pulses per field:



thdh = The LCD display is not updated from the Frame Memory.

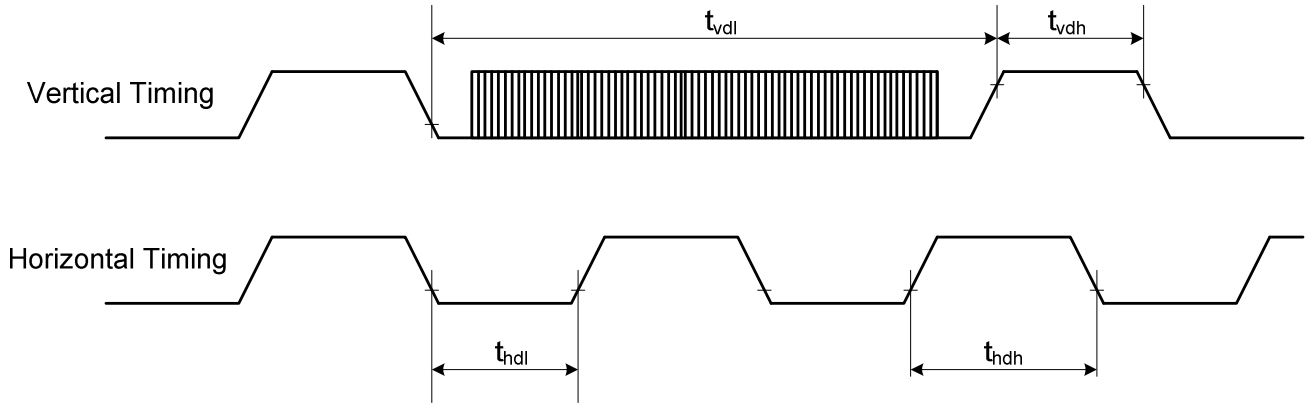
thdl = The LCD display is updated from the Frame Memory (except Invisible Line – see above).



Note: During Sleep In Mode, the Tearing Effect Output Pin is active Low.

10.1.2. Tearing Effect Line Timing

The tearing effect signal is described below:



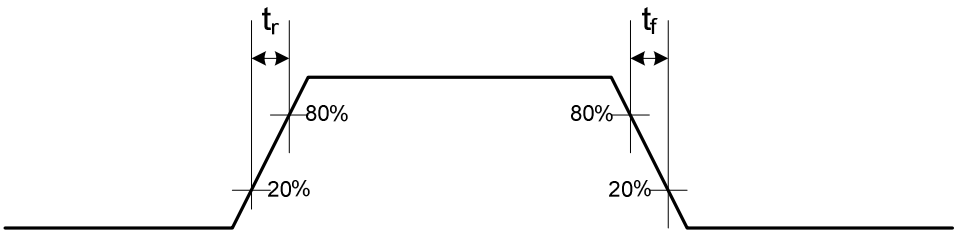
AC characteristics of Tearing Effect Signal (Frame Rate = 60.5Hz)

Symbol	Parameter	Min.	Max.	Unit	Description
t_{vdl}	Vertical timing low duration	TBD	TBD	ms	
t_{vdh}	Vertical timing high duration	1000	TBD	us	
t_{hdl}	Horizontal timing low duration	TBD	TBD	us	
t_{hdh}	Horizontal timing high duration	TBD	500	us	

Notes: 1. The timings in Table as above apply when MADCTL B4=0 and B4=1

2. Minimum frequency of the TE-line can not be less than 25Hz when the TE-line is active on Mode 1.

3. The signal's rise and fall times (tf, tr) are stipulated to be equal to or less than 15ns.



The Tearing Effect Output Line is fed back to the MCU and should be used to avoid Tearing Effect.

10.2. Tearing Effect Bus Trigger

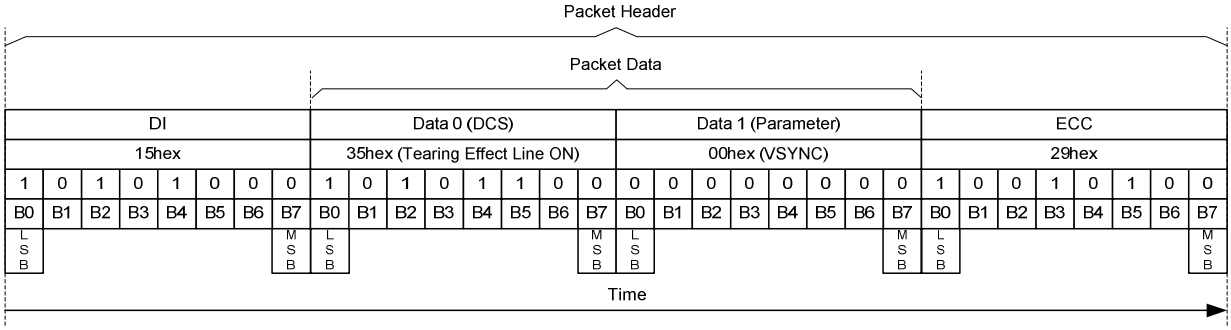
Tearing Effect Bus Trigger information supplies to the MCU a Panel synchronization trigger and this Tearing Effect Bus Trigger information can be enabled or disabled by “Tearing Effect Line Off (34h)” and “Tearing Effect Line On (35h)” commands when the only mode of the Tearing Effect Signal is VSYNC information.

The ILI9486 is sending this trigger information in Escape Mode after the Bus Turnaround (BTA) and the Tearing Effect Bus Trigger can only use in DSI case without the TE line.

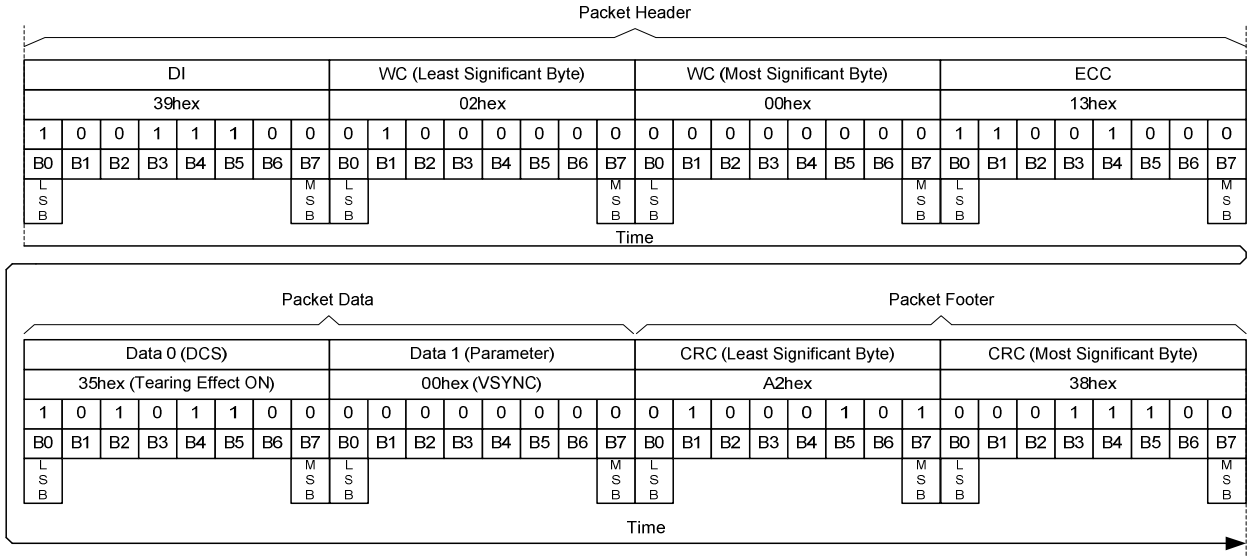
10.2.1. Tearing Effect Bus Trigger Enable

The MCU can enable the Tearing Effect Bus Trigger on ILI9486 in 2 different ways when a Short Packet (SPa) or Long Packet (LPa) is used. These cases are illustrated below.

Tearing Effect Bus Trigger Enable - Short Packet



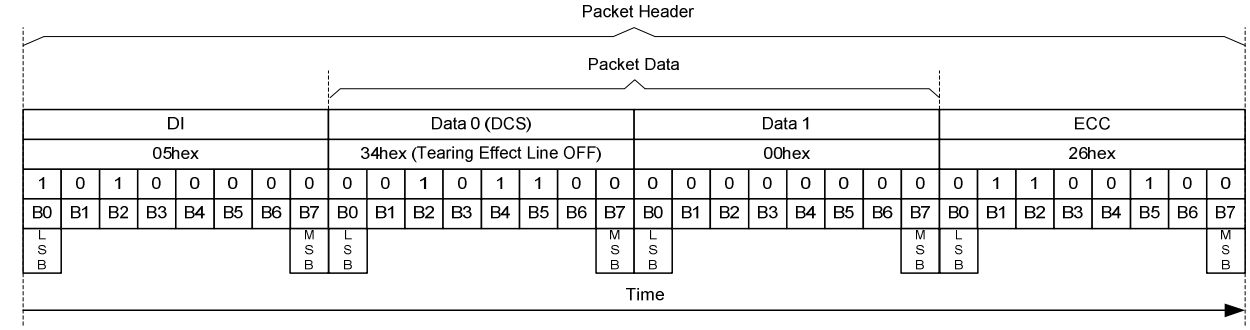
Tearing Effect Bus Trigger Enable - Long Packet



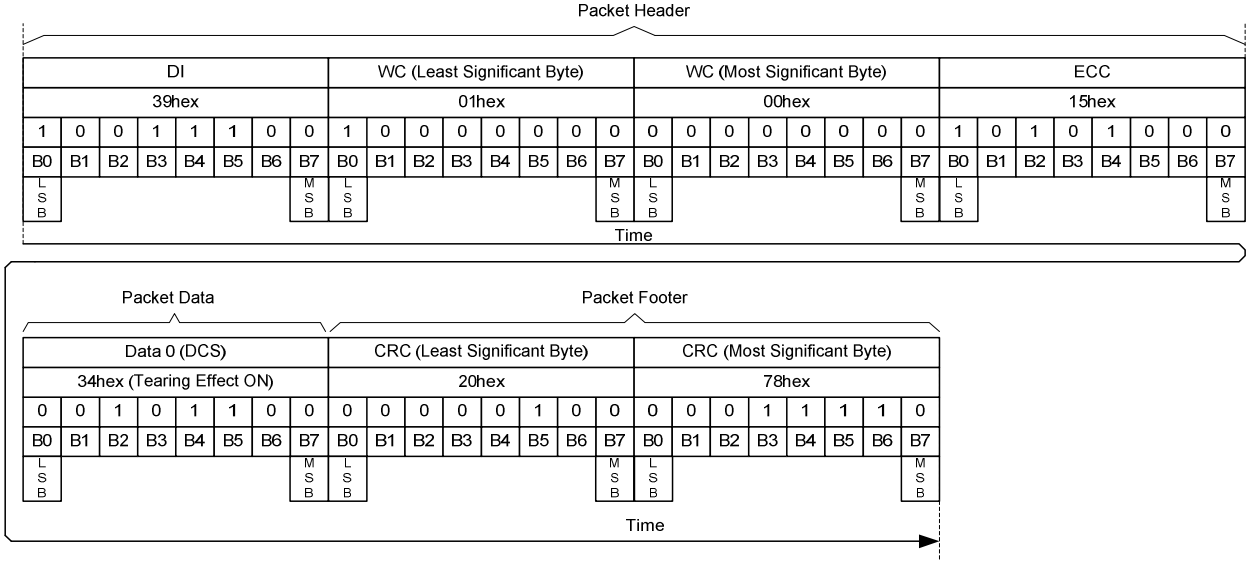
10.2.2. Tearing Effect Bus Trigger Disable

The MCU can enable the Tearing Effect Bus Trigger on ILI9486 in 2 different ways when a Short Packet (SPa) or Long Packet (LPa) is used. These both possibilities are illustrated below.

Tearing Effect Bus Trigger Disable - Short Packet



Tearing Effect Bus Trigger Disable - Long Packet



10.2.3. Tearing Effect Bus Trigger Sequences

Tearing Effect Bus Trigger Enable Sequence – DCS Write (Long Packet) and HSDT						
Line	MCU		Information Direction	Display Module		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	-	LP-11	→	-	-	Start
2	DCS Write (LPa)	HSDT	→	-	-	Tearing Effect Bus Trigger Enable
3	-	LP-11	→	-	-	
4	-	BTA	⇔	BTA	-	Interface Control Change from the MCU to ILI9486
5	-	-	←	LP-11	-	If No Error, then go to Line 7 If Error occurs, then go to Line 12
6						
7	-	-	←	TEE	-	TE (Escape Trigger) on the next VSYNC
8	-	-	←	LP-11	-	
9	-	BTA	⇔	BTA	-	Interface Control Change from ILI9486 to MCU
10	-	LP-11	→	-	-	End
11						
12	-	-	←	LPDT	Acknowledge Error Report	Error Report
13	-	-	←	LP-1	-	
14	-	BTA	⇔	BTA	-	
15	-	LP-11	→	-	-	End

Tearing Effect Bus Trigger Enable Sequence – DCS Write (Long Packet) and LPDT						
Line	MCU		Information Direction	Display Module		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	-	LP-11	→	-	-	Start
2	DCS Write (LPa)	LPDT	→	-	-	Tearing Effect Bus Trigger Enable
3	-	LP-11	→	-	-	
4	-	BTA	⇔	BTA	-	Interface Control Change from the MCU to ILI9486
5	-	-	←	LP-11	-	If No Error, then go to Line 7 If Error occurs, then go to Line 12
6						
7	-	-	←	TEE	-	TE (Escape Trigger) on the next VSYNC
8	-	-	←	LP-11	-	
9	-	BTA	⇔	BTA	-	Interface Control Change from ILI9486 to MCU
10	-	LP-11	→	-	-	End
11						
12	-	-	←	LPDT	Acknowledge Error Report	Error Report
13	-	-	←	LP-1	-	
14	-	BTA	⇔	BTA	-	
15	-	LP-11	→	-	-	End

Tearing Effect Bus Trigger Enable Sequence – DCS Write, 1 Parameter (Short Packet) and HSDT						
Line	MCU		Information Direction	Display Module		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	-	LP-11	→	-	-	Start
2	DCS Write (SPa)	HSDT	→	-	-	Tearing Effect Bus Trigger Enable
3	-	LP-11	→	-	-	
4	-	BTA	⇔	BTA	-	Interface Control Change from the MCU to ILI9486
5	-	-	←	LP-11	-	If No Error, then go to Line 7 If Error occurs, then go to Line 12
6						
7	-	-	←	TEE	-	TE (Escape Trigger) on the next VSYNC
8	-	-	←	LP-11	-	
9	-	BTA	⇔	BTA	-	Interface Control Change from ILI9486 to MCU
10	-	LP-11	→	-	-	End
11						
12	-	-	←	LPDT	Acknowledge Error Report	Error Report
13	-	-	←	LP-1	-	
14	-	BTA	⇔	BTA	-	
15	-	LP-11	→	-	-	End

Tearing Effect Bus Trigger Enable Sequence – DCS Write, 1 Parameter (Short Packet) and LPDT						
Line	MCU		Information Direction	Display Module		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	-	LP-11	→	-	-	Start
2	DCS Write (SPa)	LPDT	→	-	-	Tearing Effect Bus Trigger Enable
3	-	LP-11	→	-	-	
4	-	BTA	⇔	BTA	-	Interface Control Change from the MCU to ILI9486
5	-	-	←	LP-11	-	If No Error, then go to Line 7 If Error occurs, then go to Line 12
6						
7	-	-	←	TEE	-	TE (Escape Trigger) on the next VSYNC
8	-	-	←	LP-11	-	
9	-	BTA	⇔	BTA	-	Interface Control Change from ILI9486 to MCU
10	-	LP-11	→	-	-	End
11						
12	-	-	←	LPDT	Acknowledge Error Report	Error Report
13	-	-	←	LP-1	-	
14	-	BTA	⇔	BTA	-	
15	-	LP-11	→	-	-	End

Tearing Effect Bus Trigger Disable Sequence – DCS Write, No Parameter (Short Packet) and LPDT						
Line	MCU		Information Direction	Display Module		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	-	LP-11	→	-	-	Start
2	DCS Write (SPa)	LPDT	→	-	-	Tearing Effect Bus Trigger Disable
3	-	LP-11	→	-	-	End

Tearing Effect Bus Trigger Disable Sequence – DCS Write, No Parameter (Short Packet) and HSDT						
Line	MCU		Information Direction	Display Module		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	-	LP-11	→	-	-	Start
2	DCS Write (SPa)	HSDT	→	-	-	Tearing Effect Bus Trigger Disable
3	-	LP-11	→	-	-	End

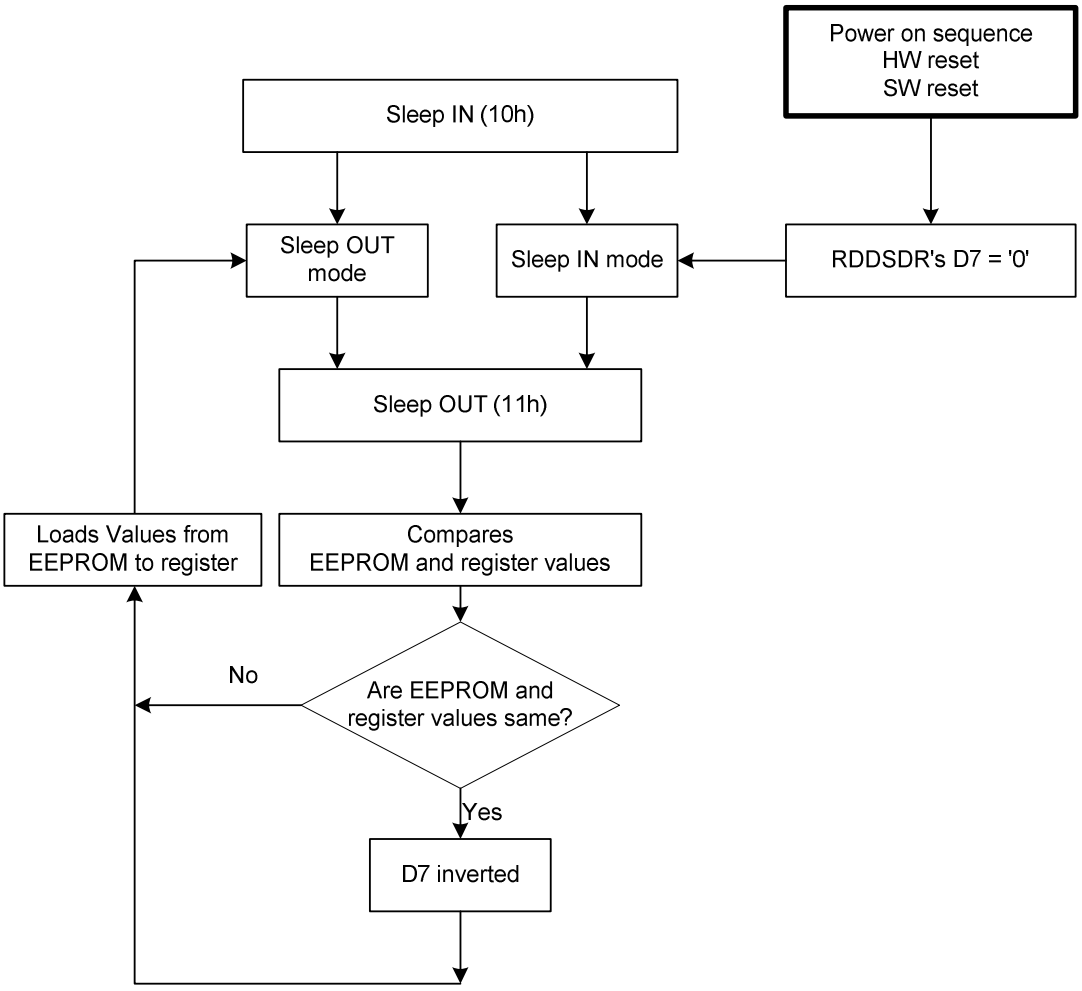
11. Sleep Out – Command and Self-Diagnostic Functions of ILI9486

11.1. Register loading Detection

Sleep Out-command (Command “Sleep Out (11h)”) is a trigger for an internal function of ILI9486, which indicates, if ILI9486 loading function of factory default values from EEPROM (or similar device) to registers of the display controller is working properly.

There are compared factory values of the EEPROM and register values of the display controller by the display controller (1st step: compares register and EEPROM values, 2nd step: loads EEPROM values to registers). If those both values (EEPROM and register values) are same, there is inverted (= increased by 1) a bit, which is defined in command “Read Display Self-Diagnostic Result (0Fh)” (= RDDSDR) (The used bit of this command is D7). If those both values are not same, this bit (D7) is not inverted (= not increased by 1).

The flow chart for this internal function is following:



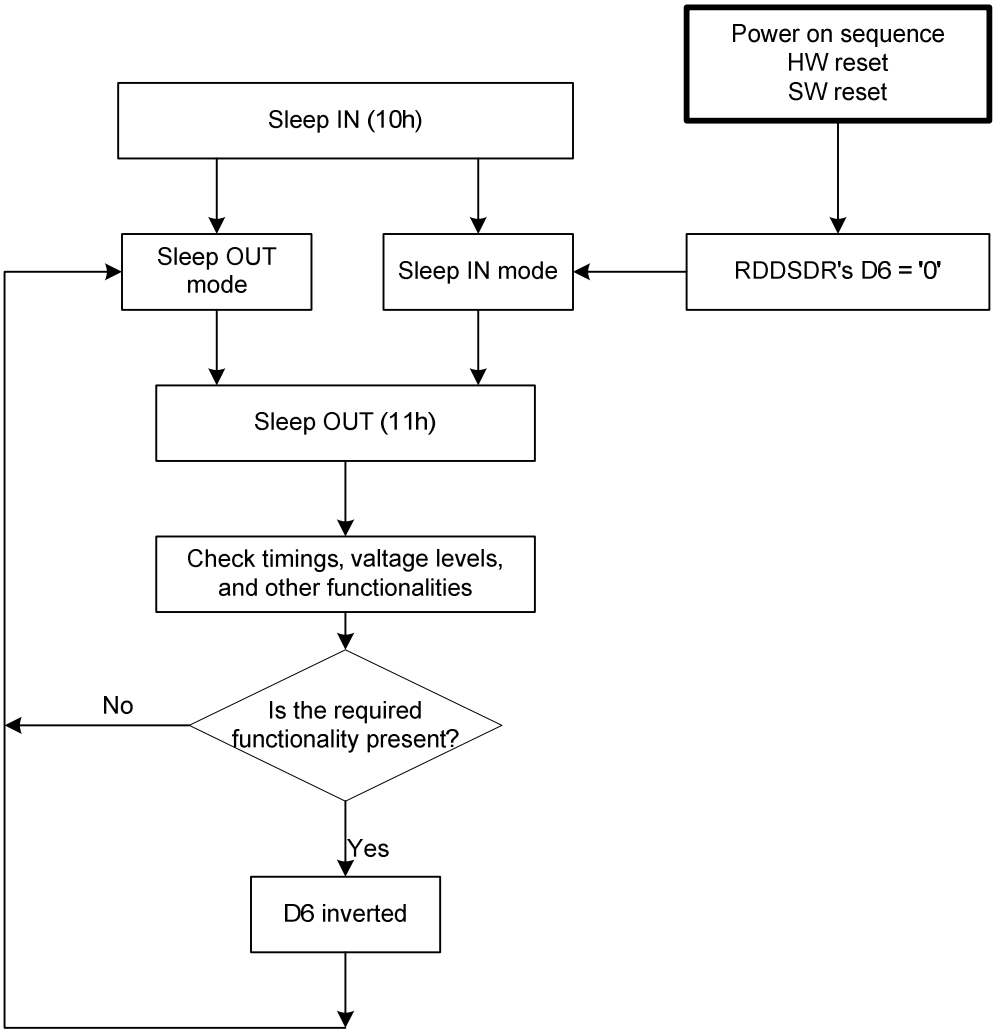
Note 1: There is not compared and loaded register values, which can be changed by User (User area commands: 00h to AFh and DAh to DDh), by ILI9486.

11.2. Functionality Detection

Sleep Out-command (Command “Sleep Out (11h)”) is a trigger for an internal function of ILI9486, which indicates, if ILI9486 is still running and meets functionality requirements.

The internal function (= the display controller) is comparing, if ILI9486 is still meeting functionality requirements (e.g. booster voltage levels, timings, etc.) If functionality requirement is met, there is an inverted (= increased by 1) bit, which defined in command “Read Display Self- Diagnostic Result (0Fh)” (= RDDSDR) (The used bit of this command is D6). If functionality requirement is not same, this bit (D6) is not inverted (= increased by 1). The flow chart for this internal function is shown as below.

The flow chart for this internal function is following:



Note 1: There is needed 120msec after Sleep Out -command, when there is changing from Sleep In –mode to Sleep Out -mode, before there is possible to check if User’s functionality requirements are met and a value of RDDSDR’s D6 is valid. Otherwise, there is 5msec delay for D6’s value, when Sleep Out –command is sent in Sleep Out -mode.

12. Power ON/OFF Sequence

IOVCC and VCI can be applied in any order. VCI and IOVCC can be powered down in any order. During power off, if LCD is in the Sleep Out mode, VCI and IOVCC must be powered down minimum 120msec after RESX has been released.

During power off, if LCD is in the Sleep In mode, IOVCC or VCI can be powered down minimum 0msec after RESX has been released.

Note 1: There will be no damage to ILI9486 if the power sequences are not met.

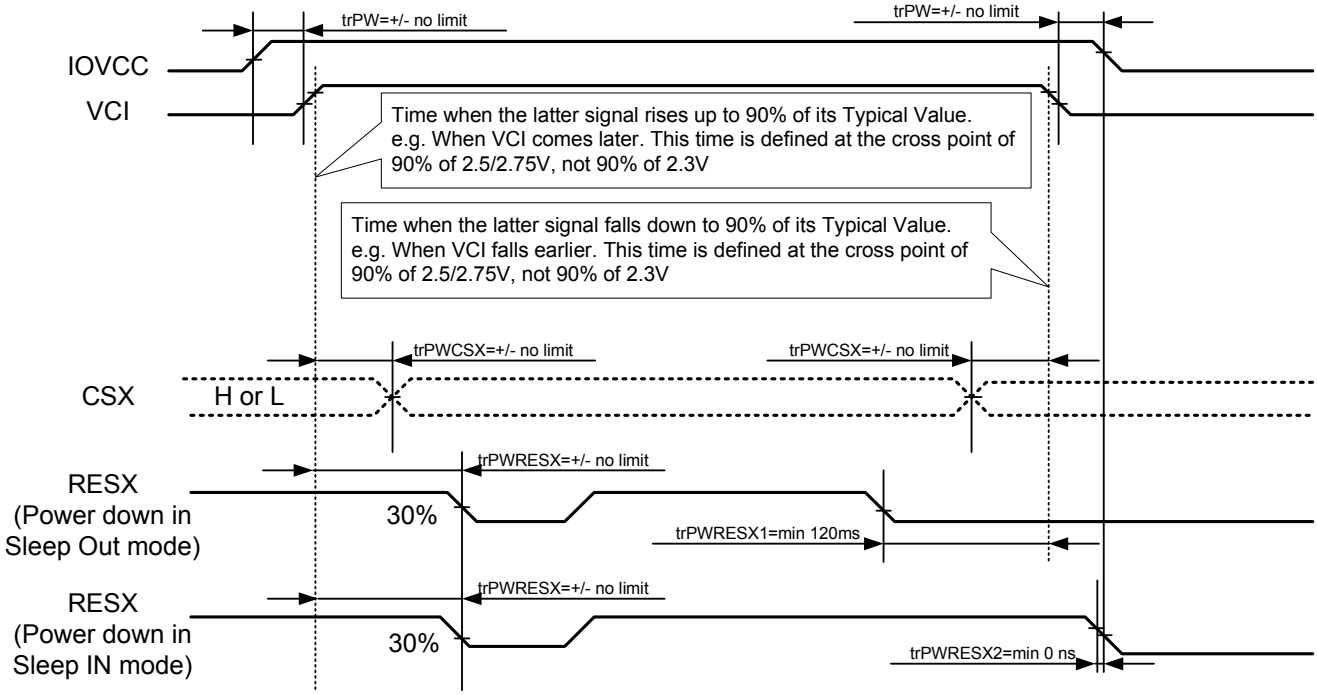
Note 2: There will be no abnormal visible effects on the display panel during the Power On/Off Sequences.

Note 3: There will be no abnormal visible effects on the display between end of Power On Sequence and before receiving Sleep Out command. Also between receiving Sleep In command and Power Off Sequence.

Note 4: If RESX line is not held stable by host during Power On Sequence as defined in Sections 12.1 and 12.2, then it will be necessary to apply a Hardware Reset (RESX) after Host Power On Sequence is complete to ensure correct operation. Otherwise function is not guaranteed.

12.1. Case 1 – RESX line is held High or Unstable by Host at Power ON

If RESX line is held High or unstable by the host during Power On, then a Hardware Reset must be applied after both VCI and IOVCC have been applied – otherwise correct functionality is not guaranteed. There is no timing restriction upon this hardware reset.



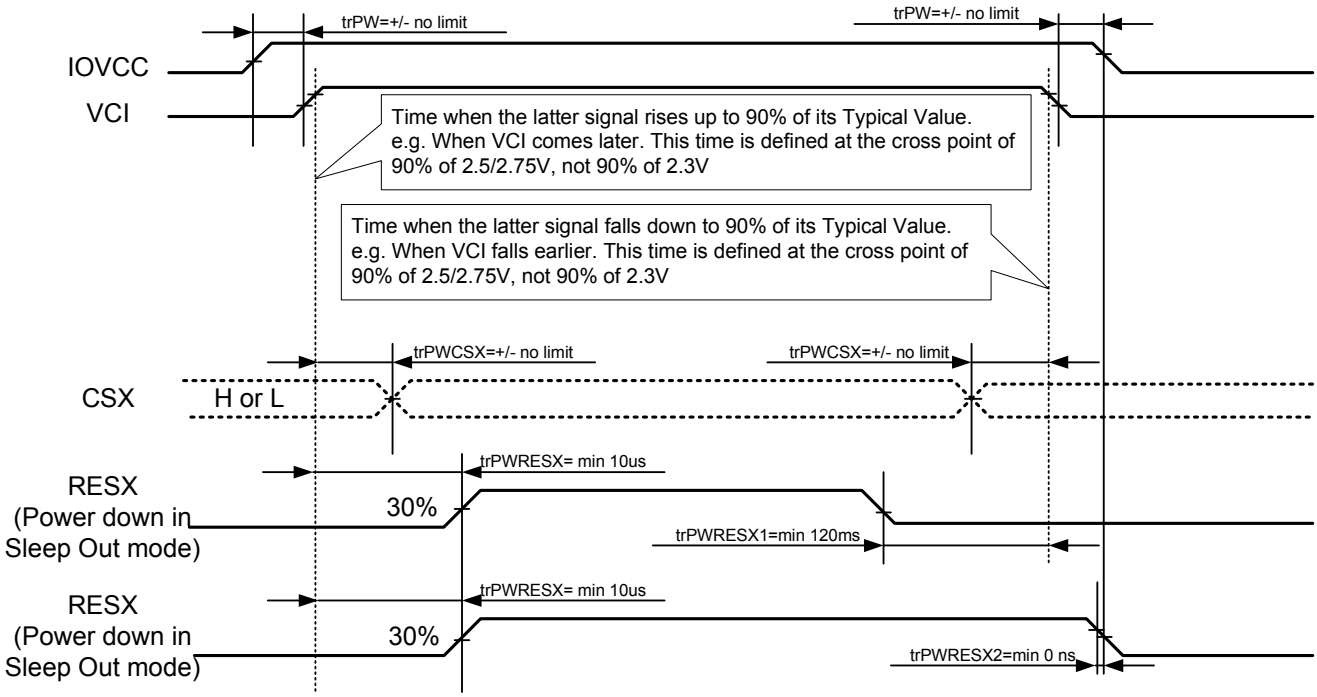
trPWRESX1 is applied to RESX falling in the Sleep Out Mode
trPWRESX2 is applied to RESX falling in the Sleep In Mode

Note 1: Unless otherwise specified, timings herein show cross point at 50% of signal power level.

12.2. Case 2 – RESX line is held Low by Host at Power ON

If RESX line is held Low (and stable) by the host during Power On, then the RESX must be held low for minimum

10µsec after both VCI and IOVCC have been applied.



trPWRESX1 is applied to RESX falling in the Sleep Out Mode
trPWRESX2 is applied to RESX falling in the Sleep In Mode

Note 1: Unless otherwise specified, timings herein show cross point at 50% of signal power level.

12.3. Uncontrolled Power Off

The uncontrolled power off means a situation when e.g. there is removed a battery without the controlled power off sequence. There will not be any damages for ILI9486 or ILI9486 will not cause any damages for the host or lines of the interface. At an uncontrolled power off event, ILI9486 will force the display to blank and will not be any abnormal visible effects with in 1 second on the display and remains blank until “Power On Sequence” powers it up.

13. Power Level Definition

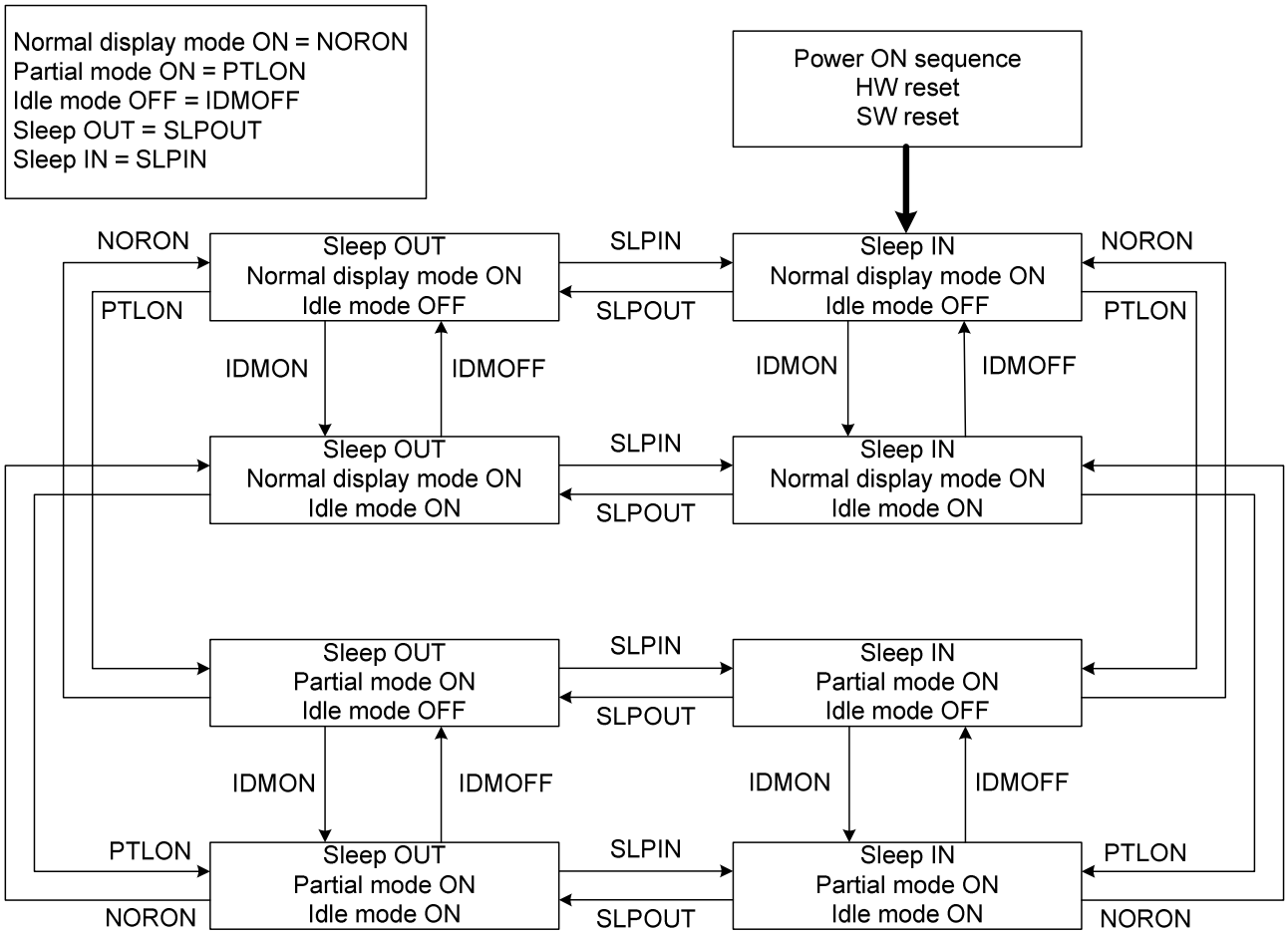
13.1. Power Levels

6 level modes are defined they are in order of Maximum Power consumption to Minimum Power Consumption:

1. Normal Mode On (full display), Idle Mode Off, Sleep Out.
   In this mode, the display is able to show maximum 262,144 colors.
2. Partial Mode On, Idle Mode Off, Sleep Out.
   In this mode part of the display is used with maximum 262,144 colors.
3. Normal Mode On (full display), Idle Mode On, Sleep Out.
   In this mode, the full display area is used but with 8 colors.
4. Partial Mode On, Idle Mode On, Sleep Out.
   In this mode, part of the display is used but with 8 colors.
5. Sleep In Mode.
   In this mode, the DC:DC converter, Internal oscillator and panel driver circuit are stopped. Only the MCU interface and memory works with IOVCC power supply. Contents of the memory are safe.
6. Power Off Mode.
   In this mode, both VCI and IOVCC are removed.

Note1: Transition between modes 1-5 is controllable by MCU commands. Mode 6 is entered only when both Power supplies are removed.

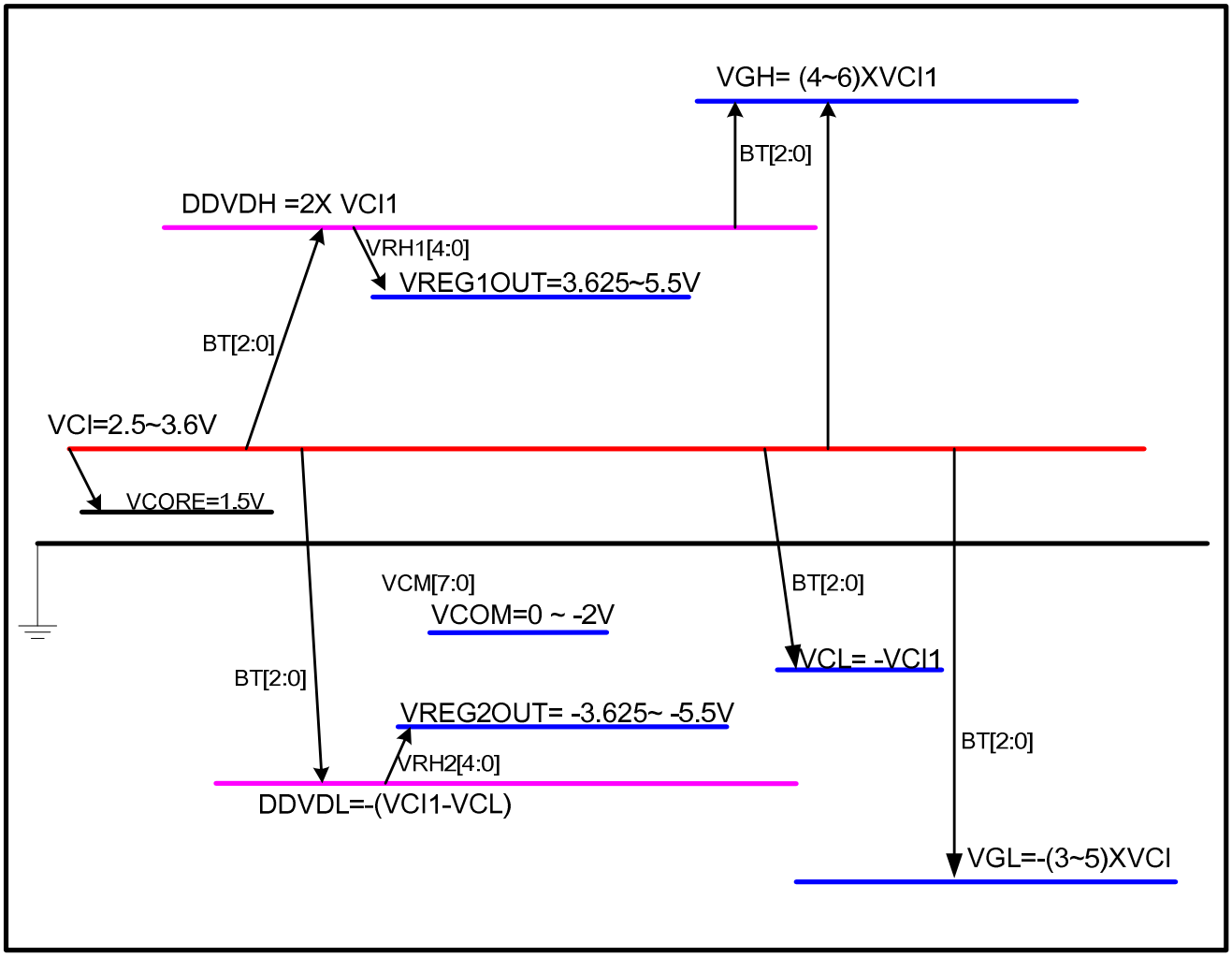
13.2. Power Flow Chart



Note 1: There is not any abnormal visual effect when there is changing from one power mode to another power mode.

Note 2: There is not any limitation, which is not specified by User, when there is changing from one power mode to another power mode.

13.3. LCM Voltage Generation



14. Reset

14.1. Registers

The registers that are initialized are listed as below:

Register	After Powered ON	After Hardware Reset	After Software Reset
Frame Memory	Random	Random	Random
Sleep	In	In	In
Display Mode	Normal	Normal	Normal
Display Status	Display Off	Display Off	Display Off
Idle Mode	Off	Off	Off
Column Start Address	0000 h	0000 h	0000 h
Column End Address	013F h	013F h	013F h
Page Start Address	0000 h	0000 h	0000 h
Page End Address	01F h	013F h	013F h
Gamma Setting	GC0	GC0	GC0
Partial Area Start	0000 h	0000 h	0000 h
Partial Area End	01DF h	01DF h	01DF h
Memory Data Access Control	00 h	00 h	00h
RDNUMED	00 h	00 h	00h
RDDPM	08 h	08 h	08 h
RDDMADCTL	00 h	00 h	00 h
RDDCOLMOD	07 h	07 h	07 h
RDDIM	00 h	00 h	00 h
RDDSM	00 h	00 h	00 h
RDDSDR	00 h	00 h	00 h
RDDISBV	00 h	00 h	00 h
RDCTRLD	00 h	00 h	00 h
RDCABC	00 h	00 h	00 h
RDCABCMB	00 h	00 h	00 h
TE Output Line	Off	Off	Off
TE Line Mode	Mode 1 (Note 3)	Mode 1 (Note 3)	Mode 1 (Note 3)

Note 1: There will be no abnormal visible effects on the display when S/W or H/W Resets are applied.

Note 2: After Powered-On Reset finishes within 10µs after both VCI & IOVCC are applied.

Note 3: Mode 1 means Tearing Effect Output Line consists of V-Blanking Information only.

14.2. Output Pins, I/O Pins

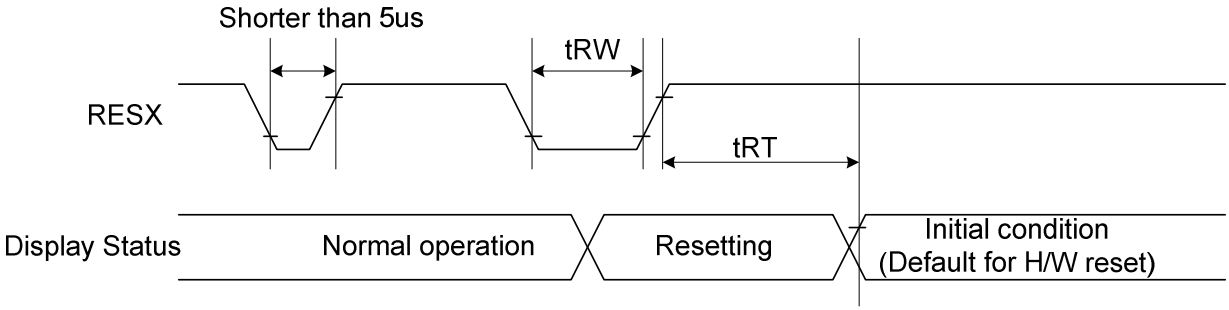
	After Power ON	After Hardware Reset	After Software Reset
TE line	Low	Low	Low
DB[17:0] (output driver), SDA	Hi-Z (Inactive)	Hi-Z (Inactive)	Hi-Z (Inactive)

Note 1: There will be no output from DB[17:0] during Power ON/OFF sequence, hardware reset and software reset.

14.3. Input Pins

	During Power ON Process	After Power ON	After Hardware Reset	After Software Reset	During Power OFF Process
RESX	See Chapter 12	Input valid	Input valid	Input valid	See Chapter 12
CSX	Input invalid	Input valid	Input valid	Input valid	Input invalid
D/CX	Input invalid	Input valid	Input valid	Input valid	Input invalid
WRX	Input invalid	Input valid	Input valid	Input valid	Input invalid
RDX	Input invalid	Input valid	Input valid	Input valid	Input invalid
RWX	Input invalid	Input valid	Input valid	Input valid	Input invalid
SCL	Input invalid	Input valid	Input valid	Input valid	Input invalid
DB[17:0] (input driver), SDA	Input invalid	Input valid	Input valid	Input valid	Input invalid

14.4. Reset Timing



Signal	Symbol	Parameter	Min	Max	Unit
RESX	tRW	Reset pulse duration	10		uS
	tRT	Reset cancel		5 (note 1,5)	mS
				120 (note 1,6,7)	mS

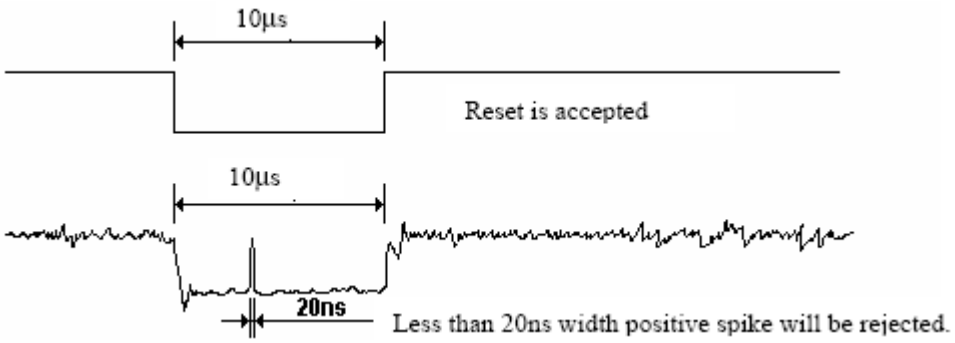
Note 1: The reset cancel includes also required time for loading ID bytes, VCOM setting and other settings from EEPROM to registers. This loading is done every time when there is HW reset cancel time (tRT) within 5 ms after a rising edge of RESX.

Note 2: Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below:

RESX Pulse	Action
Shorter than 5us	Reset Rejected
Longer than 9us	Reset
Between 5us and 9us	Reset starts

Note 3: During the Resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display remains the blank state in Sleep In -mode.) and then return to Default condition for Hardware Reset.

Note 4: Spike Rejection also applies during a valid reset pulse as shown below:

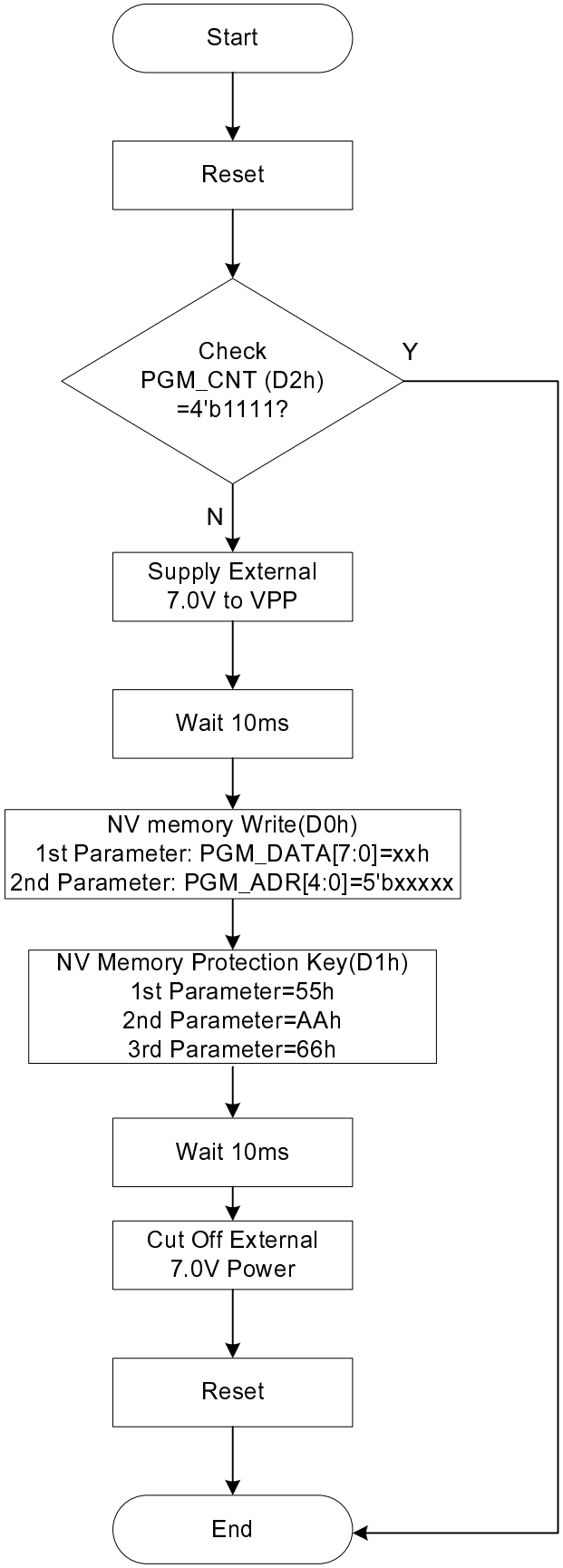


Note 5: When Reset applied during Sleep In Mode.

Note 6: When Reset applied during Sleep Out Mode.

Note7: It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec.

15. NV Memory Programming Flow



16. Gamma Correction

TBD

17. Electrical Characteristics

17.1. Absolute Maximum Ratings

The absolute maximum rating is listed on following table. When ILI9486 is used out of the absolute maximum ratings, the ILI9486 may be permanently damaged. To use the ILI9486 within the following electrical characteristics limit is strongly recommended for normal operation. If these electrical characteristic conditions are exceeded during normal operation, the ILI9486 will malfunction and cause poor reliability.

Item	Symbol	Unit	Value
Supply voltage	VCI	V	-0.3 ~ +5.0
Supply voltage (Logic)	IOVCC	V	-0.3 ~ +4.6
Supply voltage (Digital)	VCORE	V	-0.3 ~ +2.4
Driver supply voltage	VGH-VGL	V	-0.3 ~ +33.0
Logic input voltage range	VIN	V	-0.3 ~ IOVCC + 0.3
Logic output voltage range	VOUT	V	-0.3 ~ IOVCC + 0.3
Operating temperature	Topr	℃	-40 ~ +85
Storage temperature	Tstg	℃	-55 ~ +110
Notes:If the absolute maximum rating of even is one of the above parameters is exceeded even momentarily, the quality of the product may be degraded. Absolute maximum ratings, therefore, specify the values exceeding which the product may be physically damaged. Be sure to use the product within the range of the absolute maximum ratings.			

17.2. DC Characteristics

DSI is using different state codes which are depending on DC voltage levels of the clock and data lanes. The meaning of the state codes is defined on the following table.

State Code	Line DC Voltage Levels	
	CLOCK_P or DATA_N	CLOCK_N or DATA_P
HS-0	Low (HS)	High (HS)
HS-1	High (HS)	Low (HS)
LP-00	Low (LP)	Low (LP)
LP-01	Low (LP)	High (LP)
LP-10	High (LP)	Low (LP)
LP-11	High (LP)	Low (LP)

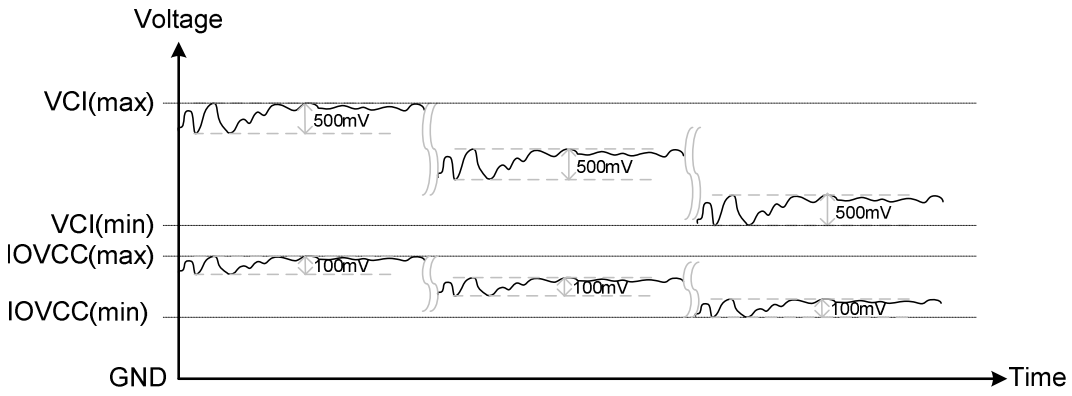
Note: Ta=-30℃ to 70℃ (to +85℃ no damage)

17.2.1. DC characteristics for Power Lines

Parameter	Symbol	Condition	Specification			Unit
			Min.	Typ.	Max.	
Analog power supply voltage	V_{CI}	Operating voltage	2.5	3.7	4.8	V
Digital power supply voltage	V_{IOVCC}	I/O supply voltage	1.65	1.8	1.95	V
Analog power supply voltage noise	V_{CI_NOISE}	Noise window, 0 to 100MHz	-	-	500	mV
Digital power supply voltage noise	V_{IOVCC_NOISE}	Noise window, 0 to 100MHz	-	-	500	mV

Note 1: Ta=-30℃ to 70℃ (to +85℃ no damage)

Note 2: These values are not symmetric amplitude, which centre points are IOVCC or VCI. See examples as reference purposes, when VCI_NOISE and IOVCC_NOISE are maximums, below.



17.2.2. DC characteristics for DSI LP mode

DC levels of the LP-00, LP-01, LP-10 and LP-11 are defined on table below: DC Characteristics for DSI LP mode when LP-RX, LP-CD or LP-TX is mentioned on the condition column. Other logical levels of the table are for MCU interface.

Parameter	Symbol	Condition	Specification			Unit
Logic High level output voltage	V_{OH}	I_{OUT}=-1mA ; Note 2	0.8 V_{IOVCC}	-	V_{IOVCC}	V
Logic Low level output voltage	V_{OL}	I_{OUT}=-1mA ; Note 2	0.0	-	0.2V_{IOVCC}	V
Logic High level input voltage	V_{IHLPCD}	LP-CD ; Note 3	450	-	1350	mV
Logic Low level input voltage	V_{ILLPCD}	LP-CD ; Note 3	0.0	-	200	mV
Logic High level input voltage	V_{IHLPRX}	LP-RX (CLOCK, DATA) ; Note 3	880	-	1350	mV
Logic Low level input voltage	V_{ILLPRX}	LP-RX (CLOCK, DATA) ; Note 3	0.0	-	550	mV
Logic Low level input voltage	$V_{ILLPRXULP}$	LP-RX (CLOCK ULP mode), Note 3	0.0	-	300	mV
Logic high level output voltage	V_{OHLPTX}	LP-TX (DATA), Note 3	1.1	-	1.3	V
Logic Low level output voltage	V_{OLLPTX}	LP-TX (DATA), Note 3	-50	-	50	mV
Logic High level input current	I_{IH}	LP-CD, LP-RX, Note 3	-	-	10	uA
Logic Low level input current	I_{IL}	LP-CD, LP-RX, Note 3	-10	-	-	uA

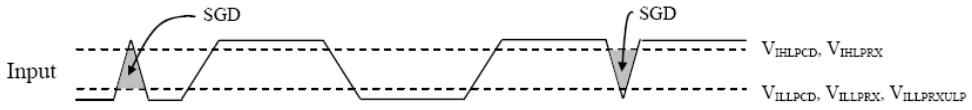
Note: (1) Ta=-30℃ to 70℃ (to +85℃ no damage)

(2) PWM_OUT, TE

(3) DSI High Speed mode is off

17.2.3. Spike / Glitch Rejection

Spike / Glitch Rejection – DSI					
Signal	Symbol	Parameter	Min	Max	Unit
Input (DSI-CLOCK_P/N, DSI-CLOCK_P/N)	SGD	Input pulse rejection for DSI	--	300	Vps



17.2.4. DC Characteristics for DSI HS mode

DC levels of the HS-0 and HS-0 are defined on table below: DC Characteristics for DSI HS mode.

Parameter	Symbol	Condition	Specification			Unit
Input Common Mode Voltage for Clock	V_{CMCLK}	DSI-CLOCK_P/N ; Note 2,3	70	-	330	mV
Input Common Mode Voltage for Data	V_{CMDATA}	DSI-DATA_P/N ; Note 2,3	70	-	330	mV
Common Mode Ripple for Clock Equal or Less than 450MHz	$V_{CMRCLKL450}$	DSI-CLOCK_P/N ; Note 4	-50	-	50	mV
Common Mode Ripple for Data Equal or Less than 450MHz	$V_{CMRDATAL450}$	DSI-DATA_P/N ; Note 4	-50	-	50	mV
Common Mode Ripple for Clock More than 450MHz (peak sine wave)	$V_{CMRCLKM450}$	DSI-CLOCK_P/N	-	-	100	mV
Common Mode Ripple for Data More than 450MHz (peak sine wave)	$V_{CMRDATAM450}$	DSI-DATA_P/N	-	-	100	mV
Differential Input Low Level Threshold Voltage for Clock	$V_{THLCLK-}$	DSI-CLOCK_P/N	-70	-	-	mV
Differential Input Low Level Threshold Voltage for Data	$V_{THLDATA-}$	DSI-DATA_P/N	-70	-	-	mV
Differential Input High Level Threshold Voltage for Clock	$V_{THHCLK+}$	DSI-CLOCK_P/N	-	-	70	mV
Differential Input High Level Threshold Voltage for Data	$V_{THHDATA+}$	DSI-DATA_P/N	-	-	70	mV
Single-ended Input Low Voltage	V_{ILHS}	DSI-CLOCK_P/N, DSI-DATA_P/N ; Note 3	-40	-	-	mV
Single-ended Input High Voltage	V_{IHHS}	DSI-CLOCK_P/N, DSI-DATA_P/N ; Note 3	-	-	460	mV
Differential Termination Resistor	R_{TERM}	DSI-CLOCK_P/N, DSI-DATA_P/N	80	100	125	Ω
Single-ended Threshold Voltage for Termination Enable	$V_{TERM-EN}$	DSI-CLOCK_P/N, DSI-DATA_P/N	-	-	450	mV
Termination Capacitor	C_{TERM}	DSI-CLOCK_P/N, DSI-DATA_P/N	-	-	14	pF

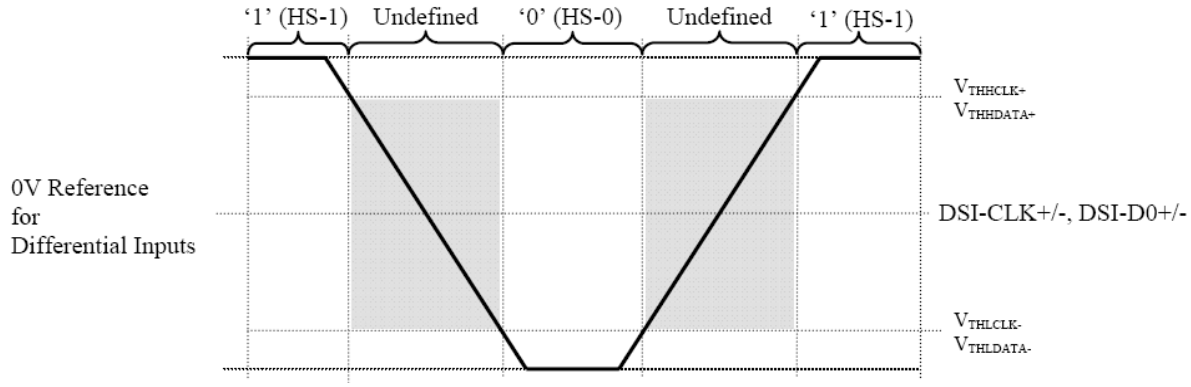
Note: (1) Ta = -30 to 70 ℃ (to +85 ℃ no damage), IOVCC = 1.65 to 1.95V, GND = 0V

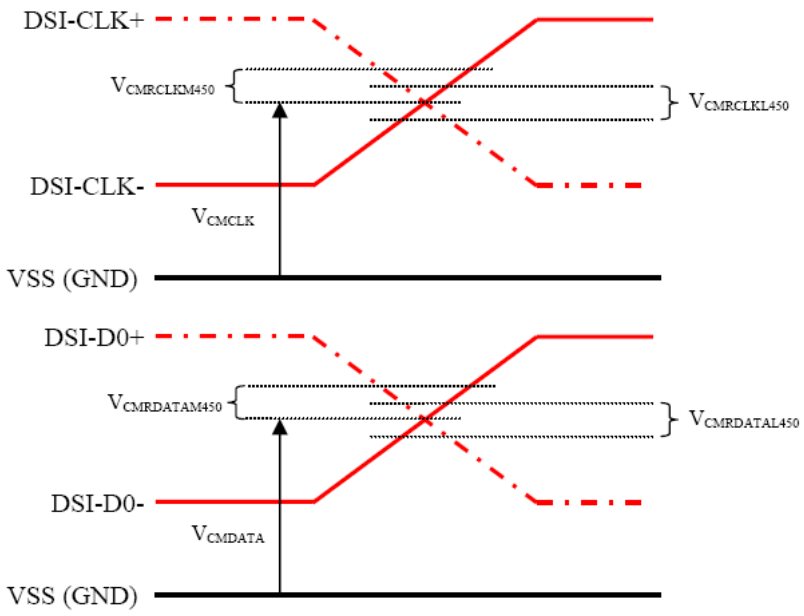
(2) Includes 50mV (-50mV to 50mV) ground difference

(3) Without VCMRCLKM450/VCMRDATAM450

(4) Without 50mV (-50mV to 50mV) ground difference

The DSI receiver (HS mode) is understanding that there is logical '1' (HS-1) when a differential voltage is more than VTHH (CLK+/DATA+) and the DSI receiver (HS mode) is understanding that there is logical '0' (HS-0) when a differential voltage is more than VTHL (CLK-/DATA-). There is undefined state if the differential voltage is less than VTHH (CLK+/DATA+) and less than VTHL (CLK-/DATA-). A reference figure is below.

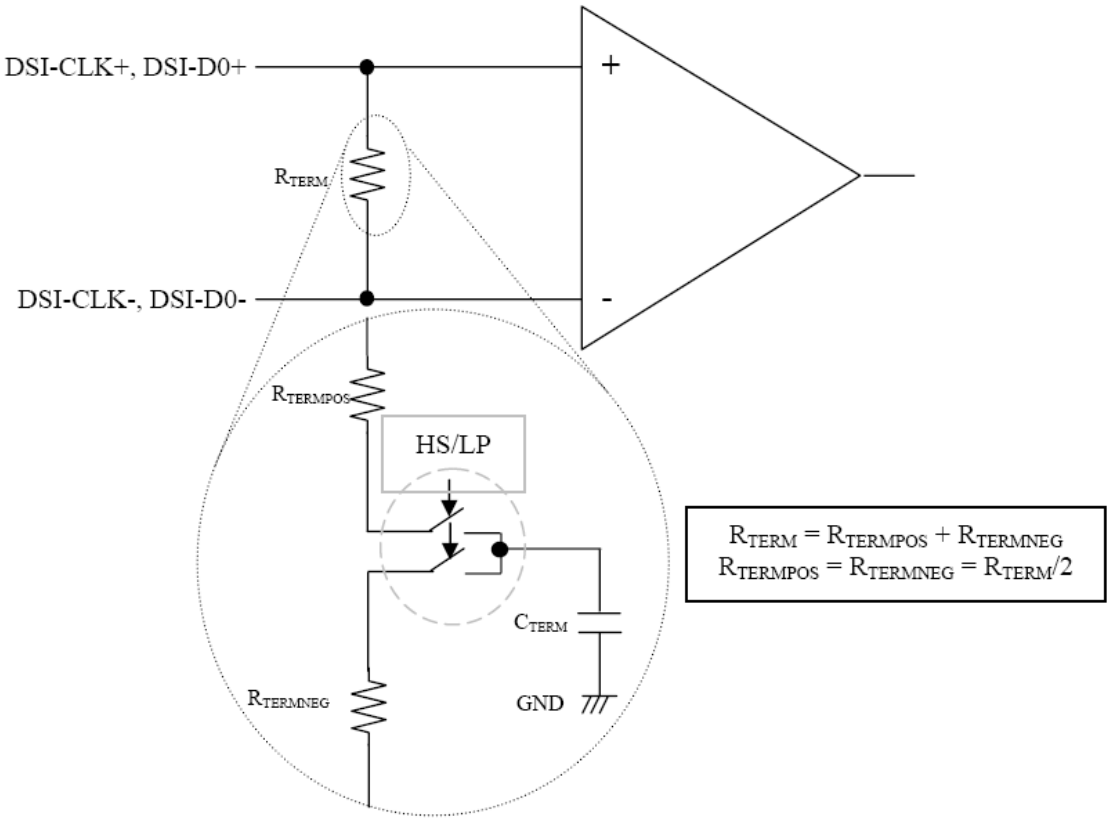




The termination resistor (RTERM) of the differential DSI receiver can be driven two different states by the receiver:

- Low Power (LP) mode when the termination resistor is not connected between differential inputs DSI-CLK+ <=> DSI-CLK- or DSI-D0+ <=> DSI-D0-)
- High Speed (HS) mode when the termination resistor is connected between differential inputs (DSI-CLK+ <=> DSI-CLK- or DSI-D0+ <=> DSI-D0-)

The termination switch (HS/LP), when the termination resistor is not connected, is illustrated below.



17.2.5. DC Characteristics for Panel Driving

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Power & Operation Voltage							
Analog operating voltage	VCI	-	2.5	2.8	3.6	V	
Logic operating voltage	IOVCC	-	1.65	2.8	3.6	V	
Digital operating voltage	VCORE	Digital block power supply	-	1.5	-	V	Note2
Gate Driver High Voltage	VGH	-	10.0	-	16.0	V	Note3
Gate Driver Low Voltage	VGL	-	-16.0	-	-9.0	V	Note3
Driver Supply Voltage	-	|VGH-VGL|	19	-	32	V	Note3
VCOM Operation							
VCOM Amplitude Voltage	VCOM	-	0	-	-2.0	V	Note3
Source Driver							
Source Output Range	Vsout	-	0.1	-	VREG1OUT-0.1	V	Note4
Positive Gamma Reference Voltage	VREG1OUT	-	3.6	-	5.5	V	Note3
Negative Gamma Reference Voltage	VREG2OUT		-5.5		-3.6	V	Note3
Source Output Setting Time	Tr	Below with 99% precision	-	15	20	uS	Note4,5
Output Deviation Voltage (Source Output channel)	Vdev	Sout>=4.2V Sout<=0.8V	-	-	20	mV	Note4
		4.2V>Sout>0.8V	-	-	15	mV	-
Output Offset Voltage	VOFSET	-	-	-	35	mV	Note6
Booster Operation							
1st Booster (VCI1x2) Voltage	DDVDH	-	4.5	-	6.0	V	Note3
1st Booster (VCI1x2) Voltage	DDVDL	-	-6.0	-	-4.5	V	Note3
1st Booster (VCI1x2 Drop Voltage	VCI1x2 drop	loading=1mA	-	-	5	%	Note3
Liner Range	Vliner	-	0.2	-	DDVDH-0.2	V	

Note 1: IOVCC=1.65 to 3.6V, VCI=2.5 to 3.6V, AGND=DGND=0V, Ta=-30 to 70 (to +85 no damage) ℃.

Note2: Please supply digital IOVCC voltage equal or less than analog VCI voltage.

Note2, 3, 4: When the measurements are performed with LCD module. Measurement Points are like below.

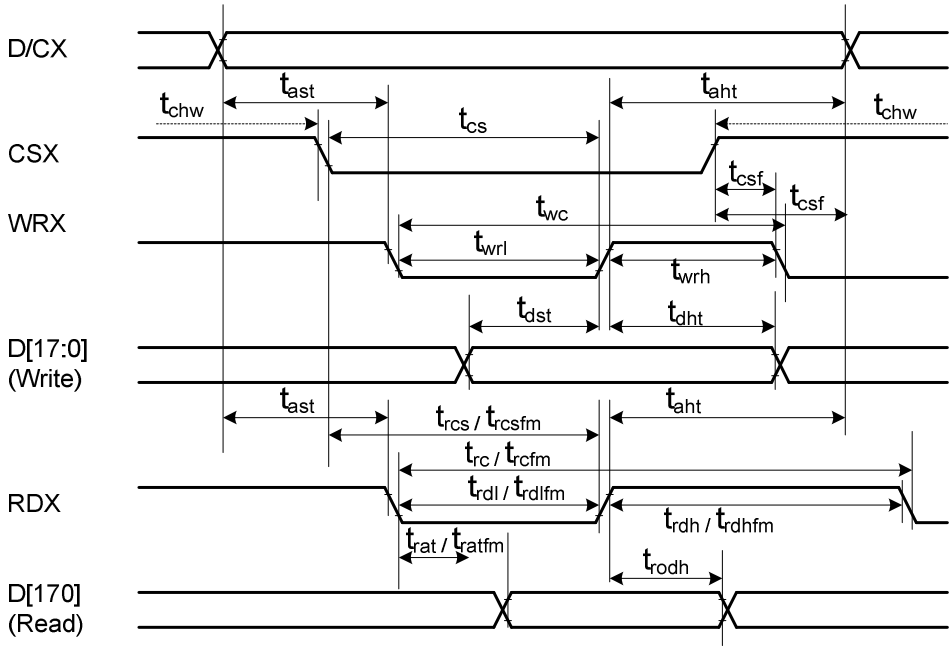
Note3: CSX, RDX, WRX, DB[17:0], D/CX, RESX, TE, SDA, SCL, IM2, IM1, IM0, and Test pins.

Note5: Source channel loading = 10pF/channel, Gate channel loading = 50pF/channel

Note6: The Max. Value is between with Note 4 measure point and Gamma setting value

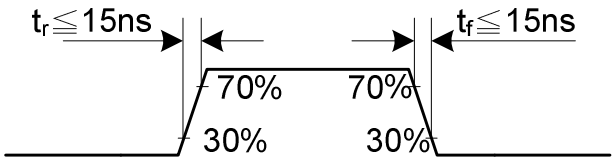
17.3. AC Characteristics

17.3.1. Display Parallel 18/16/9/8-bit Interface Timing Characteristics (8080-series)

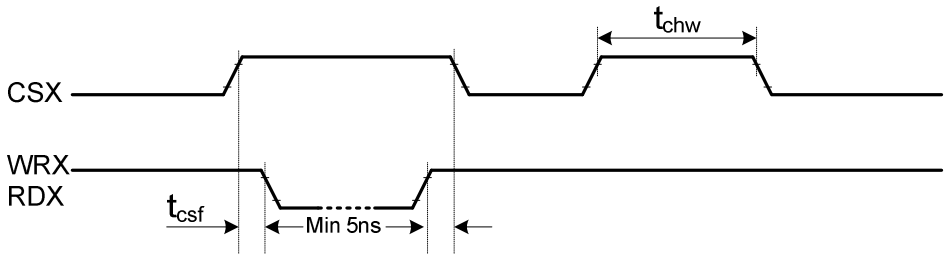


Signal	Symbol	Parameter	min	max	Unit	Description
DCX	tast	Address setup time	0	-	ns	-
	taht	Address hold time (Write/Read)	0	-	ns	-
CSX	tchw	CSX "H" pulse width	0	-	ns	-
	tcs	Chip Select setup time (Write)	15	-	ns	-
	trcs	Chip Select setup time (Read ID)	45	-	ns	-
	trcsfm	Chip Select setup time (Read FM)	355	-	ns	-
	tcsf	Chip Select Wait time (Write/Read)	0	-	ns	-
WRX	twc	Write cycle	66	-	ns	-
	twrh	Write Control pulse H duration	15	-	ns	-
	twrl	Write Control pulse L duration	15	-	ns	-
RDX (FM)	trcfm	Read Cycle (FM)	450	-	ns	When read from Frame Memory
	trdhfm	Read Control H duration (FM)	90	-	ns	
	trdlfm	Read Control L duration (FM)	355	-	ns	
RDX (ID)	trc	Read cycle (ID)	160	-	ns	When read ID data
	trdh	Read Control pulse H duration	90	-	ns	
	trdl	Read Control pulse L duration	45	-	ns	
DB[17:0], DB[15:0], DB[8:0] DB[7:0]	tdst	Write data setup time	10	-	ns	For maximum CL=30pF For minimum CL=8pF
	tdht	Write data hold time	10	-	ns	
	trat	Read access time	-	40	ns	
	tratfm	Read access time	-	340	ns	
	trod	Read output disable time	20	80	ns	

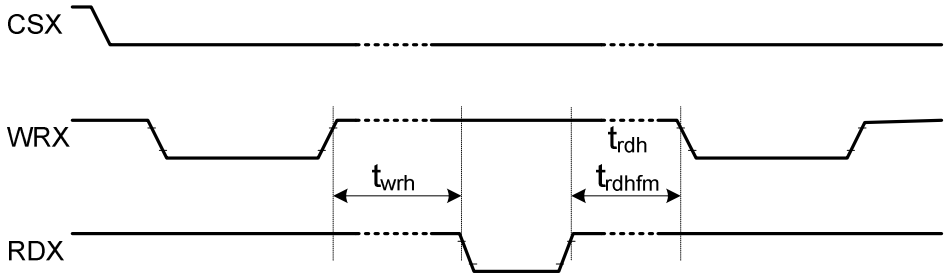
Note: (1) Ta = -30 to 70 ℃, IOVCC=1.65V to 3.6V, VCI=2.5V to 3.6V, AGND=DGND=0V



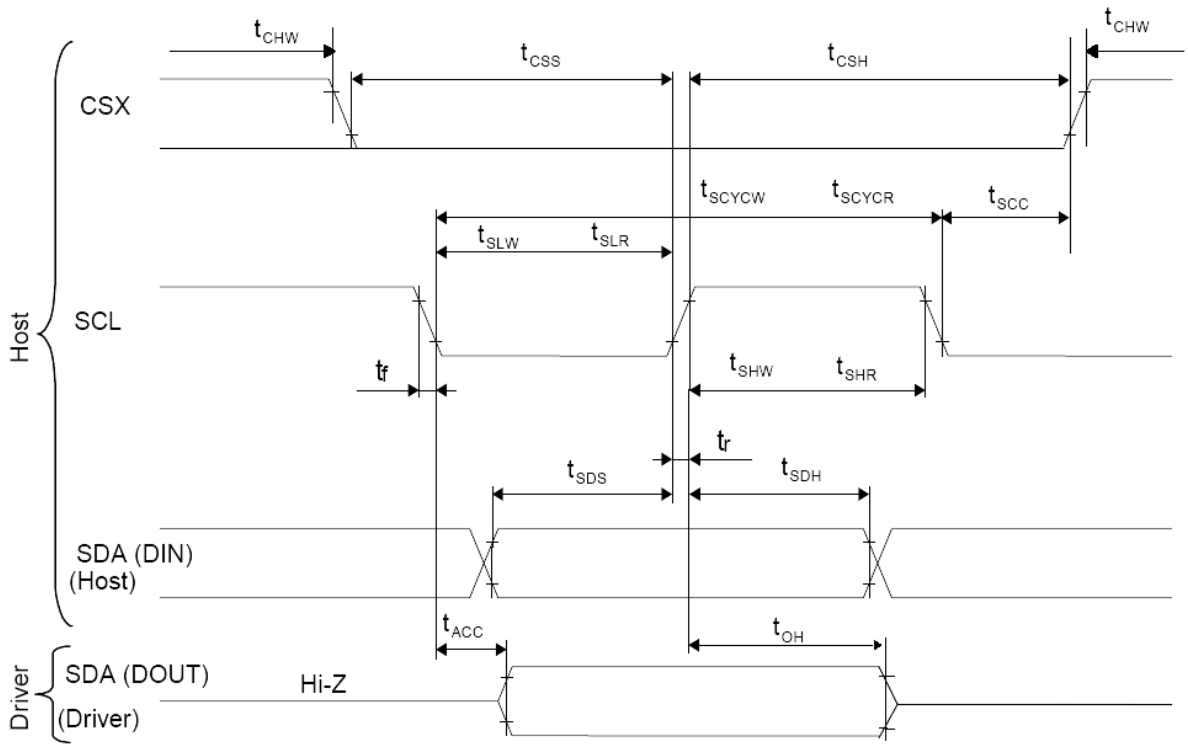
(2) Logic high and low levels are specified as 30% and 70% of IOVCC for input signals.



(3) Logic high and low levels are specified as 30% and 70% of IOVCC for input signals.

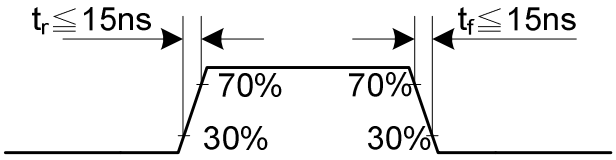


17.3.2. Display Serial Interface Timing Characteristics (3-line SPI system)

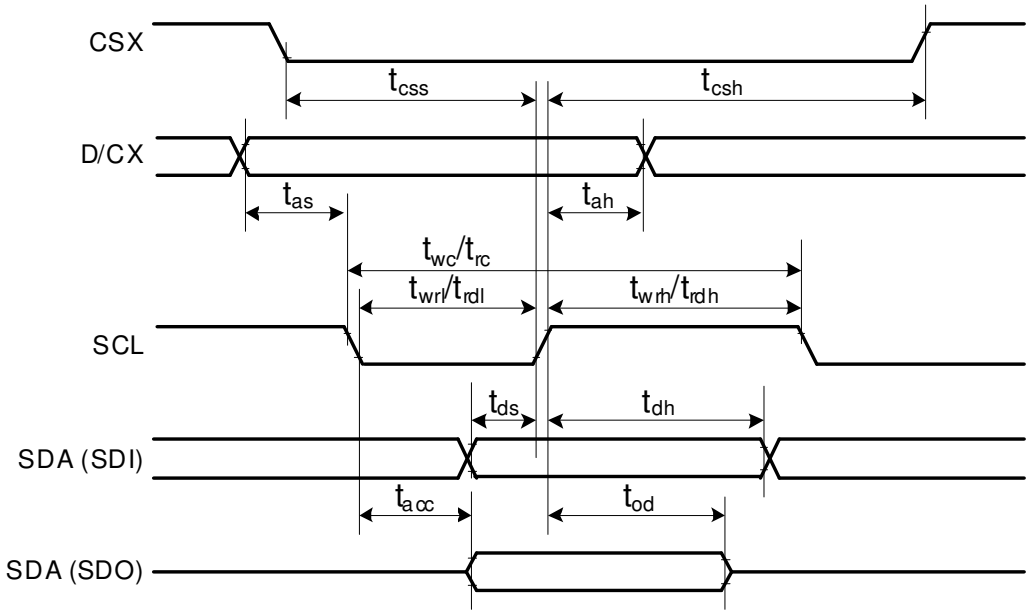


Signal	Symbol	Parameter	min	max	Unit	Description
SCL	tscycw	Serial Clock Cycle (Write)	66	-	ns	
	tshw	SCL “H” Pulse Width (Write)	15	-	ns	
	tslw	SCL “L” Pulse Width (Write)	15	-	ns	
	tscycr	Serial Clock Cycle (Read)	150	-	ns	
	tshr	SCL “H” Pulse Width (Read)	60	-	ns	
	tslr	SCL “L” Pulse Width (Read)	60	-	ns	
SDA / SDI (Input)	tsds	Data setup time (Write)	10	-	ns	
	tsdh	Data hold time (Write)	10	-	ns	
SDA / SDO (Output)	tacc	Access time (Read)	10	50	ns	
	toh	Output disable time (Read)	15	50	ns	
CSX	tscc	SCL-CSX	15	-	ns	
	tchw	CSX “H” Pulse Width	40	-	ns	
	tcss	CSX-SCL Time	60	-	ns	
	tcsh		65	-	ns	

Note: Ta = -30 to 70 ℃, IOVCC=1.65V to 3.6V, VCI=2.5V to 3.6V, AGND=DGND=0V, T=10+/-0.5ns



17.3.3. Display Serial Interface Timing Characteristics (4-line SPI system)

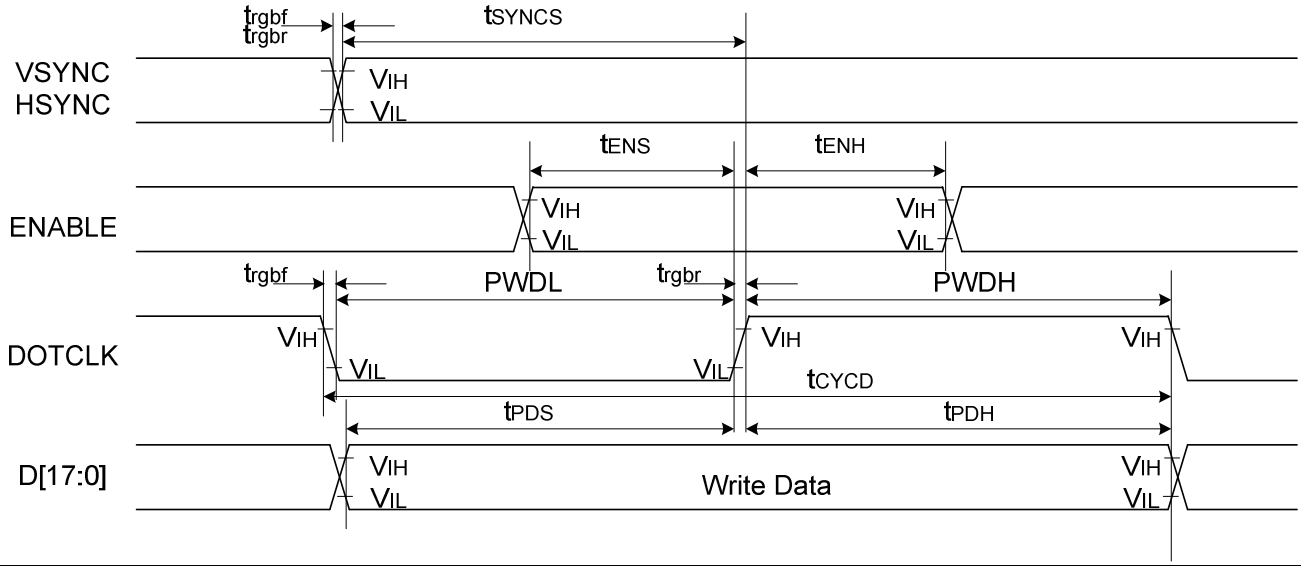


Signal	Symbol	Parameter	min	max	Unit	Description
CSX	tcss	Chip select time (Write)	15	-	ns	
	tcsh	Chip select hold time (Read)	60	-	ns	
SCL	twc	Serial clock cycle (Write)	66	-	ns	
	twrh	SCL “H” pulse width (Write)	15	-	ns	
	twrl	SCL “L” pulse width (Write)	15	-	ns	
	trc	Serial clock cycle (Read)	150	-	ns	
	trdh	SCL “H” pulse width (Read)	60	-	ns	
	trdl	SCL “L” pulse width (Read)	60	-	ns	
D/CX	tas	D/CX setup time	10	-	ns	
	tah	D/CX hold time (Write / Read)	10	-	ns	
SDA / SDI (Input)	tds	Data setup time (Write)	10	-	ns	
	tdh	Data hold time (Write)	10	-	ns	
SDA / SDO (Output)	tacc	Access time (Read)	10	50	ns	For maximum CL=30pF
	tod	Output disable time (Read)	15	50	ns	For minimum CL=8pF

Note: (1) Ta = -30 to 70 ℃, IOVCC=1.65V to 3.6V, VCI=2.5V to 3.6V, AGND=DGND=0V, T=10+/-0.5ns.

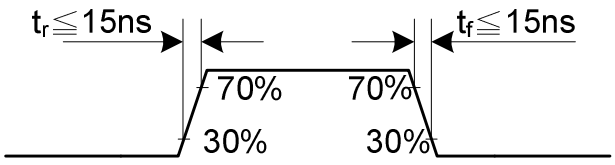
(2) Does not include signal rise and fall times.

17.3.4. Parallel 18/16-bit RGB Interface Timing Characteristics



Signal	Symbol	Parameter	min	max	Unit	Description
VSYNC / HSYNC	t_{SYNCS}	VSYNC/HSYNC setup time	15	-	ns	
	t_{SYNCH}	VSYNC/HSYNC hold time	15	-	ns	
ENABLE	t_{ENS}	ENABLE setup time	15	-	ns	
	t_{ENH}	ENABLE hold time	15	-	ns	
DB[17:0]	t_{POS}	Data setup time	15	-	ns	18/16-bit bus RGB interface mode
	t_{PDH}	Data hold time	15	-	ns	
DOTCLK	PWDH	DOTCLK high-level period	15	-	ns	
	PWDL	DOTCLK low-level period	15	-	ns	
	t_{CYCD}	DOTCLK cycle time	66	-	ns	
	t_{rgbr} , t_{rgbf}	DOTCLK,HSYNC,VSYNC rise/fall time	-	15	ns	

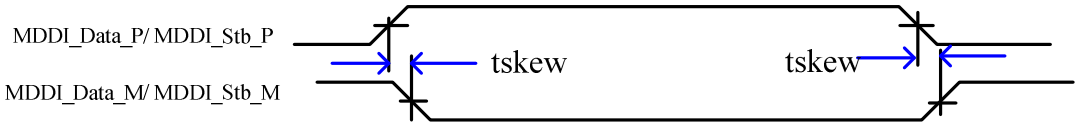
Note: Ta = -30 to 70 ℃, IOVCC=1.65V to 3.6V, VCI=2.5V to 3.3V, AGND=DGND=0V



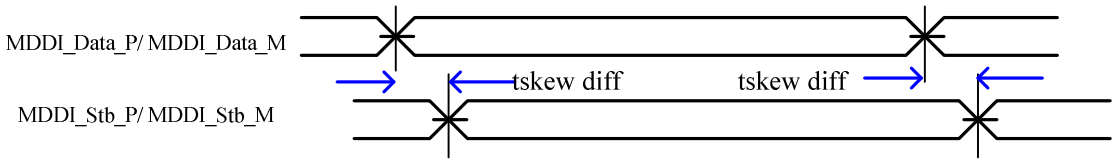
17.3.5. MDDI Receiver Timing Characteristics

Item	Symbol	Rating			Unit	Terminals
		Min	Typ	Max		
Data transfer rate	1/t Bit	-	-	400	Mbps	MDDI_Data_P, MDDI_Data_M MDDI_Stb_P, MDDI_Stb_M
Differential Transfer Input Skew	| ± tskew|	-	-	0.25	nsec	MDDI_Data_P, MDDI_Data_M MDDI_Stb_P, MDDI_Stb_M
Data_ Strobe Input Skew	| ± tskew diff|	-	-	2	nsec	MDDI_Data_P, MDDI_Data_M MDDI_Stb_P, MDDI_Stb_M

Skew between positive and negative

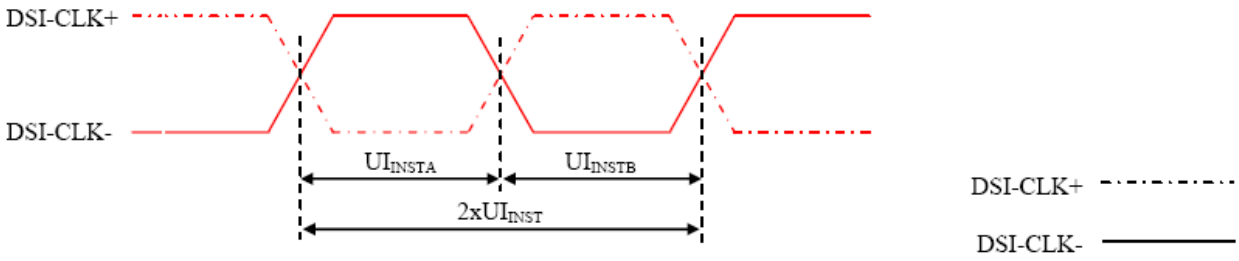


Skew between Data and Strobe



17.3.6. DSI

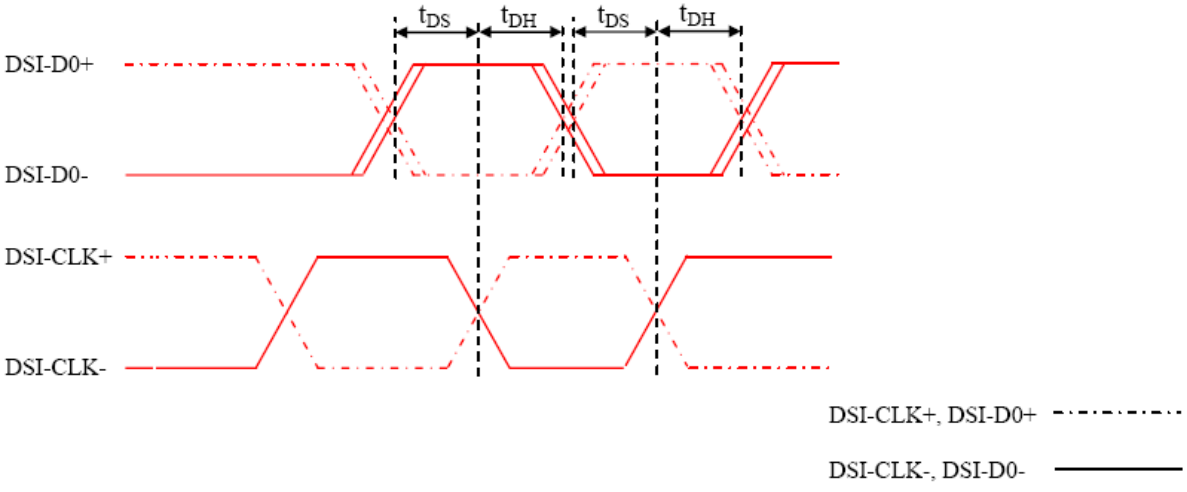
17.3.6.1. High Speed Mode – Clock Channel Timing



Signal	Symbol	Parameter	Min	Max	Unit
DSI-CLOCK_P/N	$2xUI_{INST}$	Double UI instantaneous	4	25	ns
DSI-CLOCK_P/N	UI_{INSTA},UI_{INSTB}	UI instantaneous Half	2	12.5	ns

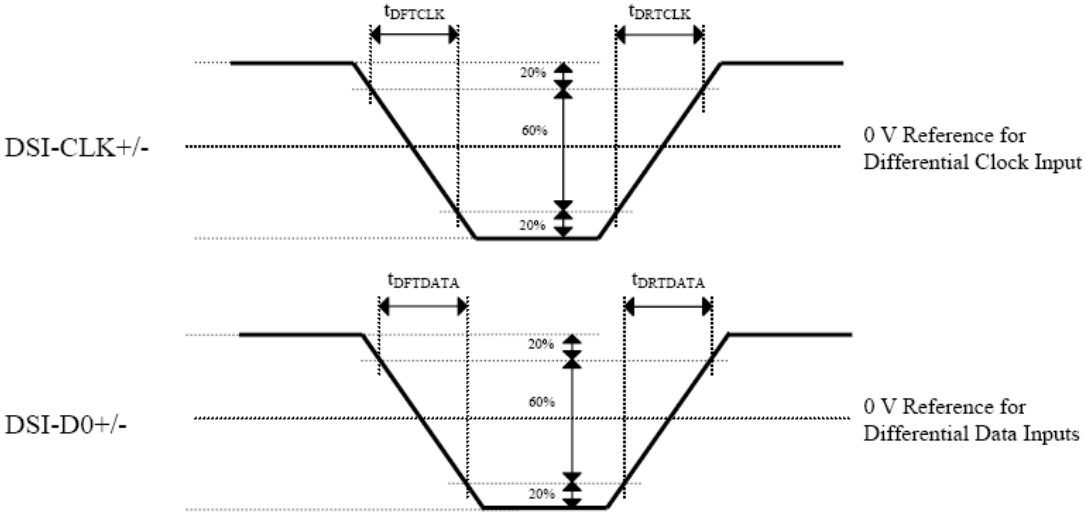
Note: UI = UI_{INSTA} = UI_{INSTB}

17.3.6.2. High Speed Mode – Data Clock Channel Timing



Signal	Symbol	Parameter	Min	Max	Unit
DSI-DATA_P/N	t_{DS}	Data to Clock Setup time	300	-	ps
DSI-DATA_P/N	t_{DH}	Clock to Data Hold Time	300	-	ps

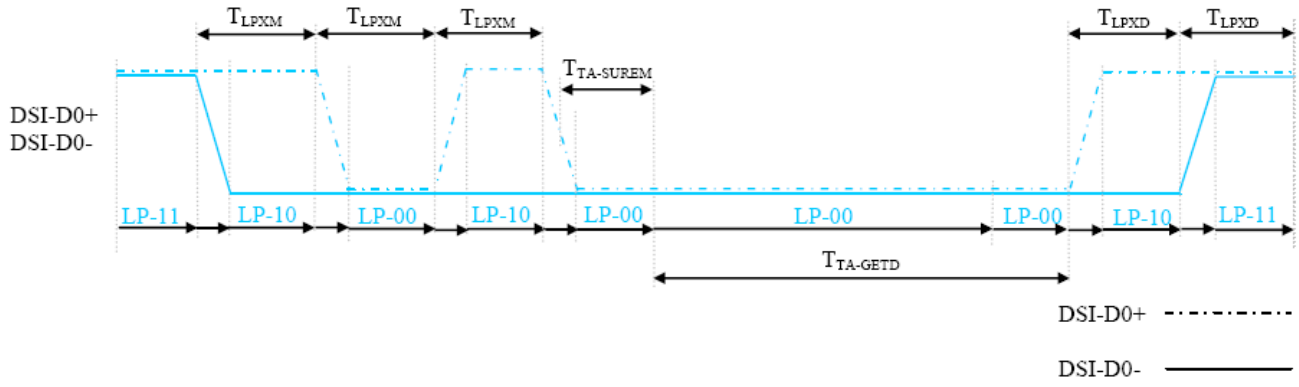
17.3.6.3. High Speed Mode – Rise and Fall Timings



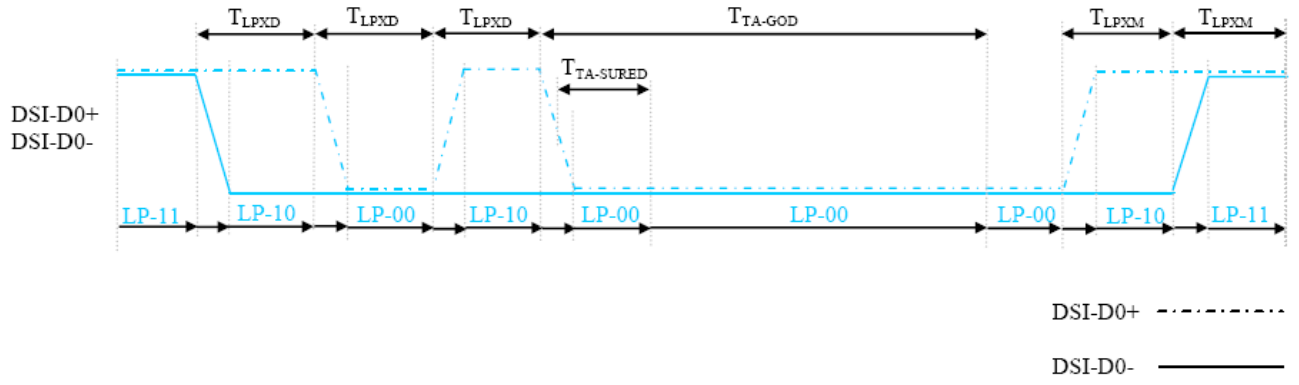
Parameter	Symbol	Condition	Specification			
			Min	Typ	Max	Unit
Differential Rise Time for Clock	t_{DRTCLK}	DSI-CLOCK_P/N	-	-	900	ps
Differential Rise Time for Data	$t_{DRTDATA}$	DSI-DATA_P/N	-	-	900	ps
Differential Fall Time for Clock	t_{DFTCLK}	DSI-CLOCK_P/N	-	-	900	ps
Differential Fall Time for Data	$t_{DFTDATA}$	DSI-DATA_P/N	-	-	900	ps

17.3.6.4. Low Speed Mode – Bus Turn Around

Lower Power Mode and its State Periods are illustrated for reference purposes on the Bus Turnaround (BTA) from the MCU to the ILI9486 sequence below.



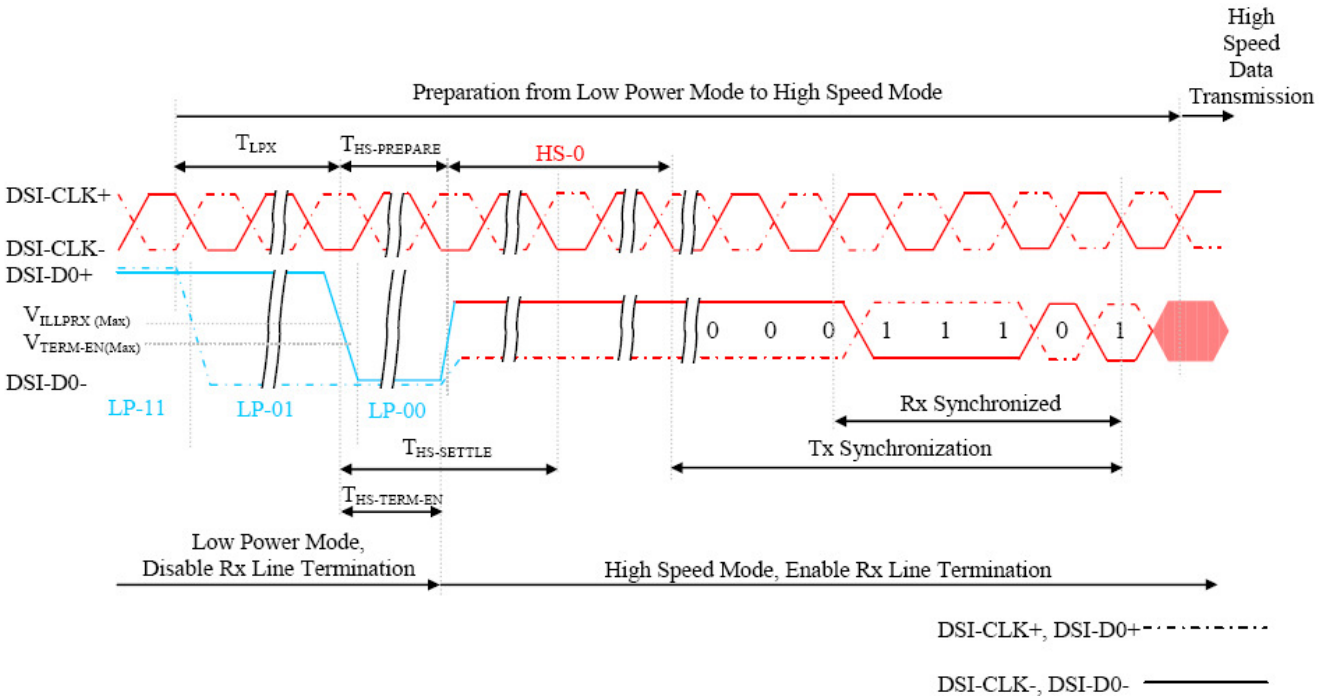
Lower Power Mode and its State Periods are illustrated for reference purposes on the Bus Turnaround (BTA) from ILI9486 to the MCU sequence below.



Signal	Symbol	Description	Min	Max	Unit
Input (DSI-DATA_P/N)	T_{LPXM}	Length of LP-00, LP-01, LP-10 or LP-11 periods MCU ➔ ILI9486	50	-	ns
Input (DSI-DATA_P/N)	$T_{TA-SUREM}$	Time-out before the ILI9486 starts driving	T_{LPXM}	$2xT_{LPXM}$	ns
Output (DSI-DATA_P/N)	T_{LPXD}	Length of LP-00, LP-01, LP-10 or LP-11 periods ILI9486 ➔ MCU	50	75	ns
Output (DSI-DATA_P/N)	$T_{TA-SURED}$	Time-out before the MCU starts driving	T_{LPXD}	$2xT_{LPXD}$	ns

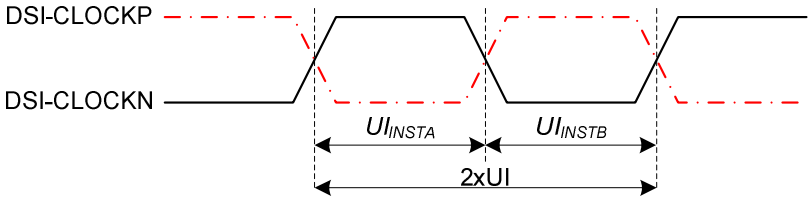
Signal	Symbol	Description	Time	Unit
Input (DSI-DATA_P/N)	$T_{TA-GETD}$	Time to drive LP-00 by ILI9486	$5xT_{LPXD}$	ns
Output (DSI-DATA_P/N)	T_{TA-GOD}	Time to drive LP-00 after turnaround request - MCU	$4xT_{LPXD}$	ns

17.3.6.5. Data Lanes from Low Power Mode to High Speed Mode

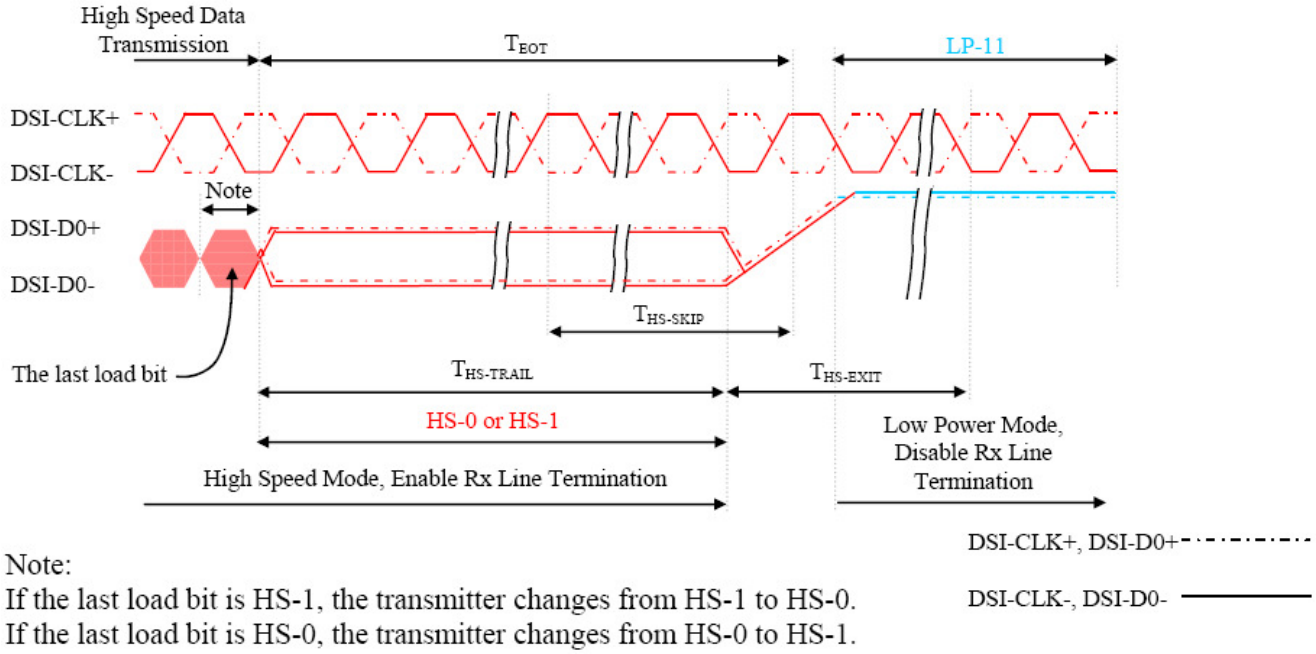


Signal	Symbol	Description	Min	Max	Unit
Input (DSI-DATA_P/N)	T_{LPX}	Length of any Low Power State Period	50	-	ns
Input (DSI-DATA_P/N)	$T_{HS-PREPARE}$	Time to Drive LP-00 to prepare for HS Transmission	40+4xUI	85+6xUI	ns
Input (DSI-DATA_P/N)	$T_{HS-TERM-EN}$	Time to enable Data Lane Receiver line termination measured from when D_n crosses V_{ILMAX}	-	35+4xUI	ns

Note: UI definition : UI = UI_{INSTA} = UI_{INSTB}



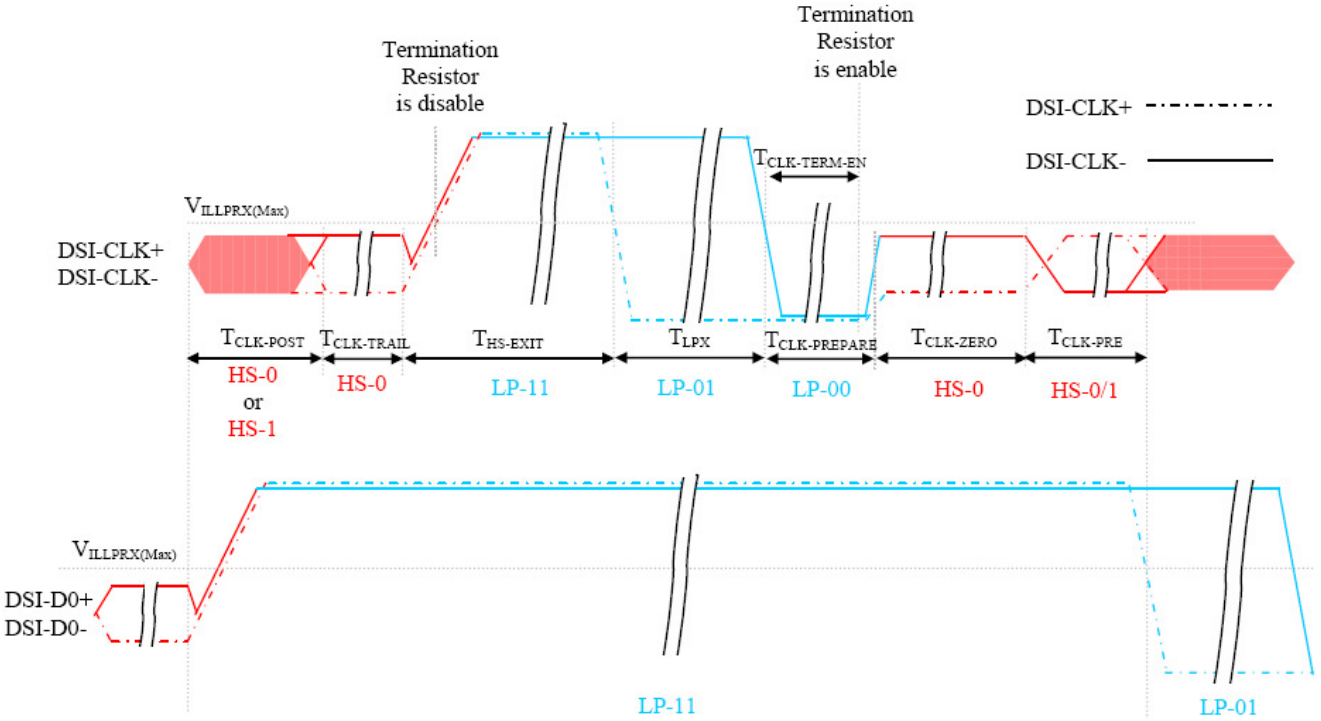
17.3.6.6. Data Lanes from High Speed Mode to Low Power Mode



Note:
If the last load bit is HS-1, the transmitter changes from HS-1 to HS-0.
If the last load bit is HS-0, the transmitter changes from HS-0 to HS-1.

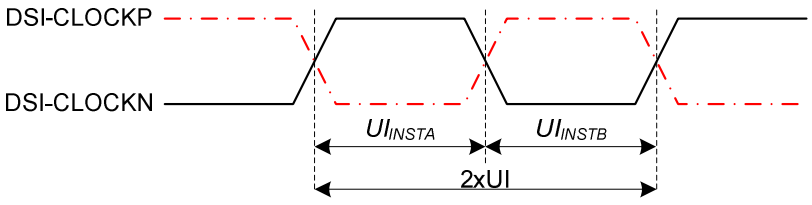
Signal	Symbol	Description	Min	Max	Unit
Input (DSI-DATA_P/N)	$T_{HS-SKIP}$	Time-out at ILI9486 to Ignore Transition Period of EoT	40	50+4xUI	ns
Input (DSI-DATA_P/N)	$T_{HS-EXIT}$	Time to Driver LP-11 after HS burst	100	-	ns

17.3.6.7. DSI Clock Burst – High Speed Mode to/from Low Power Mode

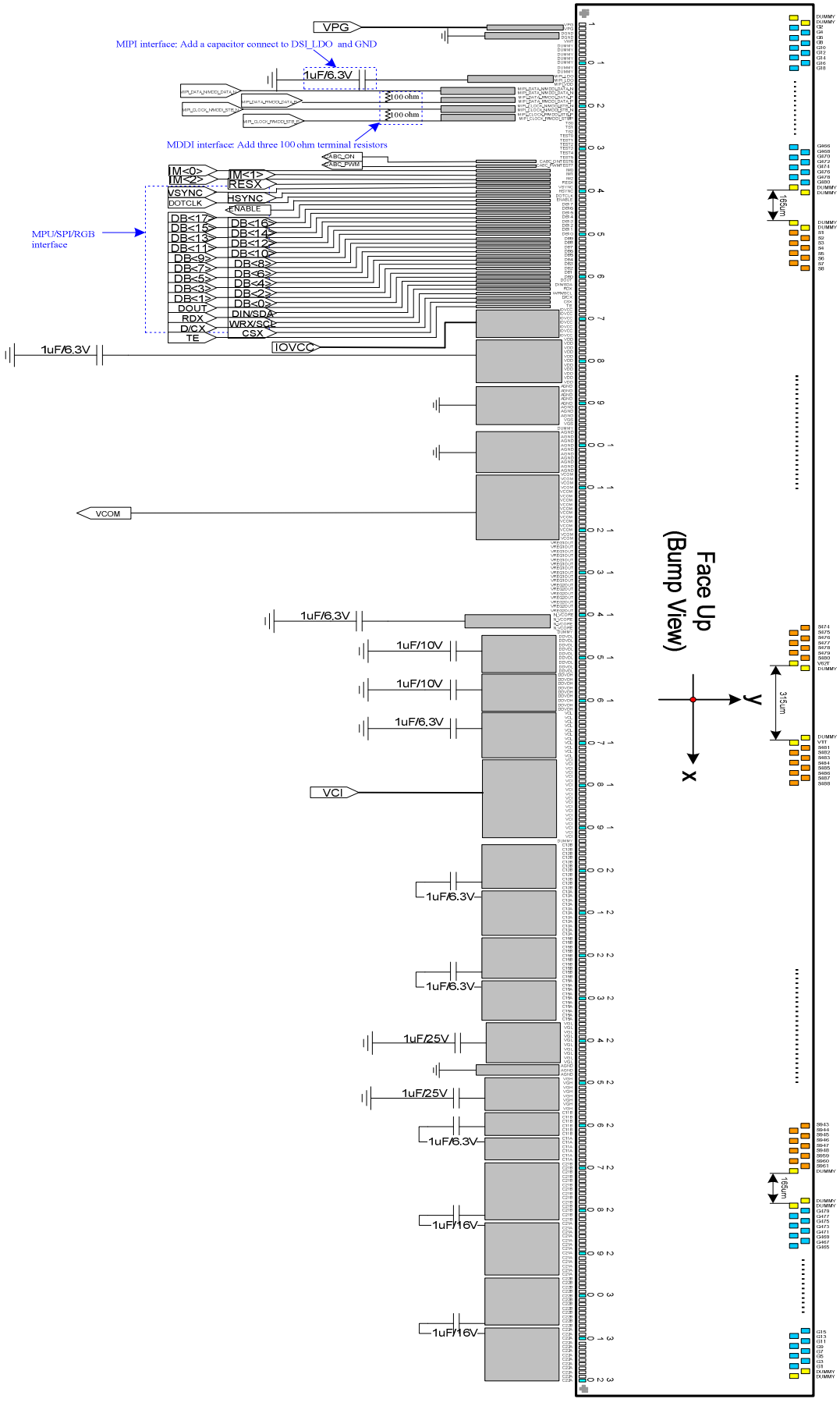


Signal	Symbol	Description	Min	Max	Unit
Input (DSI-CLOCK_P/N)	$T_{CLK-POST}$	Time that the MCU shall continue sending HS clock after the last associated Data Lanes has transitioned to LP mode	60+52xUI	-	ns
Input (DSI-CLOCK_P/N)	$T_{CLK-TRAIL}$	Time to drive HS differential state after last payload clock bit of a HS transmission burst	60	-	ns
Input (DSI-CLOCK_P/N)	$T_{HS-EXIT}$	Time to drive LP-11 after HS burst	100	-	ns
Input (DSI-CLOCK_P/N)	$T_{CLK-PREPARE}$	Time to drive LP-00 to prepare for HS transmission	38	95	ns
Input (DSI-CLOCK_P/N)	$T_{CLK-TERM-EN}$	Time-out at Clock Lane to enable HS termination	-	38	ns
Input (DSI-CLOCK_P/N)	$T_{CLK-PREPARE}$	Minimum lead HS-0 drive period before starting Clock	300	-	ns
Input (DSI-CLOCK_P/N)	$T_{CLK-PRE}$	Time that the HS clock shall be driven prior to any associated Data Lane beginning the transition from LP to HS mode	8xUI	-	ns

Note: UI definition : UI = UI_{INSTA} = UI_{INSTB}



18. Application Circuit



The following table shows specifications of external elements connected to the ILI9486's power supply circuit.

Items	Recommended Specification	Pin connection
Capacity 1 µF (B characteristics)	6.3V	C11A/B, C13A/B, C15A/B, VCL(back up), VDD(back up), N_VCORE(back up)
	10V	DDVDH, DDVDL
	16V	C21 A/B, C22A/B(for +6,-3 backup)
	25V	VGH (back up), VGL (back up)

19. Revision History

Version No.	Date	Page	Description
V.001	2010/09/02	All	New created
V.001	2010/11/04	147 286 310	Modify command list Add LCM voltage generation Application circuit